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A Gate Driver for Crosstalk Suppression of eGaN HEMT Power Devices

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Abstract

The eGaN HEMT power devices face serious crosstalk problems when applied to high-frequency bridge circuits, thereby limiting the switching performance of these devices. To address this issue, a gate driver is proposed in this paper that can suppress both positive and negative crosstalk of eGaN HEMT power devices, offering the advantages of simple control and easy integration. The basic idea is to suppress positive crosstalk by constructing a negative voltage capacitor, and to suppress negative crosstalk by reducing the impedance of the gate loop. To verify the capability of the proposed gate driver, double-pulse and synchronous Buck test platforms are constructed. The experimental results clearly demonstrate that the proposed gate driver reduces the positive and negative crosstalk spikes by 2.03 V and 1.54 V, respectively, ensuring that the positive and negative crosstalk spikes fall within a safe operating range. Additionally, the turn-off speed of the device is enhanced, leading to a reduction in switching loss.

Keywords: gate driver; eGaN HEMT; crosstalk suppression; phase-leg configuration

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1. Introduction

GaN power devices have many advantages, such as low on-resistance, excellent thermal conductivity, and fast switching speed [1–4]. The eGaN HEMT devices are increasingly favored by the market due to their excellent performance, including higher operating frequency, higher blocking voltage, and higher operating temperature [5–9]. In the application of eGaN HEMT power devices, the switching frequency of the power converter can reach several MHz, which improves the power density [10–14]. However, compared with Si devices, eGaN HEMT power devices have lower threshold voltages and smaller gate reverse voltage withstand capabilities, which are easily threatened by crosstalk voltage spikes triggered by higher dv/dt and di/dt in applications such as high-power bridge circuits, and may even lead to device misconduct or gate reverse breakdown conditions [15]. To guarantee the safe and stable operation of power devices, scholars have proposed different solutions to cope with the challenges posed by the crosstalk problem.

There are three main types of crosstalk suppression methods: reducing the amplitude of the device dv/dt and di/dt variations, minimizing the impedance of the drive loop, and using negative voltage turn-off. A specific analysis of these three types is as follows:

(1) Reducing the amplitude of device dv/dt and di/dt variations [16–18]: The fundamental idea is to directly reduce the magnitude of the Miller current. In [17], a capacitor is proposed to be connected in parallel with the gate-source capacitance, which achieves good crosstalk suppression but affects the device's turn-on speed.

In [18], the study implements soft switching to suppress crosstalk voltage spikes by exploiting the critical conduction mode of the current; however, it is difficult to apply in high-power applications. These negative effects limit the practical value of crosstalk suppression circuits.

(2) Minimizing the impedance of the drive loop [19–21]: The fundamental idea is to provide a low-impedance path for Miller current [19]. The effect of crosstalk can be counteracted by actively injecting a current into the gate, with the current flowing in the opposite direction to the Miller current [20]. Adding a Miller clamping circuit to supply a low-impedance branch is proposed to reduce crosstalk [21]. However, the two methods add extra transistors, increasing the power loss.

(3) Using negative voltage turn-off [22–29]: The fundamental idea is to pull down the positive crosstalk voltage spike below the device threshold voltage to reduce the risk of device misconduct. It is an effective approach to suppress positive crosstalk, and the main measures include adding a negative voltage or a voltage divider circuit. By adding a negative voltage across the device's gate-source, the positive crosstalk spike would be reduced; however, this approach introduces a larger negative crosstalk spike, which may damage the device [22]. In [23], a RCD (resistor–capacitor–diode) voltage divider circuit is proposed to suppress positive crosstalk, but it affects the turn-on speed of the devices and exacerbates negative crosstalk. The gate driver proposed in [24] enables negative voltage recovery, but does not address the problem of affecting the turn-on speed of the device. On this basis, the multi-level structure, due to the large voltage difference between each level, can suppress crosstalk through active clamping of negative voltage turn-off [25–27]. However, employing multiple power supplies and switching devices will increase the cost of circuit design and the complexity of control.

In summary, existing crosstalk suppression circuits have problems such as complicated control and exacerbated negative crosstalk. Therefore, this paper proposes a gate driver that suppresses positive crosstalk by constructing a negative voltage capacitor and suppresses negative crosstalk by minimizing the impedance of the drive loop. The circuit has the advantages of being simple to control and speeding up the device's turn-off. This paper first analyses the mechanism of crosstalk and explains the operating modes of the proposed gate driver. On this basis, the design criteria for component parameters are presented. Finally, the proposed gate driver is validated by building a double-pulse and synchronous Buck test platform.

2. Crosstalk Mechanism Analysis

To facilitate the analysis of the crosstalk problem formation in eGaN HEMT power devices [22], a simplified equivalent half-bridge circuit is used as an example, as shown in Figure 1. According to Kirchhoff's formula:

$$\begin{cases} v_{\mathrm{dsL}} = v_{\mathrm{gsL}} + v_{\mathrm{gdL}} \\ v_{\mathrm{gsL}} = R_{\mathrm{gL}}\left(C_{\mathrm{gdL}}\frac{dv_{\mathrm{gdL}}}{dt} - C_{\mathrm{gsL}}\frac{dv_{\mathrm{gsL}}}{dt}\right) + v_{\mathrm{gL}} \\ v_{\mathrm{dsL}} = at \end{cases} \tag{1}$$

where a is the rate of change of v_{dsL} [22], v_{gsL} and v_{gdL} are the gate-source and gate-drain voltages of eGaN$_{\mathrm{L}}$, respectively, C_{gsL} is the gate-source capacitance, and v_{gL} is the voltage of the eGaN$_{\mathrm{L}}$ driver IC.

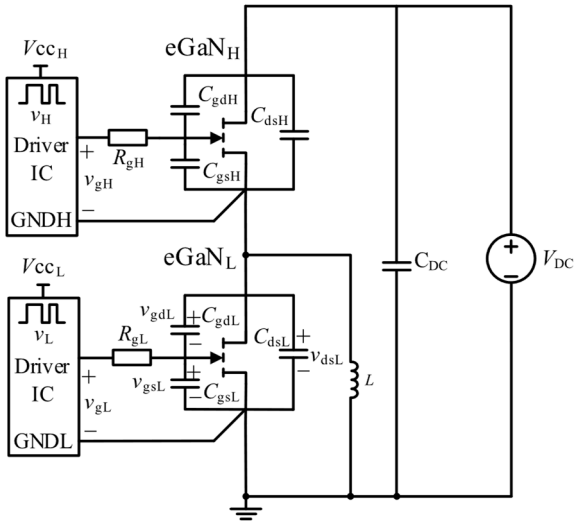


Figure 1. Schematic diagram of the $eGaN_H$ turn-on in a half-bridge circuit.

The time-domain expression for crosstalk voltage v_{gsL} at the gate-source of $eGaN_L$ is derived from Equation (1):

$$v_{gsL} = (aR_{gL}C_{gdL} + v_{gL})(1 - e^{\frac{-t}{R_{gL}(C_{gsL}+C_{gdL})}}) \quad (2)$$

From the above equation, v_{gL} is 0 V, because the drive signal of the $eGaN_L$ is at a low level at this moment, and the v_{gsL} increases with t. Then, when $t = V_{DC}/a$, the source voltage v_{gsL} reaches its maximum value, i.e., the maximum positive crosstalk voltage.

$$v_{gsLmax} = aR_{gL}C_{gdL}(1 - e^{\frac{-V_{DC}}{aR_{gL}(C_{gsL}+C_{gdL})}}) \quad (3)$$

Based on the analysis above, it is evident that v_{gsLmax} is positively correlated with bus voltage V_{DC}, drive resistor R_{gL}, and gate-drain capacitance C_{gdL}, but negatively correlated with the gate-source capacitance C_{gsL}. So, the amplitude of v_{gsLmax} can be reduced by decreasing R_{gL} and increasing C_{gsL}. Equivalently, one can derive the negative crosstalk voltage spike on $eGaN_L$ when $eGaN_H$ is turned off.

3. Design of the Proposed Gate Driver

To solve the problems of the existing crosstalk suppression circuit, such as its complex structure and numerous control signals, this paper proposes a crosstalk suppression gate driver using only passive components. It employs capacitor discharge as the core principle to suppress positive crosstalk voltage spikes and reduces the impedance of the gate driver as the core principle to suppress negative crosstalk voltage spikes.

As shown in Figure 2, the crosstalk suppression gate driver consists of three units. The voltage regulator unit (G_1) includes diode D_3, voltage regulator diode D_4, and drive resistor R_4. The negative voltage unit (G_2) includes capacitor C_1, voltage regulator diode D_2, and resistor R_2. By selecting the appropriate capacitance value for capacitor C_1, negative voltage turn-off can be achieved, thereby inhibiting positive crosstalk. The low-impedance unit (G_3) comprises resistor R_1 and diode D_1. Selecting the appropriate resistance value for resistor R_1 can reduce the gate-source drive loop's impedance to suppress negative crosstalk. Resistor R_3 is a current-limiting resistor, whose primary function is to ensure the safe operation of voltage regulator diodes D_2 and D_4.

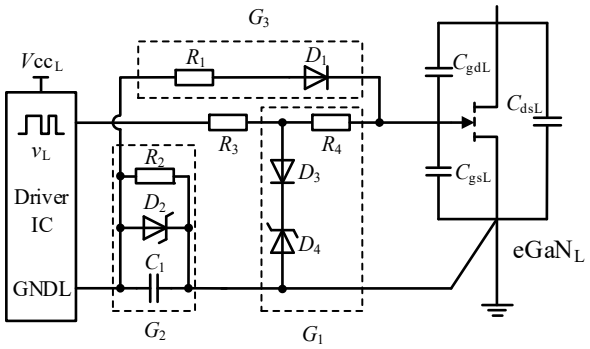


Figure 2. Proposed gate driver topology.

In this paper, the eGaN$_L$ is taken as an example to demonstrate how the proposed gate driver works. Figure 3 shows the drive signals v_H for eGaN$_H$ and v_L for eGaN$_L$, along with the drain-source v_{dsL} and gate-source v_{gsL} voltage waveforms of eGaN$_L$. The working mechanism of the proposed gate driver can be described as follows.

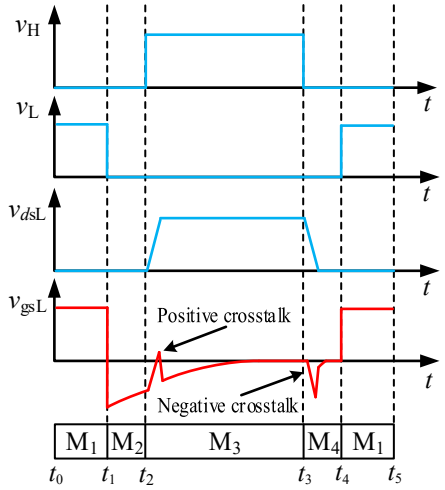


Figure 3. Timing diagram of proposed gate driver.

M$_1$ [t_0~t_1] [t_4~t_5]: The circuit operating mode is shown in Figure 4a. At this stage, the drive voltage of eGaNH is low and it is turned off, while the drive voltage of eGaNL is high and it is turned on. Additionally, the bus voltage V_{DC} is applied on both ends of the eGaN$_H$ drain-source pole. The drive voltage amplitude is equal to the sum of the current-limiting resistor R_3's voltage drop, diode D_3's voltage drop, the voltage regulator diode D_4's regulated value, and the charging voltage of capacitor C_1. During this period, the drive voltage charges capacitor C_1, polarizing it with the left terminal negative and the right terminal positive.

M$_2$ [t_1~t_2]: The circuit operating mode is shown in Figure 4b. This phase is the transition phase of the eGaN$_H$ and eGaN$_L$; the drive voltages of eGaN$_H$ and eGaN$_L$ are low, and they are turned off. The charge entering capacitor C_1 in the turn-on phase is released through resistor R_2 on the one hand, and through drive resistor R_4 and current-limiting resistor R_3 on the other, constituting two discharge circuits. Diode D_3 and voltage regulator diode D_4 are in the cut-off state, and the discharge loop forms a negative voltage across the C_{gsL}, which accelerates the turn-off of eGaN$_L$.

M$_3$ [t_2~t_3]: The circuit operating mode is shown in Figure 4c. At this stage, the drive voltage of eGaNH is high, and it is turned on. The drive voltage of eGaNL is low, keeping it off. The vdsL of eGaN$_L$ gradually rises to the bus voltage V_{DC}. During this period, diodes

D_1 and D_4 are in the cut-off state, blocking Miller current. Miller current, on the one hand, flows through resistors R_3 and R_4 to drive the GNDL; on the other hand, it flows through the gate-source capacitance C_{gsL}, capacitor C_1, and resistor R_2 to the GND_L. Currently, the voltage across capacitor C_1 counteracts the voltage across resistors R_3 and R_4, thereby reducing the positive crosstalk. After the positive crosstalk, the $eGaN_L$ remains turned off, capacitor C_1 is discharged through resistor R_2, and the gate-source voltage returns to 0 V.

M_4 [t_3~t_4]: The circuit operating state is shown in Figure 4d. At this stage, the eGaNH begins to be turned off at t_3. The drive signal of eGaNL is low, and it is turned off. Consequently, the VDSL gradually decreases from the bus voltage VDC to 0 V. At this stage, diodes D_3 and D_2 are in the cut-off state, blocking the Miller current. In high-frequency conditions, the impedance of capacitor C_1 is very low and can be approximated as that of a wire. In this stage, resistance R_2 is short-circuited by capacitance C_1. Miller current flows through capacitor C_1, current-limiting resistor R_3, and drive resistor R_4 to load L on one hand, and through capacitor C_1, resistor R_1, and diode D_1 to load L on the other hand. At this time, the two branches of the Miller current are in a parallel relationship, which reduces the voltage drop compared to a single circuit composed of a large resistor, thereby mitigating negative crosstalk.

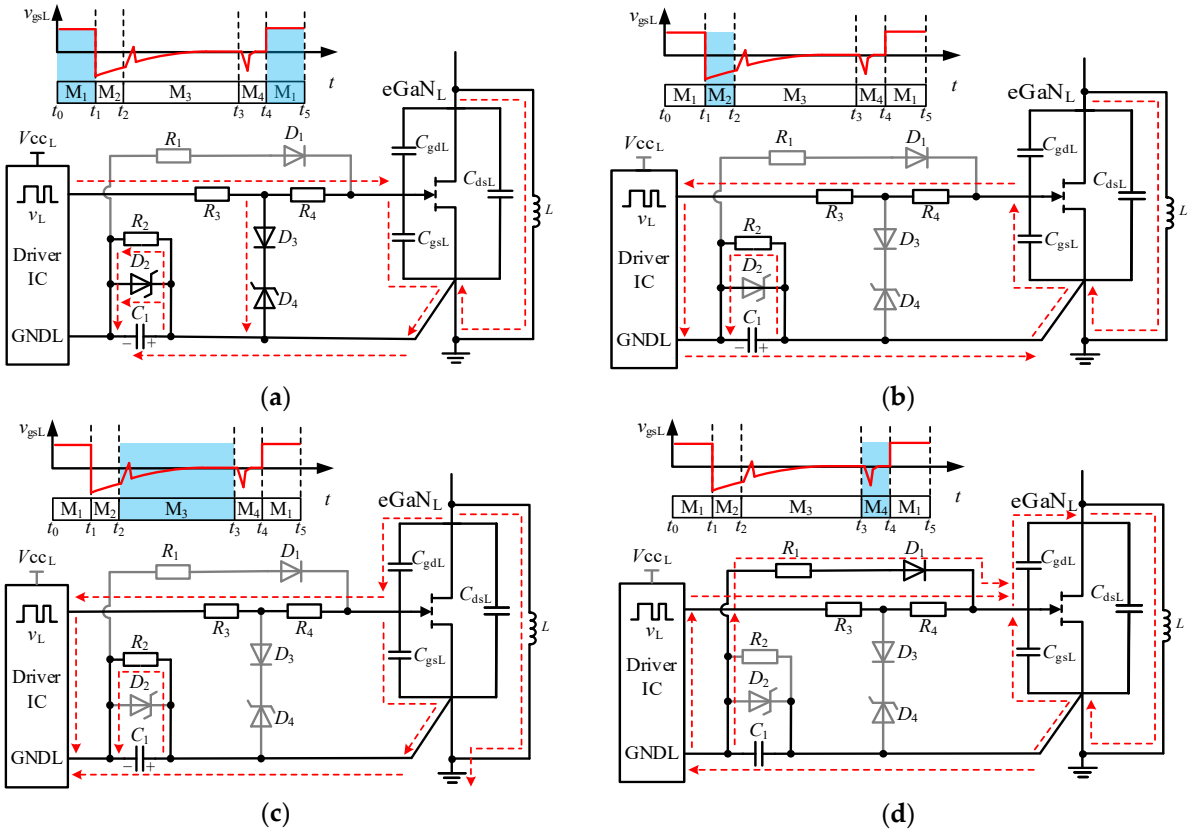


Figure 4. Gate driver modal diagram. (**a**) M_1: turn-on phase; (**b**) M_2: transition phase; (**c**) M_3: positive crosstalk suppression phase; and (**d**) M_4: negative crosstalk suppression phase.

4. Component Parameters Design

The crosstalk suppression capability of the proposed gate driver directly depends on the parameter values of the components in the circuit. The derivation of the range of the main component parameters is presented as follows.

4.1. Voltage Regulator Diode D_2

When the $eGaN_H$ is turned off and the $eGaN_L$ is turned on, the $eGaN_L$ drive voltage v_{gL} charges the capacitor C_1, and the voltage at the two terminals of C_1 is determined by the regulator value V_{D2} of D_2, which is connected in parallel with it. Capacitor C_1 begins to discharge through resistor R_2 at t_1. It can be obtained:

$$\begin{cases} v_{C1}(t_1) = V_{D2} \\ v_{C1} = R_2 C_1 \frac{dv_{C1}}{dt} \end{cases} \tag{4}$$

The collation leads to:

$$v_{C1} = V_{D2} e^{-\frac{t}{R_2 C_1}} \tag{5}$$

Then the voltage V_{t2} across C_1 at t_2 is:

$$V_{t2} = V_{D2} e^{-\frac{\Delta T_2}{R_2 C_1}} \tag{6}$$

where ΔT_2 is the duration of the transition phase (from t_1 to t_2).

Since the positive crosstalk suppression phase is much smaller than the time constant R_2C_1 of capacitor C_1 discharging through resistor R_2, it can be assumed that the voltage on capacitor C_1 is unchanged in this phase, and its value is the voltage of C_1 at t_2. The equivalent circuit is shown in Figure 5, the red arrow indicates the direction of current flow. From Figure 5:

$$\begin{cases} v_{gsL} + v_{gdL} = v_{dsL} = at \\ i_1 = C_{gdL} \frac{dv_{gdL}}{dt} - C_{gsL} \frac{dv_{gsL}}{dt} \\ (R_3 + R_4) i_1 - v_{gsL} - V_{t2} = 0 \end{cases} \tag{7}$$

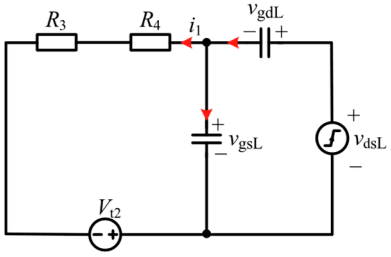


Figure 5. Positive crosstalk suppression phase equivalent circuit.

The collation leads to:

$$v_{gsL} = (aR_{gL}C_{gdL} - V_{t2})(1 - e^{-\frac{t}{C_{issL}R_{gL}}}) \tag{8}$$

where $R_{gL} = R_3 + R_4$, $C_{issL} = C_{gsL} + C_{gdL}$. From Equation (8), v_{gsL} is positively correlated with t; when $t \to V_{DC}/a$, v_{gsL} reaches its maximum value. Currently, it is necessary to meet the condition that the positive crosstalk voltage peak is less than the threshold voltage of the device.

$$aMR_{gL}C_{gdL} - MV_{D2} e^{-\frac{\Delta T_2}{R_2 C_1}} < V_{th} \tag{9}$$

where Vth represents the device's threshold voltage, M is for:

$$M = 1 - e^{-\frac{V_{DC}}{aC_{issL}R_{gL}}} \tag{10}$$

Capacitor C_1 is discharged through resistor R_2 during t_2~t_3. To prevent the voltage of C_1 from aggravating the negative crosstalk, the voltage at both ends of C_1 needs to be

restored to 0 V before t_3, when the negative crosstalk is generated. According to the RC discharge characteristics, the period ΔT_3 from t_2 to t_3 is defined as five times the discharge time constant R_2C_1:

$$\Delta T_3 = 5R_2C_1 \tag{11}$$

Combining Equations (9) and (11) yields:

$$V_{D2} > (aR_{gL}C_{gdL} - V_{th}M^{-1})e^{\frac{5\Delta T_2}{\Delta T_3}} \tag{12}$$

The negative voltage of capacitor C_1 cannot exceed the reverse breakdown voltage of the device gate, so the value of V_{D2} is as small as possible under the condition of satisfying Equation (12) to reduce the reverse voltage on the device gate.

4.2. Capacitor C_1

The value of capacitor C_1 needs to be selected considering the following two factors. The first factor is that the charge stored in C_1, Q_{C1}, should be larger than the total charge Q_{GL} of the gate capacitance of the device. When the device is turned off, the polarity of the voltage across C_1 is opposite to that of the gate parasitic capacitance, and C_1 must accommodate the Q_{GL}. The second factor is that the sum of the energy stored in C_1 and the energy required by the gate of the device should be smaller than the output energy of the driver IC, ensuring the reliable functioning of the driver IC.

For the first factor, to ensure that the amount of charge Q_{C1} stored in C_1 at device turn-off is sufficient to counteract the total gate charge Q_{GL} of the $eGaN_L$, Q_{C1} must satisfy the following condition.

$$Q_{C1} = C_1V_{D2} > Q_{GL} \tag{13}$$

For the second factor, the following condition must be satisfied to ensure that the driver's IC works properly.

$$P_D > \alpha(P_{C1} + P_{GL}) \tag{14}$$

where P_D is the supplied energy of the driver IC, P_{C1} is the energy stored in C_1, P_{GL} is the energy required for the gate of the device, and α is the safety margin factor ($\alpha > 1$). P_{C1} and P_{GL} can be expressed as follows [30]:

$$\begin{cases} P_{C1} = \frac{C_1{V_{D2}}^2 f_s}{2} \\ P_{GL} = V_{GL}Q_{GL}f_s \end{cases} \tag{15}$$

where f_s is the switching frequency of the $eGaN_L$, and V_{GL} is the drive voltage of the $eGaN_L$. Combining with Equations (13)–(15), the range of values of C_1 is determined as follows:

$$\frac{Q_{GL}}{V_{D2}} < C_1 < \frac{2(P_D - \alpha V_{GL}Q_{GL}f_s)}{\alpha {V_{D2}}^2 f_s} \tag{16}$$

Under the condition that Equation (16) is satisfied, the value of C_1 should be as small as possible. This will shorten the time for C_1 to discharge, enabling the eGaN device to operate at a higher switching frequency. Meanwhile, combining with Equation (11), the time constant of C_1 discharge, R_2C_1, and the device's switching frequency f_s should satisfy the following equation:

$$5R_2C_1 < \frac{1}{f_s} \tag{17}$$

4.3. Resistor R_1

Due to the unidirectional conductivity of diode D_1, resistor R_1 and diode D_1 operate only in the negative crosstalk suppression stage. The forward voltage drop of diode D_1 is

small and is ignored for ease of calculation. The equivalent circuit of the negative crosstalk phase is presented in Figure 6, the red arrow indicates the direction of current flow.

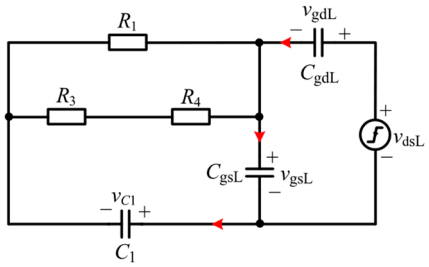


Figure 6. Negative crosstalk suppression phase equivalent circuit.

Writing Kirchhoff's laws for Figure 6 yields:

$$\begin{cases} C_1\frac{dv_{C1}}{dt} + C_{gdL}\frac{dv_{gdL}}{dt} = C_{gsL}\frac{dv_{gsL}}{dt} \\ v_{dsL} = v_{gdL} + v_{gsL} = V_{DC} - at \\ \frac{v_{gsL}+v_{C1}}{R_1} + \frac{v_{gsL}+v_{C1}}{R_3+R_4} = -C_1\frac{dv_{C1}}{dt} \end{cases} \tag{18}$$

The collation leads to:

$$v_{gsL} = -\frac{aC_{gdL}t}{B} - \frac{aC_1{}^2C_{gdL}R_B}{B^2R_A}\left(1 - e^{-\frac{BR_At}{C_1C_{issL}R_B}}\right) \tag{19}$$

where $B = C_1 + C_{issL}$, $R_A = R_1 + R_3 + R_4$, $R_B = R_1\ (R_3 + R_4)$. From Equation (19), the v_{gsL} of the $eGaN_L$ increases with the increase in t, when $t \to V_{DC}/a$, v_{gsL} reaches its maximum value v_{gsLm}:

$$v_{gsLm} = -\frac{V_{DC}C_{gdL}}{B} - \frac{aC_1{}^2C_{gdL}R_B}{B^2R_A}\left(1 - e^{-\frac{BR_AV_{DC}}{aC_1C_{issL}R_B}}\right) \tag{20}$$

Figure 7 shows the correlation between resistor R_1 and the peak negative crosstalk voltage v_{gsLm}, from which it can be obtained that the value of v_{gsLm} is positively correlated with R_1. Therefore, the smaller the resistance value of R_1, the better. At the same time, as R_1 decreases, the impedance of the gate driver decreases, increasing the device gate-source oscillation. This results in the positive oscillation being too large and exceeding the device threshold voltage, thereby increasing the risk of device misconduct. The relationship between the device gate-source oscillation and R_1 is shown in Figure 8. Therefore, both factors must be considered when selecting the value of R_1.

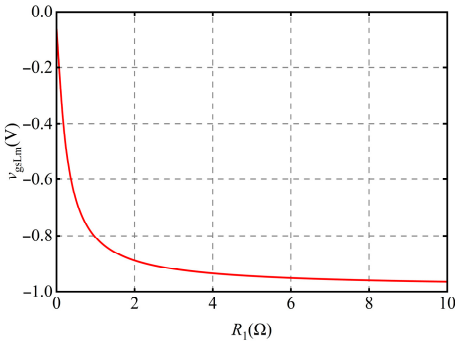


Figure 7. Effect of R_1 on the peak of the negative crosstalk.

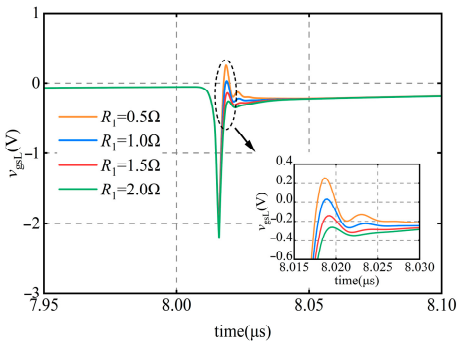


Figure 8. Effect of different R_1 on gate source oscillation.

4.4. Other Component Parameters

For the resistor R_2, which, together with capacitor C_1, determines the discharge rate of C_1, it is also necessary to ensure that capacitor C_1 discharges the stored charge and returns to 0 V at t_3. With the value of capacitor C_1 determined, the following equation can be derived from Equation (11).

$$R_2 = \frac{\Delta T_3}{5C_1} \tag{21}$$

For the voltage regulator diode D_4, its regulated value, V_{D4}, and the forward conduction voltage drop, V_{D3}, of diode D_3, together form the drive voltage, V_{GL}, of the device. Therefore, it can be obtained that:

$$V_{D4} = V_{GL} - V_{D3} \tag{22}$$

For the resistor R_3, it acts as a current-limiting resistor for the voltage regulator diodes D_2 and D_4, ensuring that the voltage regulator diodes can function properly. Therefore, the value of resistor R_3 can be determined by the following equation:

$$R_3 = \frac{V_{ccL} - V_{D2} - V_{D4} - V_{D3}}{I_Z} \tag{23}$$

where V_{D2} and V_{D4} are, respectively, the regulated values of regulator diodes, and I_z is the current of the regulator diode during normal operation.

For the resistor R_4, since it and resistor R_3 together form the drive resistance R_{gL} of the device, it can be obtained that:

$$R_4 = R_{gL} - R_3 \tag{24}$$

For diodes D_1 and D_3, their role is to enable unidirectional current flow in the branch. D_1 is used to prevent current from flowing through resistor R_1 and affecting the turn-on speed when the device is turned on. Diode D_3 is used to prevent capacitor C_1 from discharging rapidly through paths C_1-D_4-D_3-R_3, which affects the effectiveness of the negative voltage suppression and the reduction of positive crosstalk of C_1.

To adapt to the fast-switching characteristics of the eGaN HEMT, Schottky diodes are used for D_1 and D_3. The maximum reverse peak voltages V_{RM1} and V_{RM3} of the two diodes are selected based on the following: for D_1, the maximum reverse voltage is the sum of the device drive voltage V_{GL} and the maximum negative voltage of capacitor C_1,

which is the regulated voltage value V_{D2} of D_2; for D_3, the maximum reverse voltage is the maximum negative voltage of capacitor C_1. The following equation can be derived:

$$\begin{cases} V_{RM1} > V_{GL} + V_{D2} \\ V_{RM3} > V_{D2} \end{cases} \tag{25}$$

For the auxiliary power supply V_{ccL}, in order to make D_2 work normally and the $eGaN_L$ gate to reach the set drive voltage V_{GL}, it is necessary to satisfy the following:

$$V_{ccL} = \beta(V_{GL} + V_{D2}) \tag{26}$$

Considering that there will be some voltage drops inside the driver IC and on resistor R_3 when the device is operating, V_{ccL} needs to be designed with a margin factor β ($\beta > 1$).

5. Experimental Verification

The effect of the proposed gate driver on the suppression of both positive and negative crosstalk, as well as on the switching speed of the device, is tested using a double-pulse test platform. The performance of the proposed gate driver in practical engineering is validated by a synchronous Buck test platform. GS61008P was selected as the test device, which has a rated drain voltage of 100 V, a rated drain current of 90 A, and a total gate charge of 8 nC. To satisfy the test requirements, the oscilloscope is TDS3054C. The voltage and current waveforms are measured using a voltage probe (P6139B) and a current probe (TCPA300).

5.1. Double-Pulse Test

The setup of the double-pulse test platform is shown in Figure 9a, where $eGaN_H$ is an active tube and $eGaN_L$ is a passive tube; V_{DC} is the input power supply, which is 50 V; C_{in} is the DC link capacitor, which is 330 µF; L_D is the load inductance, which is 50 µH.

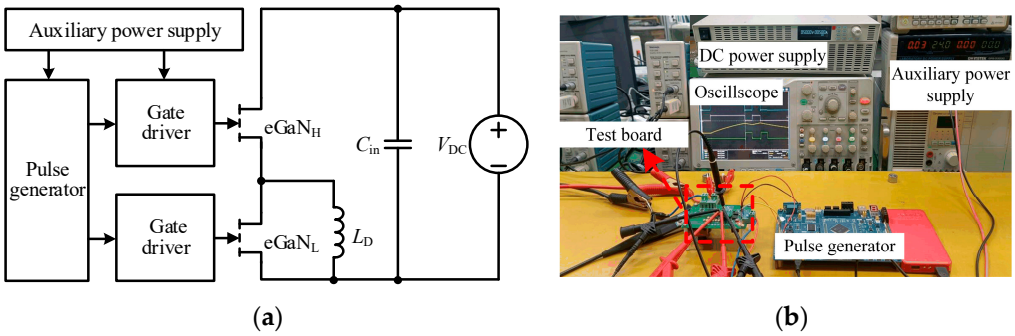


Figure 9. Double-pulse test platform. (**a**) Mechanism diagram; (**b**) experiment platform.

For the regulator diode D_2, the MMSZ5226BT1G with a regulated value of 3.3 V is selected according to Equation (12). For the regulator diode D_4, the MMSZ5232A with a regulated voltage of 5.6 V is selected, as recommended by the datasheet and Equation (22) for a 6 V drive voltage. Considering the reverse voltage stress on the diodes D_1 and D_3, Schottky diodes 1N5818 are selected for D_1 and D_3. According to the technical instruction recommendation, one 10 Ω drive resistor is set after the driver IC of the conventional gate driver for the control group [31]. According to Equations (16)–(24), the value of capacitor C_1 is 6.8 nF, and the values of resistors R_2 to R_4 are 59 Ω, 1 Ω, and 9 Ω, respectively. The supply voltage Vcc_L in the conventional gate driver is set to 6 V. According to Equation (26), the supply voltage Vcc_L in the proposed gate driver is set to 12 V.

During the switching process of the device, due to the interaction between the parasitic inductance and capacitance of the circuit, overshoot and ringing phenomena occur in the

drain-source voltage of the device, increasing the risk of drain-source breakdown and thereby affecting the circuit's safety. In this paper, the method of connecting an RC snubber in parallel with the drain and source of the device is adopted to reduce the ringing. The drain-source waveforms before and after adding the RC snubber are shown in Figure 10. From the results, it is evident that the maximum value of the ring is reduced by 33 V.

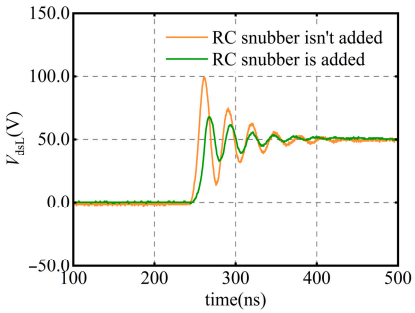


Figure 10. The drain-source waveforms before and after adding the RC snubber.

Figure 11 shows the gate voltage oscillation under different values of R_1 in the experiment. When R_1 is configured to 1 Ω, the positive gate voltage oscillation reaches 1.82 V, which exceeds the device's threshold voltage of 1.7 V. Therefore, the device is at risk of misconduct. To prevent device misconduct and minimize negative crosstalk voltage, the value of R1 is ultimately set to 2 Ω.

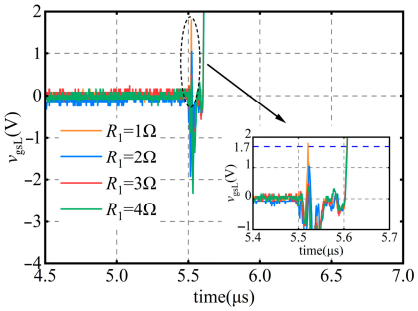
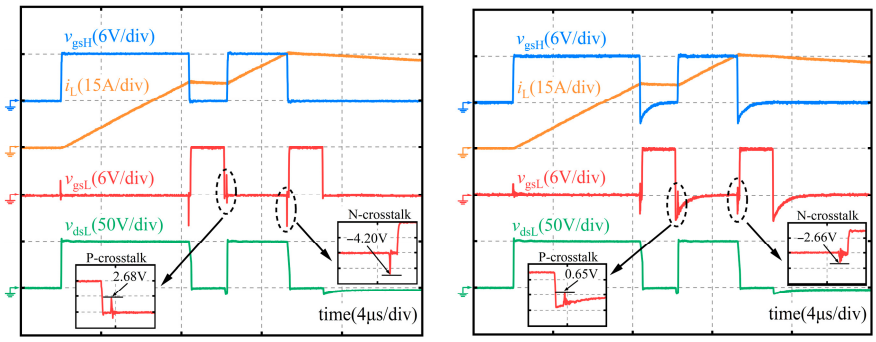


Figure 11. The gate voltage oscillation under different values of R_1.

The double-pulse test results of the devices under the conventional gate driver and the proposed gate driver are shown in Figure 12. A 2.03 V reduction in the positive crosstalk peak is achieved by the proposed gate driver compared to the conventional one, with its positive crosstalk peak falling below the 1.7 V threshold voltage of the GS61008P, thereby reducing the risk of device misconduct. The negative crosstalk spike of the proposed gate driver is reduced by 1.54 V compared to the conventional one, which validates the driver's negative crosstalk suppression capability.

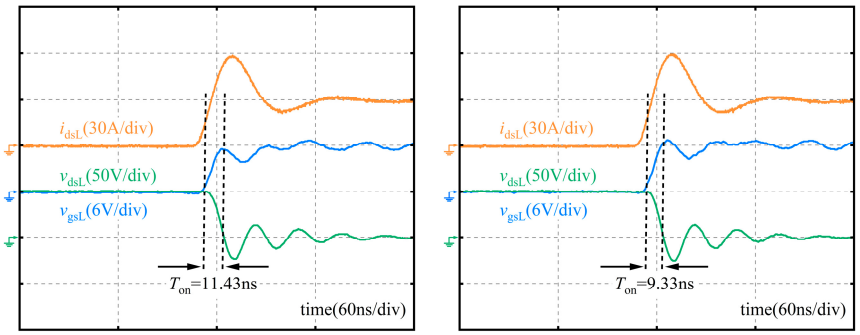
The proposed gate driver is also applicable to other eGaN devices with different gate charges, such as the GS66508P, which has a gate charge of 5.8 nC. Since the GS66508P can operate at higher voltage levels, larger crosstalk spikes may occur. To achieve better suppression, a regulator diode with a higher regulated voltage should be selected for D_2 to provide a larger negative voltage.



(**a**) (**b**)

Figure 12. Double-pulse test results. (**a**) Conventional gate driver; (**b**) proposed gate driver.

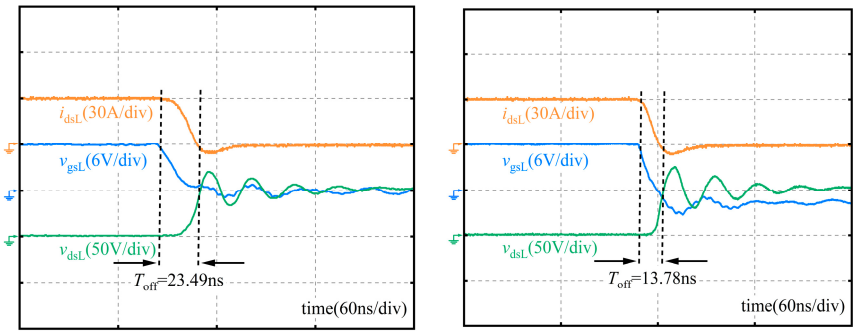
To investigate the effect of the proposed gate driver on the switching performance of the device under test, the switching waveforms of the device are compared under both the conventional gate driver and the proposed gate driver. The turn-on waveforms of the device under these two circuits are shown in Figure 13, from which it can be observed that the turn-on time of the device under the traditional gate driver is 11.43 ns, and the turn-on time under the proposed gate driver is 9.33 ns.



(**a**) (**b**)

Figure 13. The turn-on waveforms. (**a**) Conventional gate driver; (**b**) proposed gate driver.

The turn-off waveforms of the device tested under these two gate drivers are shown in Figure 14, from which it can be seen that the turn-off time is 23.49 ns under the conventional gate driver and 13.78 ns under the proposed one. Under the proposed gate driver's operation, the device's turn-off speed is enhanced by approximately 41.34% compared to the conventional driver, as C1 enables negative-voltage turn-off of the device.



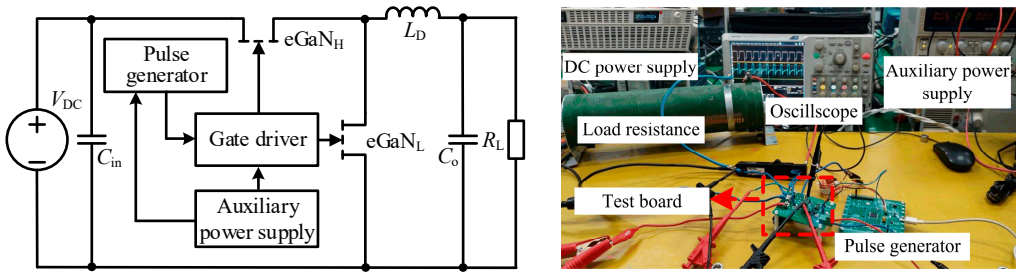
(**a**) (**b**)

Figure 14. The turn-off waveforms. (**a**) Conventional gate driver; (**b**) proposed gate driver.

To investigate the impact of the proposed gate driver on the switching loss of the device, the switching loss of the device is calculated when tested with these two drivers. The turn-on loss is 12.09 μJ and 10.87 μJ in the conventional gate driver and the proposed one, respectively, indicating that the proposed circuit has little impact on the device's turn-on loss; while the turn-off loss is 1.51 μJ and 0.35 μJ, respectively, indicating that the proposed gate driver is capable to significantly reduce the turn-off loss by 76.82%.

5.2. Synchronous Buck Test

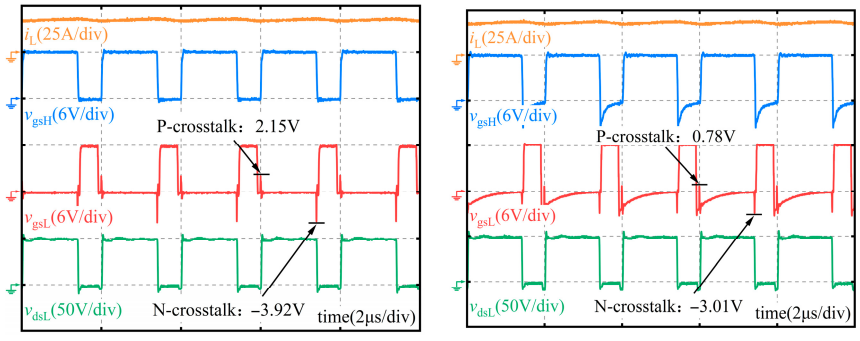
The mechanism of the synchronous Buck test platform is shown in Figure 15a, where $eGaN_H$ is the active tube and $eGaN_L$ is the passive tube; V_{DC} is the input power supply, which is 50 V; C_{in} is DC link capacitor, which is 330 μF; L_D is the load inductance, which is 20 μH; C_o is the output voltage regulator capacitance, which is 150 μF; and R_L is the load resistor, which is 1.8 Ω. The synchronous Buck circuit operates at a 500 kHz frequency in the testing of this experiment.



(**a**) (**b**)

Figure 15. Synchronous Buck test platform. (**a**) Mechanism diagram; (**b**) experiment platform.

The synchronous Buck test results are shown in Figure 16. The positive crosstalk peak value of the proposed gate driver is reduced by 1.37 V compared to the conventional gate driver, and the negative crosstalk peak value is decreased by 0.91 V. Crosstalk suppression capability is more evident in double-pulse tests than in synchronous Buck circuits. However, the result demonstrates that the proposed gate driver presents a positive crosstalk peak value of less than 1.7 V and a negative crosstalk voltage peak value of more than −10 V under both test conditions, which meets the safe operation requirements.



(**a**) (**b**)

Figure 16. Synchronous Buck test results. (**a**) Conventional gate driver; (**b**) proposed gate driver.

6. Discussion

To illustrate the characteristics of the proposed gate driver, this paper compares some typical crosstalk suppression circuits by evaluating them from three perspectives: reducing

device turn-on speed, mitigating negative crosstalk, and increasing control complexity, as shown in Table 1.

Table 1. Comparison of different suppression circuits.

Circuits	Reducing Device Turn-on Speed	Exacerbating Negative Crosstalk	Increasing Control Complexity
In [23]	Yes	Yes	No
In [24]	Yes	No	No
In [27]	No	No	Yes
In [28]	No	Yes	No
In [29]	No	No	Yes
This paper	No	No	No

1. From the perspective of reducing the device turn-on speed, the circuits proposed in [23,24] require charging the auxiliary capacitor placed in parallel with the gate, which in turn reduces the device turn-on speed. The circuits proposed in [27–29] do not have auxiliary capacitors in parallel, which does not affect the device turn-on speed. In this paper, the structure without an auxiliary capacitor in parallel is also employed, and its effect on the device's turn-on speed is negligible.
2. From the perspective of exacerbating negative crosstalk, the circuits proposed in [23,28] do not provide an effective discharge path for the negative voltage capacitor, which will exacerbate the gate negative crosstalk and increase the risk of gate reverse breakdown. The circuit proposed in [29] uses an auxiliary MOSFET to clamp the negative voltage without exacerbating the negative crosstalk. The circuits proposed in [27] provide a discharge path for the negative voltage capacitor, allowing for negative voltage recovery without affecting gate-to-negative crosstalk. In this paper, this idea is also adopted to avoid exacerbating the gate negative crosstalk.
3. From the perspective of increasing control complexity, the circuits proposed in [27,29] require the introduction of MOSFET, which increases the control complexity. In contrast, the circuits proposed in this paper and the other literature do not require additional control, which improves the ease of application.

7. Conclusions

This paper provides a brief analysis of the crosstalk problem in the half-bridge circuit. It proposes a gate driver that suppresses both positive and negative crosstalk, addressing the limitations of existing crosstalk suppression circuits that require additional control signals or exacerbate negative crosstalk. Double-pulse experiments are conducted to validate the crosstalk suppression capability of the proposed gate driver, which achieves shorter device turn-off time and lower loss compared to the conventional driver. By building a synchronous Buck circuit, the practical value of the proposed circuit is validated in real working conditions, which provides a basis for further improvement in the gate driver.

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References

1. Khadar, R.A.; Liu, C.; Soleimanzadeh, R.; Matioli, E. Fully Vertical GaN-on-Si power MOSFETs. *IEEE Electron. Device Lett.* **2019**, *40*, 443–446. [CrossRef]
2. Wang, K.; Zhu, Y.; Zhao, H.; Zhao, R.; Zhu, B. Steady-State Temperature-Sensitive Electrical Parameters' Characteristics of GaN HEMT Power Devices. *Electronics* **2024**, *13*, 363. [CrossRef]
3. Manandhar, M.B.; Matin, M.A. Comparative Modelling and Thermal Analysis of AlGaN/GaN Power Devices. *J. Low Power Electron. Appl.* **2021**, *11*, 33. [CrossRef]
4. Yang, Y.; Zhu, B.; She, X.; Wang, K.; Liu, A. A Family of Bipolar DC–DC Converters With Interpolar Voltage Self-Balancing Based on FB-BVMs for BLVDC Microgrid. *IEEE Trans. Ind. Electron.* **2025**. [CrossRef]
5. Faraji, R.; Farzanehfard, H.; Kampitsis, G.; Mattavelli, M.; Matioli, E.; Esteki, M. Fully Soft-Switched High Step-Up Nonisolated Three-Port DC–DC Converter Using GaN HEMTs. *IEEE Trans. Ind. Electron.* **2020**, *67*, 8371–8380. [CrossRef]
6. Wen, H.; Gong, J.; Zhao, X.; Yeh, C.S.; Lai, J.S. Analysis of Diode Reverse Recovery Effect on ZVS Condition for GaN-Based LLC Resonant Converter. *IEEE Trans. Power Electron.* **2019**, *34*, 11952–11963. [CrossRef]
7. Murukesan, K.; Efthymiou, L.; Udrea, F. On the challenges of reliable threshold voltage measurement in ohmic and schottky gate p-GaN HEMTs. *IEEE J. Electron. Devices Soc.* **2021**, *9*, 831–838. [CrossRef]
8. Avraham, T.; Dhyani, M.; Bernstein, J.B. Reliability Challenges, Models, and Physics of Silicon Carbide and Gallium Nitride Power Devices. *Energies* **2025**, *18*, 1046. [CrossRef]
9. Yang, Y.; Zhu, B.; She, X.; Wang, K.; Liu, A. A Family of Voltage Balancers with Fault-Tolerance and Interpolar Voltage Self-Balancing Ability for Bipolar DC Power Systems. *IEEE Trans. Transp. Electrif.* **2025**. [CrossRef]
10. Chen, J.; Luo, Q.; Huang, J.; He, Q.; Du, X. A Complete Switching Analytical Model of Low-Voltage eGaN HEMTs and Its Application in Loss Analysis. *IEEE Trans. Ind. Electron.* **2020**, *67*, 1615–1625. [CrossRef]
11. Xie, R.; Yang, X.; Xu, G.; Wei, J.; Wang, Y.; Wang, H.; Tian, M.; Zhang, F.; Chen, W.; Wang, L.; et al. Switching transient analysis for normally-off GaN transistor with p-GaN gate in a phase-leg circuit. *IEEE Trans. Power Electron.* **2019**, *34*, 3711–3728. [CrossRef]
12. Zhang, W.; Wang, F.; Costinett, D.J.; Tolbert, L.M.; Blalock, B.J. Investigation of gallium nitride devices in high-frequency LLC resonant converters. *IEEE Trans. Power Electron.* **2017**, *32*, 571–583. [CrossRef]
13. Wang, X.; Zhao, Q.; Zhao, Z.; Meng, F. Full-Bridge DC-DC Converter with Synchronous Rectification Based on GaN Transistors. *J. Low Power Electron. Appl.* **2025**, *15*, 25. [CrossRef]
14. Belkacemi, K.; Hocine, R. Efficient 3D-TLM Modeling and Simulation for the Thermal Management of Microwave AlGaN/GaN HEMT Used in High Power Amplifiers SSPA. *J. Low Power Electron. Appl.* **2018**, *8*, 23. [CrossRef]
15. Xie, R.; Wang, H.; Tang, G.; Yang, X.; Chen, K.J. An Analytical Model for False Turn-On Evaluation of High-Voltage Enhancement-Mode GaN Transistor in Bridge-Leg Configuration. *IEEE Trans. Power Electron.* **2017**, *32*, 6416–6433. [CrossRef]
16. Riazmontazer, H.; Rahnamaee, A.; Mojab, A.; Mehrnami, S.; Mazumder, S.K.; Zefran, M. Closed-loop control of switching transition of SiC MOSFETs. In Proceedings of the 2015 IEEE Applied Power Electronics Conference and Exposition (APEC), Charlotte, NC, USA, 15–19 March 2015; pp. 782–788.
17. Zushi, Y.; Sato, S.; Matsui, K.; Murakami, Y.; Tanimoto, S. A novel gate assist circuit for quick and stable driving of SiC-JFETs in a 3-phase inverter. In Proceedings of the 2012 Twenty-Seventh Annual IEEE Applied Power Electronics Conference and Exposition (APEC), Orlando, FL, USA, 5–9 February 2012; pp. 1734–1739.
18. Huang, X.; Liu, Z.; Lee, F.C.; Li, Q. Characterization and Enhancement of High-Voltage Cascode GaN Devices. *IEEE Trans. Electron Devices* **2015**, *62*, 270–277. [CrossRef]
19. Hu, K.; Yang, M.; Zhang, X. A Multilevel Self-Driving Gate Driver of SiC MOSFET for Crosstalk Suppression Considering Common-Source Inductance. *IEEE Trans. Power Electron.* **2025**, *40*, 906–919. [CrossRef]
20. Zhang, B.; Wang, S. A crosstalk suppression technique for SiC MOSFETs in the bridge-leg configuration. In Proceedings of the 2020 IEEE Applied Power Electronics Conference and Exposition (APEC), New Orleans, LA, USA, 15–19 March 2020; pp. 1513–1520.
21. Zhang, Z.; Dix, J.; Wang, F.F.; Blalock, B.J.; Costinett, D.; Tolbert, L.M. Intelligent Gate Drive for Fast Switching and Crosstalk Suppression of SiC Devices. *IEEE Trans. Power Electron.* **2017**, *32*, 9319–9332. [CrossRef]
22. Zhang, Z.; Wang, F.; Tolbert, L.M.; Blalock, B.J. Active Gate Driver for Crosstalk Suppression of SiC Devices in a Phase-Leg Configuration. *IEEE Trans. Power Electron.* **2014**, *29*, 1986–1997. [CrossRef]
23. Wang, J.; Chung, H.S.H. A novel RCD level shifter for elimination of spurious turn-on in the bridge-Leg configuration. *IEEE Trans. Power Electron.* **2015**, *30*, 976–984. [CrossRef]

24. Li, B.; Zhang, G.; Li, C.; Wang, G.; Liu, S.; Xu, D. Crosstalk suppression method for GaN-based bridge configuration using negative voltage self-recovery gate drive. *IEEE Trans. Power Electron.* **2022**, *37*, 4406–4418. [CrossRef]
25. Lu, Z.; Li, C.; Wu, H.; Li, W.; He, X.; Li, S. Design of Active SiC MOSFET Gate Driver for Crosstalk Suppression Considering Impedance Coordination between Gate Loop and Power Loop. In Proceedings of the 2019 IEEE Applied Power Electronics Conference and Exposition (APEC), Anaheim, CA, USA, 17–21 March 2019; pp. 986–990.
26. Liu, C.; Zhang, Z.; Liu, Y.; Si, Y.; Lei, Q. Smart Self-Driving Multilevel Gate Driver for Fast Switching and Crosstalk Suppression of SiC MOSFETs. *IEEE J. Emerg. Sel. Top. Power Electron.* **2020**, *8*, 442–453. [CrossRef]
27. Wu, X.; Zaman, H.; Wu, P.; Jia, R.; Zhao, X.; Wu, X. A Quasi-Multilevel Gate Driver for Fast Switching and Crosstalk Suppression of SiC Devices. *IEEE Access* **2020**, *8*, 191403–191412. [CrossRef]
28. Zaman, H.; Wu, X.; Zheng, X.; Khan, S.; Ali, H. Suppression of switching crosstalk and voltage oscillations in a SiC MOSFET based half-bridge converter. *Energies* **2018**, *11*, 3111. [CrossRef]
29. Qiu, Z.; Li, H.; Jiang, Y.; Shao, T.; Yang, Z.; Wang, J.; Zhang, Z. An Intelligent Three-level Active Gate Driver for Crosstalk Suppression of SiC MOSFET. In Proceedings of the 2020 IEEE Energy Conversion Congress and Exposition (ECCE), Detroit, MI, USA, 11–15 October 2020; pp. 203–208.
30. Jafari, A.; Nikoo, M.S.; Perera, N.; Karakaya, F.; Soleimanzadeh, R.; Matioli, E. Small-signal approach for precise evaluation of gate losses in soft-switched wide-band-gap transistors. In Proceedings of the 2020 IEEE 21st Workshop on Control and Modeling for Power Electronics (COMPEL), Aalborg, Denmark, 9–12 November 2020; pp. 1–5.
31. GAN, S. Gate Driver Circuit Design with GaN E-HEMTs. 2022. Available online: https://gansystems.com/wp-content/uploads/2022/03/GN012_Gate-Driver-Design-with-GaN-E-HEMTs_220308.pdf (accessed on 1 March 2024).