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A 0.8 V Low-Power Wide-Tuning-Range CMOS VCO for 802.11ac and IoT C-Band Applications

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Abstract: This paper presents a 0.8 V low-power CMOS voltage-controlled oscillator (VCO) with a wide tuning range, fabricated using a TSMC 0.18 μm process. The proposed design incorporates body-biasing techniques and an optimized varactor structure to achieve a tuning range of 1124 MHz (5.829–4.705 GHz) and low phase noise of −117.6 dBc/Hz at a 1 MHz offset. Operating at an ultra-low supply voltage of 0.8 V, the VCO consumes only 3.4 mW, demonstrating excellent power efficiency. A buffer circuit is also employed to enhance output symmetry and suppress flicker noise without introducing additional control complexity. With a figure-of-merit (FOM) of −188.6 dBc/Hz and a wide tuning range of 22.2%, the proposed VCO is well-suited for modern low-power communication systems, including 802.11ac, 5G transceivers, satellite links, and compact IoT devices.

Keywords: VCO; tuning range; phase noise; low-power design; C-band; body-bias technique; CMOS RF circuits; IoT applications

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1. Introduction

In modern wireless and optical communication systems, efficient voltage-controlled oscillators (VCOs) play a critical role in signal generation. CMOS VCOs have been widely utilized due to their cost-effectiveness and compatibility with System-on-Chip (SoC) integration. However, achieving a wide tuning range and low power consumption while maintaining low phase noise remains a challenge in traditional designs.

Previous research has extensively investigated the fundamental limitations of phase noise and power efficiency in CMOS VCO designs [1–4]. Several techniques have been proposed to optimize phase noise performance, including approaches aimed at minimizing flicker noise and enhancing the tuning range [4–7]. More recent studies have introduced advanced techniques such as switched biasing and resistive tuning to achieve low-power operation and wide frequency tunability. However, these techniques generally suffer from increased design complexity, limited reduction in power consumption, or constrained frequency tuning ranges. Therefore, designing a VCO that simultaneously achieves ultra-low power consumption, low phase noise, wide tuning range, and simplified circuit architecture remains a significant challenge and warrants further exploration.

This work presents a novel CMOS VCO that employs body-bias technology and an optimized buffer circuit to significantly extend the tuning range and enhance power efficiency. Operating at an ultra-low voltage of 0.8 V, the proposed design demonstrates substantially reduced power consumption compared to conventional designs typically requiring supply voltages of 1.2 V or higher. The design achieves a wide tuning range

of 1124 MHz and maintains excellent phase noise performance, making it an attractive solution for 5G, satellite communications, and optical networking applications.

2. VCO Architecture

2.1. Phase Noise

In addition to the noise generated by the circuits, noise from the power supply also affects phase noise [8–10]. Using the transistor as the tail current source can decrease the noise from the power supply to the VCO. For PMOS-only VCO, the active region provides the VCO with better protection against noise from the power supply [11]. The mechanism of phase noise generation through bias noise conversion is illustrated in Figure 1.

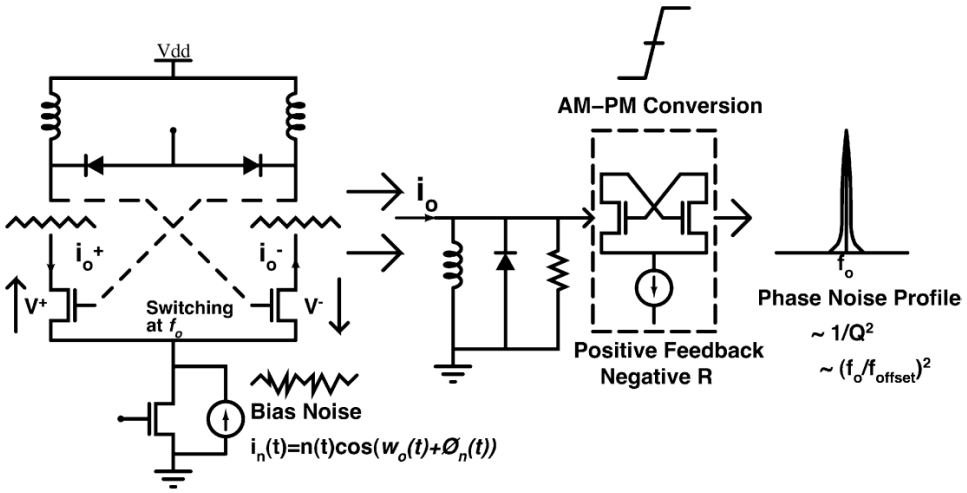


Figure 1. Conversion of bias noise into phase noise.

It must be noted that the phase noise improves as quality factor Q increases. The Q of standard inductor L1 is around 8.62, and the Q value of the center-tapped inductor L3 is around 5.39. The LC-tank quality factor (Q) is about 7.9, and the impedance at the resonance frequency is approximately 0.75 Ω, as shown in Figure 2.

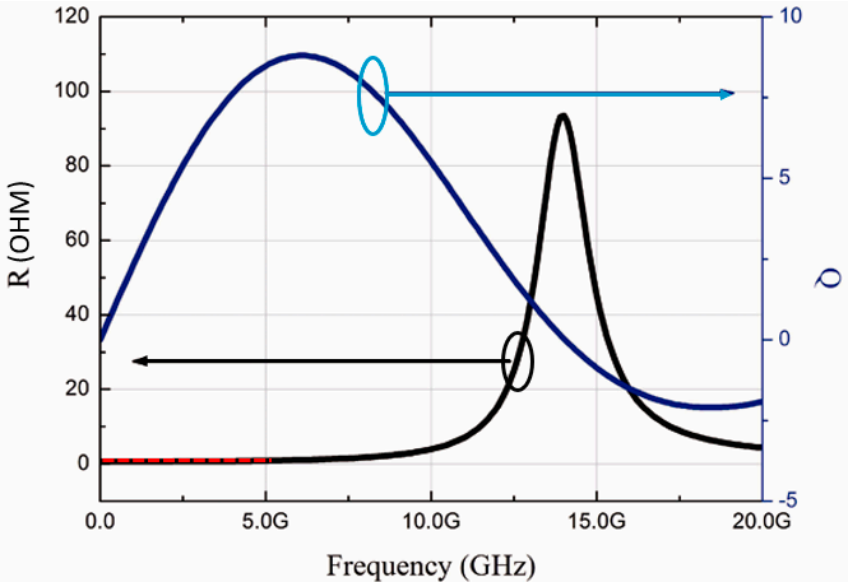


Figure 2. Simulated impedance and quality factor versus frequency characteristics in the LC tank. R and Q are plotted with respect to frequency in GHz.

The phase noise behavior is further analyzed using Leeson's model, which relates phase noise to offset frequency, power consumption, and the LC-tank quality factor. The simplified form is as follows:

$$L(\Delta f) = 10 \cdot log\left[\frac{F \cdot k \cdot T}{2 \cdot P_{DC}} \cdot \left(\frac{f_0}{\Delta f \cdot Q}\right)^2\right] \quad (1)$$

where F is the noise factor (~2–3), k is Boltzmann's constant, T is the absolute temperature (300 K), P_{DC} is the DC power consumption, f_0 is the oscillation frequency, Δf is the offset frequency, and Q is the quality factor of the LC tank. Based on post-layout simulation, with P_{DC} = 3.4 mW, Q = 10.5, and f_0 = 5.06 GHz, the estimated phase noise at 1 MHz offset is approximately −117.6 dBc/Hz, which matches well with the measured results. This confirms the theoretical basis of our design approach.

2.2. Buffer Circuit and Optimization

The cross-coupled pair is used to suppress parasitic effects introduced by the transistors. It can increase the ratio of tuning capacitance (C_v) and parasitic capacitance ($C_{parasitic}$). A high $C_v/C_{parasitic}$ ratio can achieve a wider frequency tuning range. The PMOS varactor C_v value at different control voltages is shown in Figure 3. Figure 3 shows a good C_{max}/C_{min} ratio of about 2.78, which can be achieved when using 0.18 μm bulk CMOS technology with a tuning voltage ±2 V.

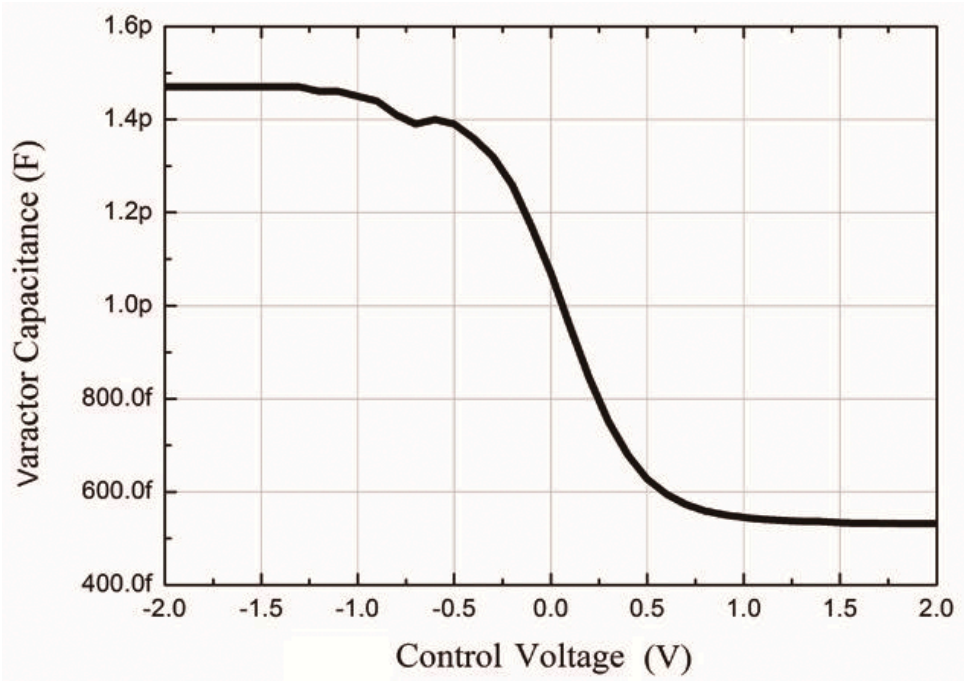


Figure 3. Simulation C-V curve of the PMOS varactor.

The varactor is designed using PMOS devices operated in the accumulation–depletion mode. By tuning the gate and body voltages, the capacitance is adjusted across the intended voltage swing.

To analyze the impact of this ratio, we conducted a series of simulations by sweeping C_{max}/C_{min} values from 2.0 to 3.5. The results show that increasing this ratio can broaden the frequency tuning range but tends to reduce linearity and Q-factor. Through optimization, a C_{max}/C_{min} of 2.78 was selected as the optimal trade-off, providing sufficient tunability while maintaining acceptable phase noise and output symmetry.

The oscillator frequency can be determined with Equation (2).

$$f_{OSC} = \left(2\pi\sqrt{L(C_{ind} + C_v + C_{MOS})}\right)^{-1} \quad (2)$$

where C_{ind} is the equivalent parallel capacitance of the inductor, C_v is the equivalent capacitance of one varactor, and C_{MOS} is the equivalent parallel capacitance of the NMOS crossed-coupled transistor.

The proposed VCO is based on a negative resistance LC-tank topology with a cross-coupled NMOS pair as the core active components. The complete schematic is depicted in Figure 4. The tuning mechanism utilizes a pair of varactors (C_1, C_2), controlled by the tuning voltage (V_t), enabling frequency adjustment between 5.829 GHz and 4.705 GHz.

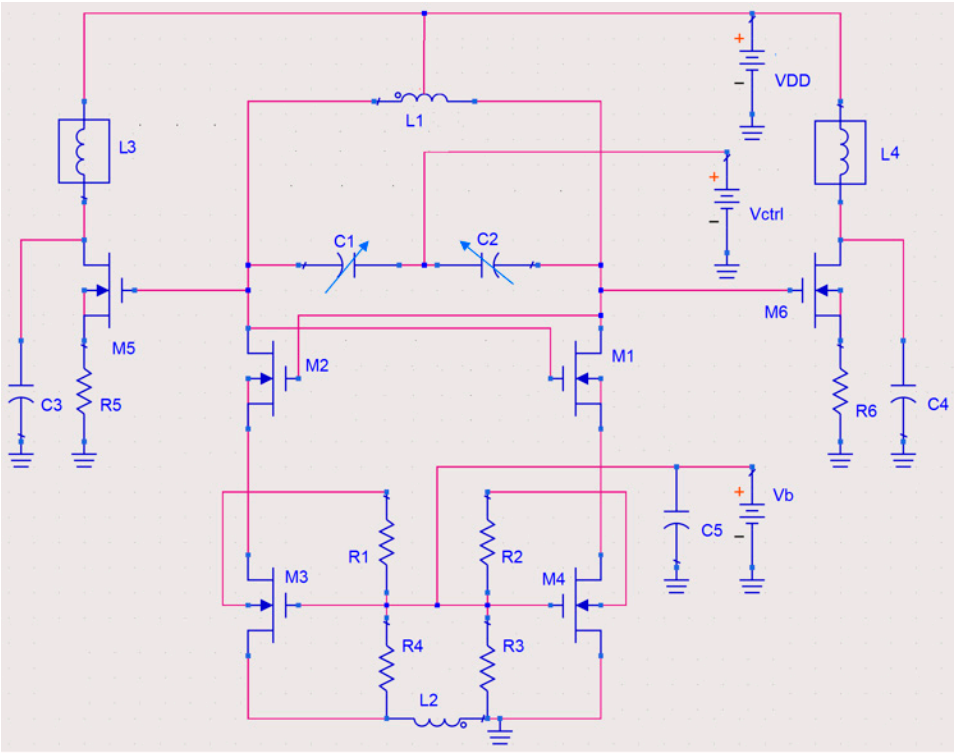


Figure 4. Schematic of the proposed CMOS voltage-controlled oscillator (VCO). This diagram illustrates the complete circuit topology, including the cross-coupled NMOS pair, varactors, biasing network, and buffer stages. Passive component values (L, C, R) are process-optimized and discussed in Section 3.1.

To achieve low power consumption, the circuit operates at a reduced supply voltage of 0.8V. A body-biasing technique is applied to transistors M_3 and M_4, lowering the threshold voltage and enabling operation with minimal power dissipation. This results in a measured power consumption of 3.4 mW. For phase noise optimization, a buffer stage comprising transistors M_5 and M_6, and inductors L_3 and L_4 is included to enhance the output signal swing and minimize phase noise degradation.

Although switched-biasing techniques effectively reduce flicker noise, they typically require additional control circuits, which increase design complexity and power consumption. Instead, our approach utilizes a carefully designed buffer circuit to achieve a comparable improvement in phase noise while maintaining ultra-low power consumption. The measured phase noise at 1 MHz offset is −117.6 dBc/Hz. The buffer circuit also improves waveform symmetry, reducing flicker noise contributions and enhancing overall signal integrity.

Jitter simulation was not performed in this work; however, transient simulations confirmed improved waveform symmetry and reduced distortion.

3. Simulation and Measurement Results

This section presents the performance evaluation of the proposed VCO based on both post-layout simulations and measurement results. The results are categorized into key performance metrics, including frequency tuning range, phase noise, power consumption, and spectral purity. Each metric is discussed with corresponding figures and tables to provide a comprehensive validation of the design.

3.1. Simulation Results

Design process:

1. First, the application specifications must be developed.
2. The design is to be simulated using ADS software (Advanced Design System, Keysight Technologies, version 2019) to determine if the specifications can be met by the circuit architecture.
3. The layout is designed using the Virtuoso layout editor. The caliber is used for the verification of DRC and LVS.
4. The layout file is reloaded into ADS. It is recommended that an EM simulation is performed using ADS. This is to extract whether the circuit conforms to the specification after realization.

Figure 5 shows the simulated phase noise of the VCO, which achieves −116.5 dBc/Hz at a 1 MHz offset, confirming low-noise operation. Figure 6 illustrates the frequency tuning curve versus control voltage, demonstrating a tuning range from 5.8 GHz to 4.5 GHz as Vctrl sweeps from 0 to 1.2 V.

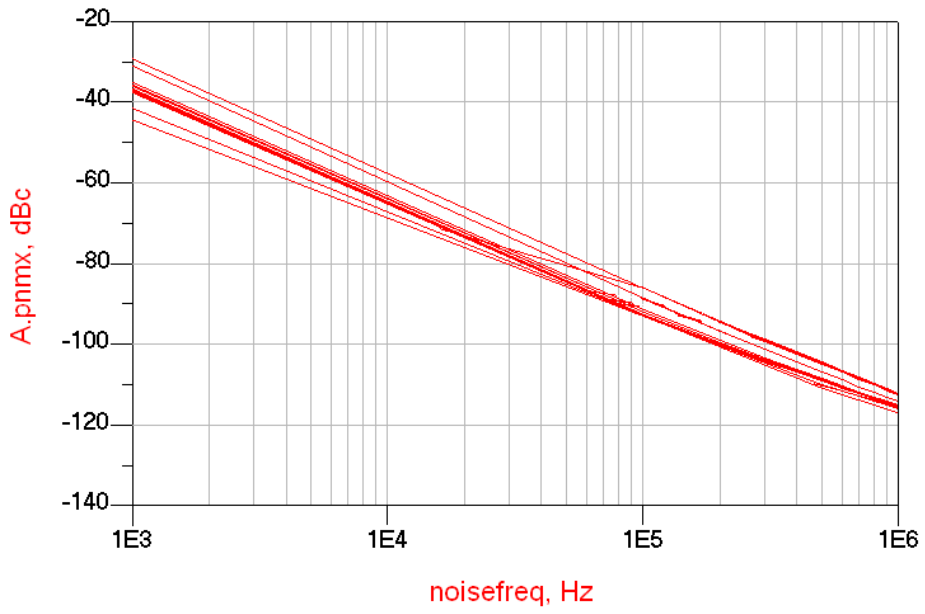


Figure 5. Simulation result of the phase noise.

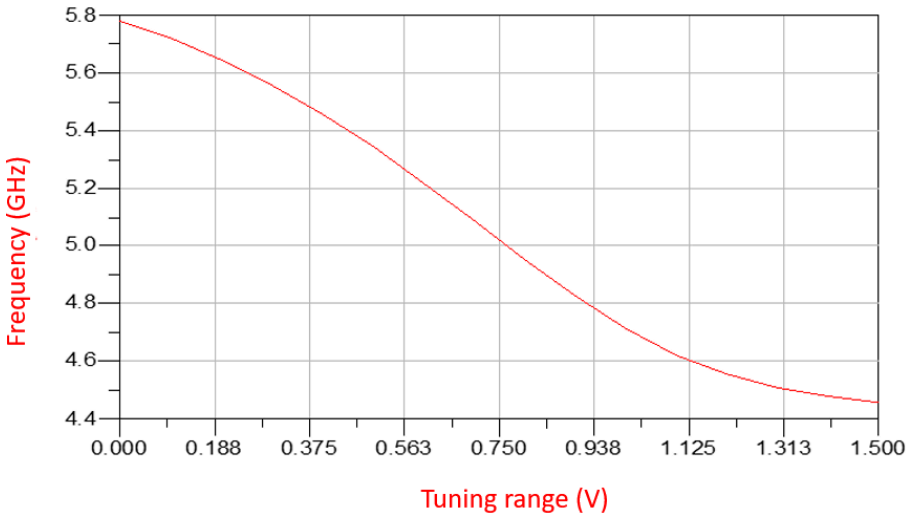


Figure 6. Simulated tuning range of the VCO.

3.2. Measurement Results

The VCO circuit is designed and fabricated in TSMC's 0.18-μm CMOS process. The process offers six metal layers for interconnection, and various kinds of RF inductors and varactors. The physical dimension of the low-phase-noise VCO chip is 0.499 mm^2 including pads. Figure 7 presents the microphotograph of the fabricated VCO chip, with a total area of 0.499 mm^2 including I/O pads. The measured tuning range is 1124 MHz for the control voltage in the range of 0~1.3 V. The measured tuning curve is shown in Figure 8, confirming a 1124 MHz tuning range (22.2%) with the control voltage increasing from 0 to 1.3 V. Figure 9 presents the measured phase noise at 5.065 GHz, achieving −117.69 dBc/Hz at a 1 MHz offset, which is consistent with the simulation results. The phase noise at the offset frequencies of 1 MHz is −117.69 dBc/Hz. The output spectrum at 5.06 GHz is shown in Figure 10, exhibiting a clean tone with −22.44 dBm output power and well-suppressed harmonics. The FOM value is about −196.6 dBc/Hz and it is calculated using the FOM, which is defined as follows [12].

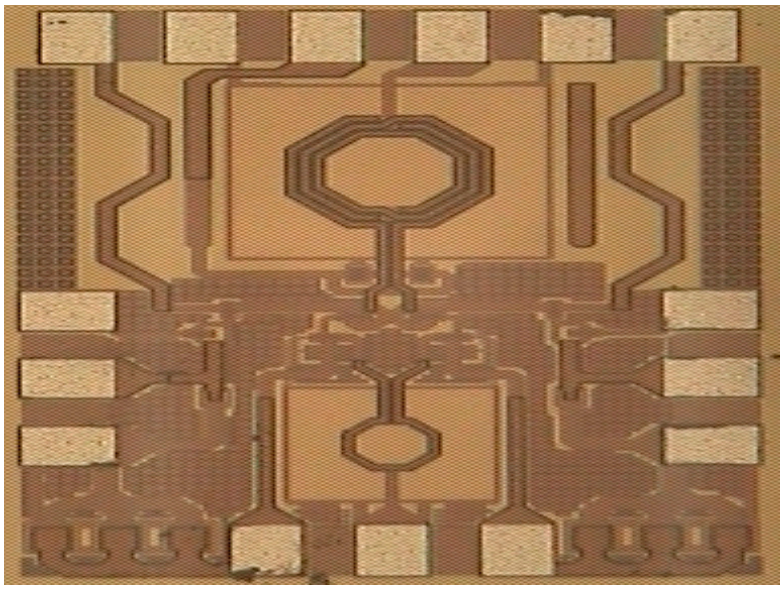


Figure 7. The photograph of the fabricated VCO chip (size: 0.499 mm^2).

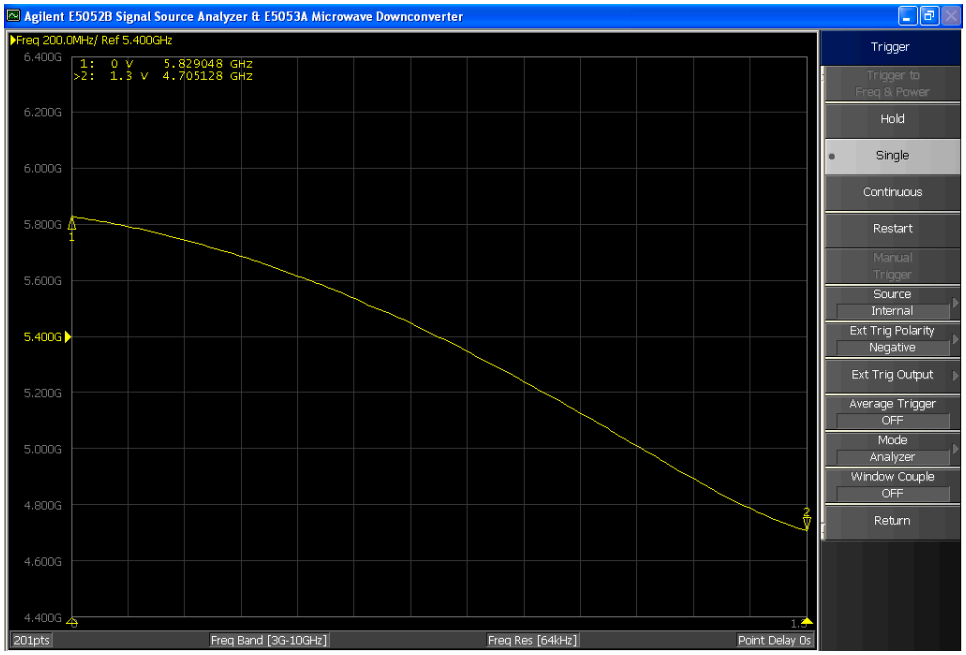


Figure 8. Measured tuning curve of the VCO.

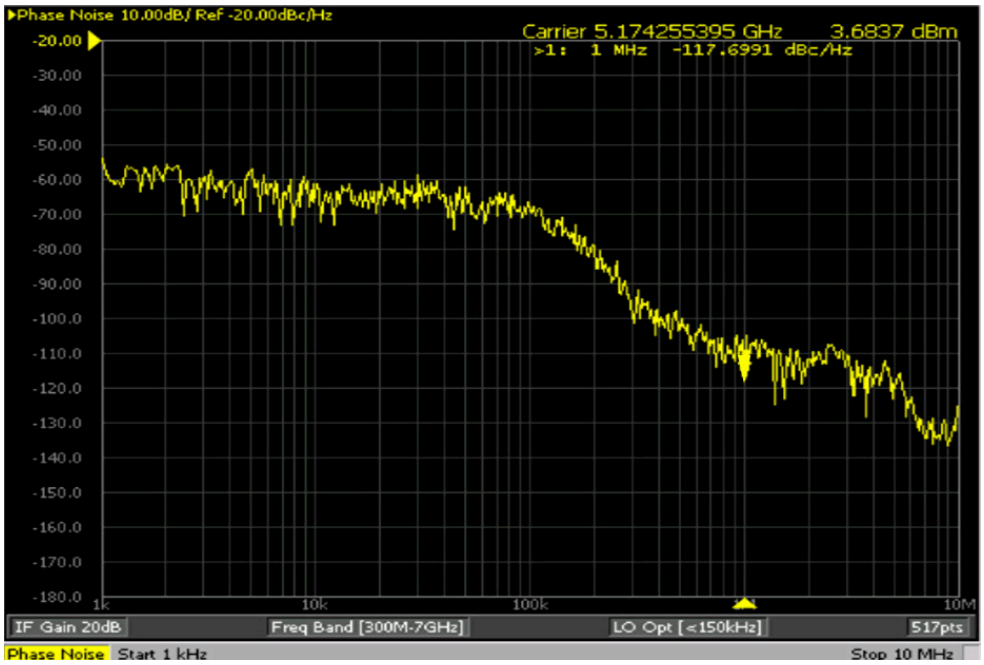


Figure 9. Measured phase noise at 1 MHz offset showing −117.69 dBc/Hz performance.

The figure-of-merit (FOM) and the power–frequency–tuning-normalized (PFTN) metrics are used to evaluate oscillator performance and compare across designs. The FOM definition is based on the classical phase noise model proposed by Leeson [7] and refined by Hajimiri and Lee [8,9], which quantifies the trade-off among phase noise, power consumption, and frequency offset. The PFTN metric further considers the tuning range as proposed in [12,13].

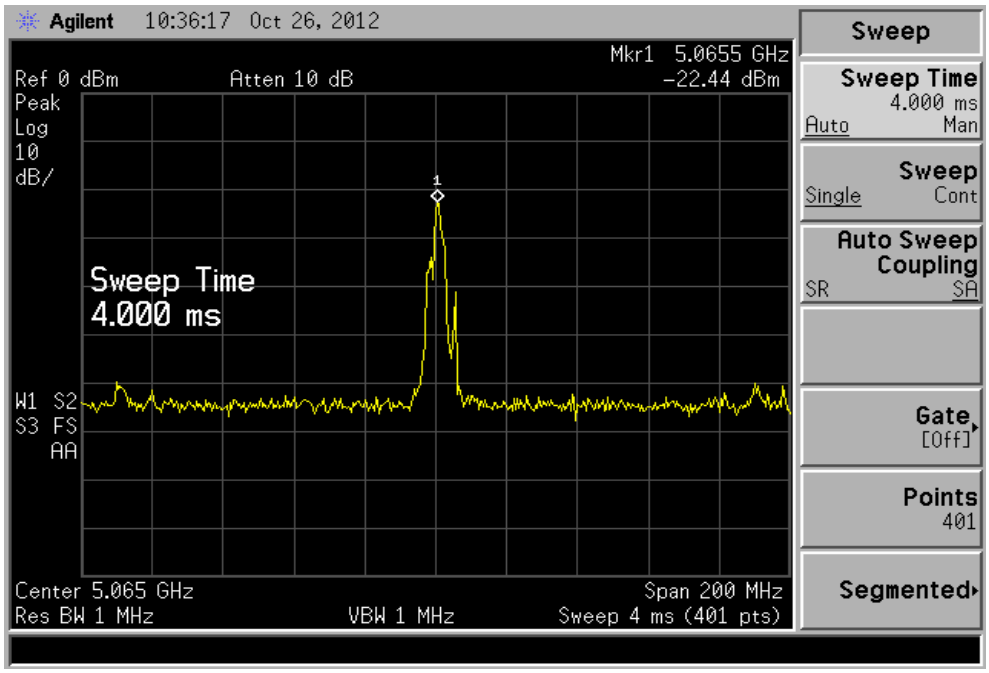


Figure 10. Measured spectrum of the VCO at 5.065-GHz.

The equations are given as follows:

$$FOM = L\{\Delta\omega\} + 10 \cdot \log(P_{DC}) - 20 \cdot \log\left(\frac{\omega_0}{\Delta\omega}\right) \quad (3)$$

ω_0 is the oscillation frequency (MHz), $L\{\Delta\omega\}$ is the measured phase noise at offset frequency Δ (Hz), and P_{DC} is the DC power consumption in mW. The power–frequency–tuning-normalized (PFTN) factor of the proposed VCO is calculated as follows [14]:

$$PFTN = 10 \cdot log\left[\left(\frac{TR}{f_{offset}}\right)^2 \cdot \frac{kT}{P_{DC}}\right] - L\left\{f_{offset}\right\} \quad (4)$$

where

- $L(\Delta f)$ is the phase noise at offset Δf.
- f_0 is the oscillation frequency (in Hz).
- P_{DC} is the power consumption (in mW).
- TR is the tuning range (%).
- T is temperature (in Kelvin), which is taken as 300 K in this work.
- TR is the tuning range and k is Boltzmann's constant. A temperature of 300 K is used for the PFTN calculation.

Table 1 summarizes the comparison between post-layout simulation and measurement results. The performance metrics including frequency, phase noise, FOM, and power consumption show close agreement, validating the design accuracy. A comparison with other recently reported VCOs is provided in Table 2, highlighting differences in frequency, tuning range, power, phase noise, and FOM. The proposed VCO achieves the widest tuning range and lowest power among all, making it well-suited for low-power communication applications. Most studies use CMOS technology with 0.18 µm, except for [15], which uses 0.13 µm. All designs operate around 5 GHz, with a frequency range of 5.0 to 5.3 GHz. Although our result has slightly worse phase noise performance (−117.7 dBc/Hz) than other studies, it achieves the widest tuning range (22.2%) and the lowest power consump-

tion (3.4 mW) while maintaining a competitive FOM. These characteristics are ideal for low-power wireless communication applications.

Table 1. Comparison between post-simulation and measured results of the proposed VCO.

	Post-Simulation	Measurement
Frequency (GHz)	5	5.06
Tuning Range (MHz)	1324	1124
Phase Noise (dBc/Hz)	−116.5	−117.69
FOM (dBc/Hz @ MHz)	−181.4	−196.6
Output Power (dBm)	−4.6	−22.44
Power Consumption (mW)	8.1	3.4
Chip Size (mm^2)	0.499	

Table 2. Performance comparison with other reported VCOs.

Ref.	CMOS Tech. (μm)	Frequency (GHz)	Phase Noise, dBc/Hz @ 1 MHz	Tuning Range (%)	FOM (dBc/Hz)	P_{DC} (mW)	PFTN (dB)
[11]	0.18	5.3	−124	8	−190	13.5	−9.09
[14]	0.18	5	−122.7	6.4	−189.3	5.28	−8.25
[15]	0.13	5	−121	20	−189	4.2	N/A
[16]	0.18	5.2	−113.7	9.56	−180	9.7	N/A
This work	0.18	5.06	−117.7	22.2	−188.6	3.4	−4.3

To validate the VCO's performance under realistic measurement conditions, on-wafer testing was performed using a microwave probe station. The setup included a six-pin DC header for supplying bias voltages and a three 3-pin DC header for control tuning. The RF input/output was accessed via two separate three 3-pin headers. The VCO consumed 4.25 mA under a 0.8 V supply, resulting in a total power consumption of 3.4 mW.

Output frequency and output power were measured using a Keysight E5052B signal source analyzer (Keysight Technologies, Santa Rosa, CA, USA). Phase noise measurements were conducted with a Keysight E5052B signal source analyzer in combination with an E5053A microwave downconverter (Keysight Technologies, Santa Rosa, CA, USA). Figure 11 illustrates both measurement setups and their corresponding equipment configurations. No external bandpass or harmonic filtering was applied during the output measurement; the results represent the direct output spectrum of the VCO.

A photo of the actual on-wafer measurement setup is provided in Figure 12.

As summarized in Table 2, although the proposed VCO has slightly higher phase noise (−117.7 dBc/Hz @ 1 MHz offset) than some recent works, it offers the widest tuning range (22.2%) and the lowest power consumption (3.4 mW) among all the listed designs.

In practical wireless applications such as 802.11ac and low-power IoT devices, energy efficiency and integration flexibility often take precedence over the optimal phase noise. A 2–3 dB phase noise difference has minimal effect on system performance in these use cases.

Furthermore, the achieved figure-of-merit (−188.6 dBc/Hz) and PFTN (−4.3 dB) metrics confirm the superior power–performance efficiency of the proposed design. These attributes make it a strong candidate for modern low-power transceivers where tuning range, power budget, and integration readiness are critical.

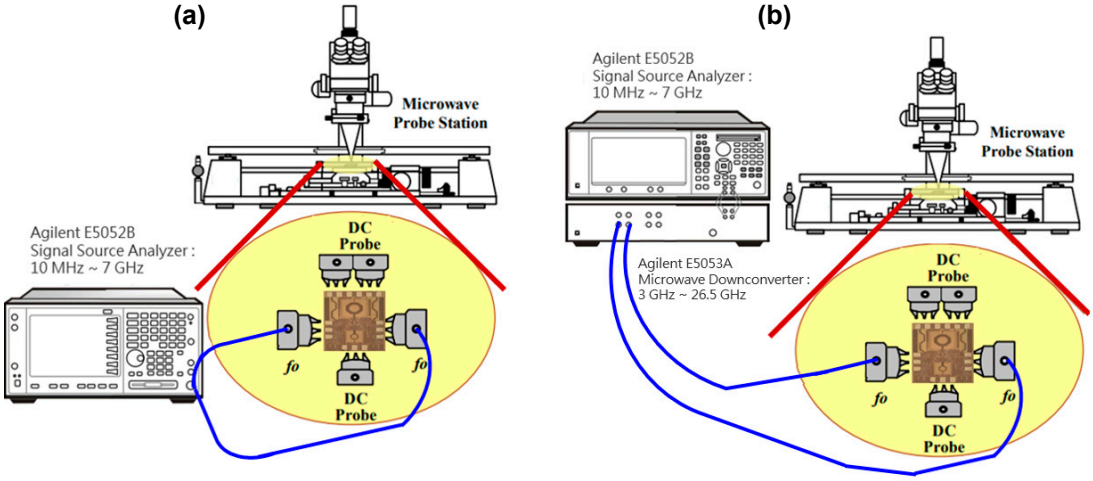


Figure 11. (**a**) Output frequency and power measurement setup using the Keysight E5052B signal source analyzer (Keysight Technologies, Santa Rosa, CA, USA). (**b**) Phase noise measurement setup using the Keysight E5052B and E5053A microwave downconverter (Keysight Technologies, Santa Rosa, CA, USA), conducted via on-wafer probing with RF probe station.

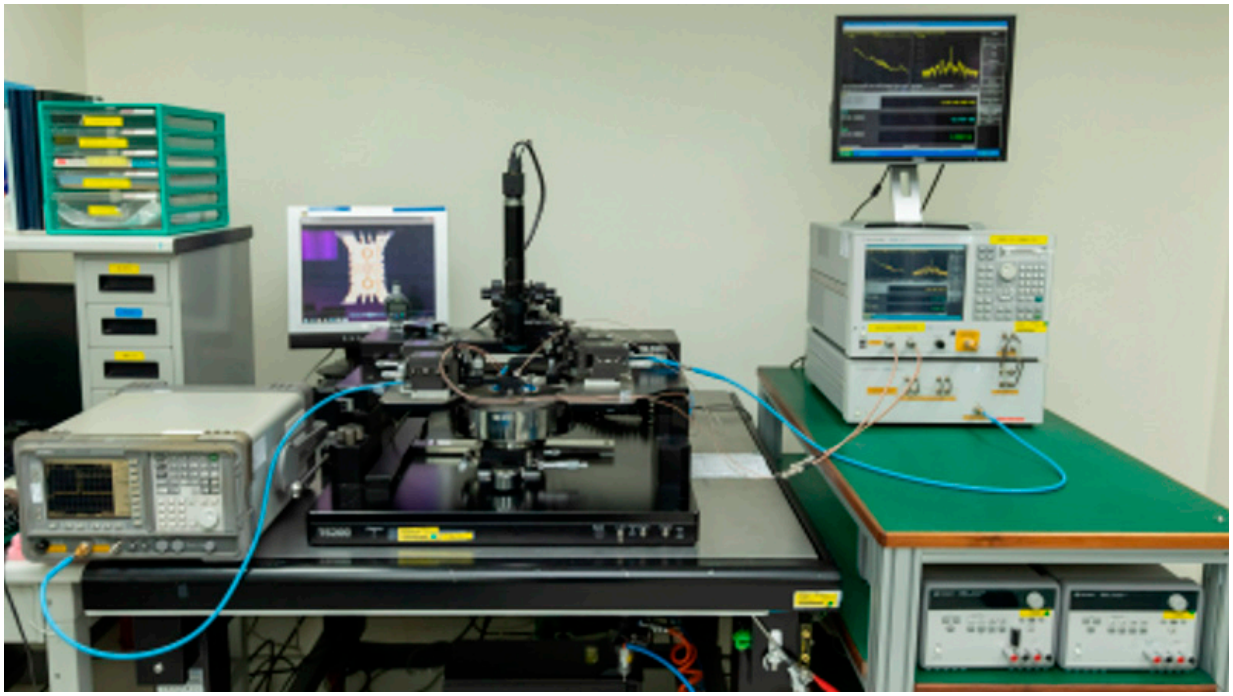


Figure 12. Photograph of the on-wafer measurement setup using a microwave probe station and the Keysight E5052B signal source analyzer (Keysight Technologies, Santa Rosa, CA, USA), showing real-time oscillator output measurement. The setup includes the probe station, the Keysight E5052B, and measurement display. The output signal of the proposed VCO is observed during actual testing, as shown on the connected monitors.

To assess the practical viability of the proposed VCO, we performed additional evaluations under realistic operating conditions. Post-layout simulations show that the oscillator maintains stable frequency output when subjected to supply voltage variation of ±5% and ambient temperature changes from 25 °C to 75 °C, exhibiting less than 1% frequency deviation.

Additionally, the oscillator's low supply voltage (0.8 V) and compact core design facilitate seamless integration with low-voltage RF modules such as PLLs and LNA front-

ends. The symmetric buffer stage also improves signal integrity and minimizes noise coupling in multi-module SoC environments.

These results support the robustness and integration readiness of the proposed VCO for use in real-world 802.11ac and IoT transceiver systems, especially where power efficiency and environmental tolerance are critical.

4. Conclusions

In this work, a low-power, wide-tuning-range voltage-controlled oscillator (VCO) for C-band applications was proposed and successfully implemented using the TSMC 0.18 μm 1P6M CMOS process. The design incorporates several techniques such as body-biasing and an optimized varactor structure to enhance tuning range and reduce power consumption, while maintaining low phase noise. The measured phase noise at a 1 MHz offset is as low as −117.6 dBc/Hz, and the achieved figure-of-merit (FOM) is −188.6 dBc/Hz. The VCO achieves a tuning range of 1124 MHz with a core power consumption of only 3.4 mW. These results demonstrate the proposed VCO's suitability for modern low-power communication systems, particularly in compact and battery-constrained IoT and 5G applications.

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Conflicts of Interest: The authors declare no conflicts of interest.

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