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0.7 V Supply SC Circuits with Relaxed Slew Rate Requirements Using GB-Enhanced Multiple-Output Class AB/AB Op-Amps

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Abstract: A family of improved low-voltage switched-capacitor circuits is introduced. It is based on the utilization of multiple-output class AB/AB op-amp architectures that provide true sample and hold outputs that are not subject to a reset phase as with conventional switched-capacitor circuits. This feature essentially relaxes the op-amp slew rate requirements, allowing a higher speed and simple low-voltage operation. A power-efficient GB boosting technique based on resistive local common mode feedback is used to significantly improve the GB and internal/external slew rate of the op-amps with only a 36.5% additional power dissipation.

Keywords: switched-capacitor circuits; low supply voltage; enhanced bandwidth; class AB Miller op-amps; resistive local common mode feedback; sample and hold

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1. Introduction

Switched-capacitor (SC) circuits were developed to overcome the accuracy limitations of integrated RC active continuous-time circuits. They allow the implementation of integrated filters with accurate time constants/frequency responses that do not require complex tuning circuitry and that are based on capacitor ratios and a highly accurate external reference clock frequency *fclk*. For this reason, they have been for many years essential buildings blocks in many signal-processing integrated systems. Besides traditional applications, SC circuits also offer advantages in many emerging fields that require an ultra-low power dissipation, like body area networks (BANs) in biomedical applications, sensor networks, the internet of things, RF power amplifiers, inductor-free switching-mode converters, etc. [1–5].

Figures 1 and 2 show the implementation of a conventional offset-compensated SC amplifier and a conventional SC first-order low-pass filter, respectively [6,7]. In practice, one of the main problems that limits the speed of SC circuits is the high slew rate (SR) requirements on the op-amps, since the outputs of the op-amps reset to zero (or to another constant value) during one clock phase and excursions from zero to the new sampled value during the other phase. This leads eventually to two large output voltage variations every clock cycle.

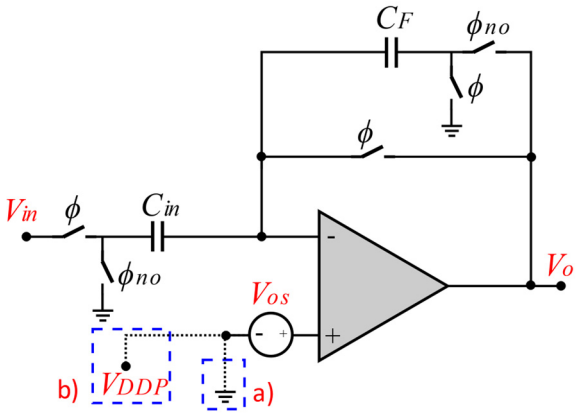


Figure 1. Conventional offset−compensated SC amplifier with a connection to (**a**) non inverting terminal is connected to a mid-supply voltage for nominal supply operation (shown here as ground potential) or (**b**) non inverting terminal connected to a voltage V_{DDP} close to one of the rails for low-voltage operation.

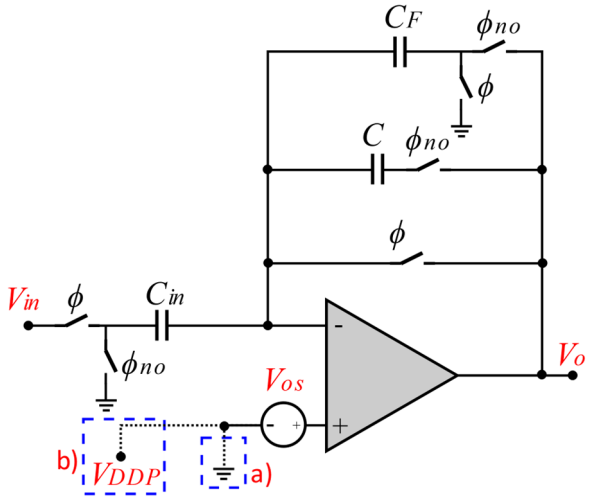


Figure 2. Conventional offset−compensated SC first−order low-pass filter (**a**) non inverting terminal is connected to a mid-supply voltage for nominal supply operation (shown here as ground potential) or (**b**) non inverting terminal connected to a voltage V_{DDP} close to one of the rails for low−voltage operation.

This problem can be avoided by using an op-amp with an auxiliary output that provides a true sample and hold signal without a reset to zero, as explained in the following section.

A second important concern for SC circuits and continuous-time analog circuits is the low-voltage operation required in modern deep sub-micrometer CMOS technologies whose nominal working supply voltages have been reduced faster than the threshold voltages with the downscaling of technology. In some cases, the nominal supply voltage in deep sub-micrometer CMOS technology does not even provide enough headroom for conventional analog circuits to be functional, unless MOS transistors operate in the subthreshold. Even in the cases where the nominal supply is sufficient to operate a circuit, lowering the supply voltage of an integrated circuit is highly desirable in order to reduce its power consumption for applications such as wireless and biomedical ones, IoT and RF IDs and especially to significantly reduce the power dissipation of the digital section of the circuit, which usually makes over 90% of the silicon area of a mixed-mode circuit and whose power dissipation is proportional to $V_{DD}{}^2$. Moreover, low-voltage operation enables a design's portability across different technologies. Some SC implementation-denoted comparator-based SC circuits have been reported where op-amps are replaced by CMOS inverters and current sources [8–10]. This is done in order to reduce power dissipation, improve the slew rate

and reduce supply requirements. Additionally, a number of op-amp architectures with an enhanced slew rate have been also reported to satisfy the high slew rate requirements of conventional SC circuits, with sample and reset to zero output signals [11–16].

In [17–19], schemes for the low-voltage operation of SC circuits were reported. The scheme reported in [17] consists simply of DC shifting the input gates of the op-amp from the conventional mid-supply voltage to a value V_{SSP} or V_{DDP} that is close to the lower or upper supply rails, V_{SS} or V_{DD}, for op-amps with a PMOS or NMOS input differential pair, respectively. This simple low-voltage technique (LVT) can be easily implemented, as illustrated in Figure 1b where an op-amp with an NMOS input differential pair is assumed. Here, low supply operation is possible, since both terminals of the op-amp operate at a reference voltage V_{DDP} that is close to V_{DD}. But this value is canceled out, along with the offset V_{os} in the signal path, since it is treated as an additional offset term. Unfortunately, this simple low-voltage implementation scheme worsens the SR limitation of the op-amp in SC circuits, since the output reset value is now close to one of the rails instead of to the mid-supply voltage, and the worst-case swing is increased by close to a factor of two. This is depicted in Figure 3 for the case of the SC amplifier of Figure 1 with a nominal gain $G = 4$ V/V that operates with ± 0.35 V supplies in 180 nm CMOS technology that has nominal supplies of ± 0.9 V. When the positive input terminal of the op-amp is connected to a voltage $V_{DDP} = 0.27$ V, the output resets also to $V_{DDP} + V_{os}$ during phase ϕ, and for the peak negative portion of the signal the required SR is almost doubled, since now a swing close to the supply is required during the reset phase ϕ. The multiple-output op-amp technique addressed above can be used to essentially alleviate this problem in low-voltage SC circuits based on the technique proposed here.

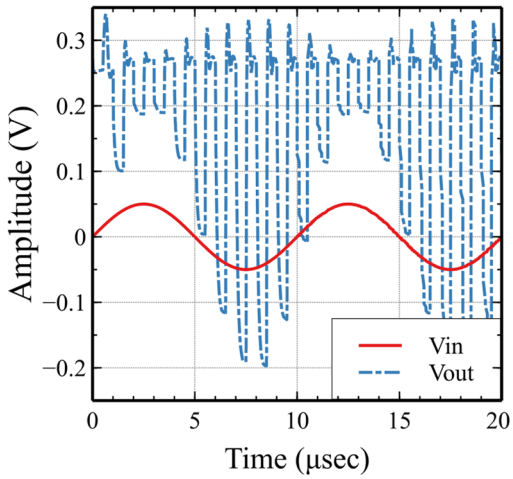


Figure 3. Transient response of the low-voltage implementation of SC amplifier of Figure 1 using a conventional op-amp for the gain.

In this paper, the implementation of low-voltage SC filters and amplifiers is presented as example of the proposed technique, but it can be extended to other SC circuits. The schemes are based on the use of op-amps with an auxiliary output that have true sample and hold output signals that greatly alleviate the op-amp slew rate requirements. We also introduce here a power-efficient class AB/AB op-amp that uses a simple GB enhancement technique to essentially improve the slew rate, GB and DC open-loop gain of the op-amp. This allows a higher frequency of operation and improved THD. SC architectures that perform correlated double sampling to cancel out offset can be easily implemented using this technique with a reduced supply voltage and with a very small additional power dissipation and silicon area.

The paper is organized as follows: Section 2 describes the proposed scheme and the GB-enhanced dual-output AB/AB op-amp used. Section 3 discusses simulation results of a low-voltage SC amplifier and a first-order low-pass filter in 180 nm CMOS technology operating with ±0.35 V supply voltages, which correspond to only 40% of the nominal supply voltage (±0.9 V) of this technology. Some conclusions are given in Section 4.

2. Circuit Description

2.1. GB-Enhanced AB/AB Op-Amp with Dual Ouputs

The multiple-output op-amp used to implement the low-voltage SC filter and amplifier is a GB-enhanced AB/AB Miller compensated op-amp with two outputs: the main signal output and an auxiliary low-power output.

Figure 4 shows a single-ended differential amplifier used commonly as the input stage of Miller op-amps. It has a gain $A_{inp} \approx A_i/2$, where $A_i = g_m r_o$ is the intrinsic gain of the MOS transistor, g_m is the transconductance gain of the differential pair transistors, and r_o is the output resistance of transistors MDP′ and MP1′ (assumed equal for simplicity). The proposed multiple-output op-amp uses a composite input stage that is GB- and slew rate-enhanced, and it is shown in Figure 5. This composite input is formed by two stages. The first stage has a differential pair and uses resistive local common-mode feedback (RLCMFB), provided by resistors R_{LCMFB} [20]. It operates in class AB, has a gain $A_{inl} \approx 5(A_i/2)$, and it has enhanced transconductance $g_{meff} \approx 5\, g_{mP2}$ as explained in the following subsection.

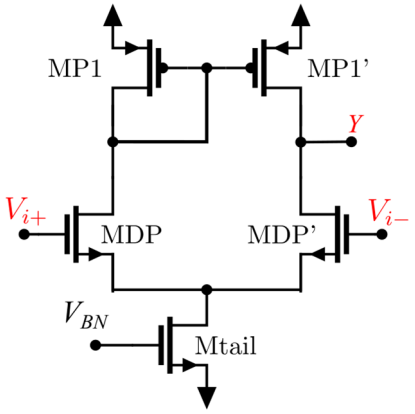


Figure 4. Input stage used commonly in Miller op-amps.

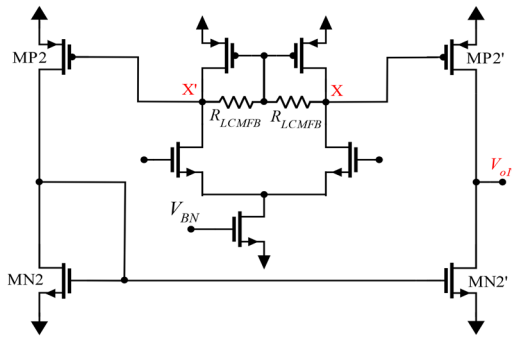


Figure 5. Gain- and GB-enhanced class AB composite input stage used in the proposed two-output Miller op-amp.

The two output stages (main and auxiliary) are shown in Figure 6. Output stage 1 shown in Figure 6a is a free class AB amplifier [21] used as the main (signal path) output of the op-amp. In this stage, free class AB dynamic operation is achieved by means of capacitor C_{bat} and resistor R_{Large}. The auxiliary output stage 2 shown in Figure 6b is a class

A amplifier, and it is used as the low-power auxiliary output of the op-amp. It operates with a bias current 10 times lower than the main output stage.

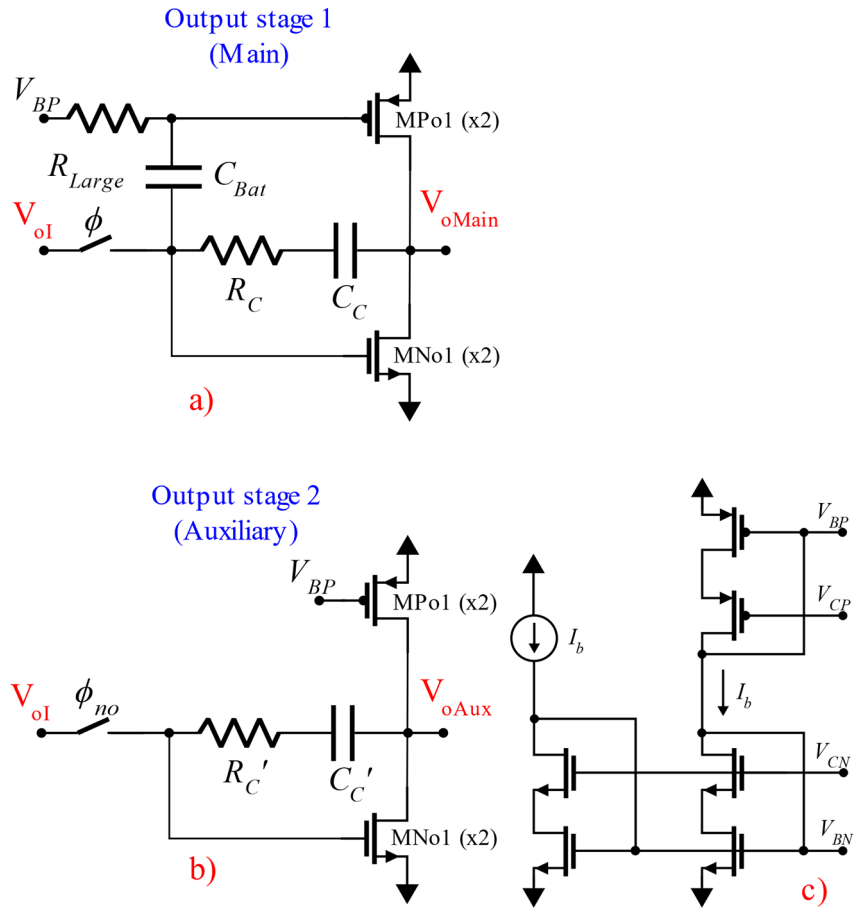


Figure 6. Output stages of multiple-output op-amp. (**a**) Main class AB output stage. (**b**) Auxiliary class A output stage. (**c**) Biasing circuit.

2.2. Operation of the Composite Input State

As indicated above, the composite input stage is formed by a differential amplifier (DA) with resistive local common-mode feedback (MDP, MDP′, MP1, MP1′ and R_{LCMFB}) and a current differencing shell with two branches formed by MN2, MP2, MN2′ and MP2′. This provides the op-amp with an enhanced gain and GB and class AB operation in the input stage. The composite input stage has a voltage gain $A_I = V_{oI}/V_d$ given by (1), where $g_{meffI} = A_{DA}g_{mP2}$ is the effective transconductance gain of the input stage, R_{outI} is the output impedance of the composite input stage at node V_{oI} given by (2), and $A_{DA} \approx 5$ is the gain enhancement factor of the differential amplifier given by (3). Therefore, the gain of the input stage can be expressed by (4), and it is approximately given by (5).

$$A_I = g_{meffI} \cdot R_{outI} = A_{DA} g_{mP2} \cdot R_{out} \tag{1}$$

$$R_{outI} = r_{oN2'} || r_{oP2} \tag{2}$$

$$A_{DA} = (V_{X'} - V_X)/(V_{i+} - V_{i-}) \approx g_{mDP} \cdot R_{LCMFB} \tag{3}$$

$$A_I = (g_{mDP} R_{LCMFB} g_{mP2}) * (r_{oN2} || r_{oP2}) \tag{4}$$

$$A_I = g_{mDP} R_{LCMFB} \frac{g_{mP2} r_o}{2} \approx A_{DA} \frac{g_{mP2} r_o}{2} \tag{5}$$

As indicated above, the gain of the composite input stage (and of the op-amp) is enhanced by a factor $R_{LCMFB}g_{mP2}A_{DP}$ with reference to the gain of the conventional op-amp using the input stage of Figure 4.

The value of R_{LCMFB} determines the gain and GB enhancement factor. It also determines the high-frequency poles $f_{pX,X'}$ at nodes X, X′. These poles are given by (6), where $C_{X,X'}$ are the parasitic capacitance at nodes X, X′. In order to avoid the phase margin degradation of the open-loop response, they are required to satisfy the condition $f_{pX,X'}$ >> GB. The maximum value of the GB enhancement factor (and consequently of R_{LCMFB}) is limited by this condition. In the herein proposed op-amps, R_{LCMFB} had a value of 50 kΩ, which provided a significant GB enhancement factor of approximately 5 and resulted in poles $f_{pX,X'}$ with values of $f_{pX,X'} \approx 65$ MHz, while the op-amp was designed for GB = 25 MHz. This corresponds to $f_{pXX'} \sim 2.6$ GB. Deep sub-micrometer CMOS technologies with finer feature sizes, have a very small capacitances $C_{X,X'}$ and make it possible to design op-amps with a higher GB enhancement factor.

$$f_{pX,X'} \approx \frac{1}{2\pi R_{LCMFB} C_{X,X'}} \tag{6}$$

Another advantage of the input stage of Figure 5 is that it operates in class AB. As explained in [20], it generates output currents at node V_{oI} that can be much higher (by close to an order of magnitude) than the bias current I_{bias}. This prevents the slew rate of the op-amp from being limited by the slew rate of the internal node V_{oI}.

The GB of the op-amp is derived in Equations (7)–(9), where $A_{II} = g_{mMPo}(r_{oMPO} \,||\, r_{oMNo}) \approx g_m r_o/2$ is the gain of the output stage(s). From (9), the GB of the op-amp is enhanced by the factor $A_{DP} \approx 5$ with respect to the GB of a conventional Miller op-amp with just a moderate increase (~33.3%) in power dissipation due to the composite input stage.

$$GB = A_I A_{II} f_{DomPole} = \frac{g_{meffI} R_{outI} A_{II}}{2\pi A_{II} R_{outI} C_C} \tag{7}$$

$$GB = \frac{g_{meffI}}{2\pi C_C} \tag{8}$$

$$GB = \frac{A_{DA} g_{mP2}}{2\pi C_C} \tag{9}$$

2.3. Operation of Output Stages

As indicated above, the dual-output op-amp used to implement the SC filter and amplifier uses two output stages, denoted the main and auxiliary output stages, which are shown in Figure 6. Output stage 1, shown in Figure 6a, is a free class AB amplifier that is used as the main signal output of the op-amp. Power-efficient free class AB operation at the output node is achieved by means of capacitor C_{bat} and resistor R_{Large} [21]. It is denoted as free class AB since it does not require additional power consumption or an increased supply voltage. The output stage 2 shown in Figure 6b is a class A amplifier, and it is used as the auxiliary output of the op-amp. The main output of the op-amp drives the load C_L = 15 pF, while the auxiliary output works around the overall offset voltage (V_{os} + V_{DDP}), drives only the capacitor C_{in} and does not require a high slew rate, since it is not subject to large voltage variations, given that it remains at an approximately constant voltage throughout the operation of the circuit, as explained below. Figure 6c shows the biasing circuit used to generate V_{BN} and V_{BP}. PMOS and NMOS diode-connected transistors with dimensions W/6L biased with a current Ib are used to generate cascode voltages V_{CN} and V_{CP}. These diode-connected transistors generate voltages $V_{GS}' = V_{TH} + V_{DSsat}'$ that have

drain–source saturation voltages $V_{DSsat}' \approx 2.5\ V_{Dssat}$ approximately 2.5 times larger than the drain–source saturation voltages of transistors in the main circuit.

The composite input stage sequentially drives the two output stages during each of the clock non-overlapping phases ϕ and ϕ_{no}. These blocks leverage the compensation capacitances C_C and C_C' to hold the output voltages of each output for close to a whole clock period while they are not in the feedback loop and are disconnected from the input stage. None of the outputs is subject to large changes due to a reset phase, as is the case in conventional SC circuits, and for this reason, the slew rate requirements imposed on the op-amp are greatly relaxed. The auxiliary output stage holds the DC voltage $V_{oAux} = V_{DDP} + V_{os}$ (see Section 2.4) and can operate with a fraction of the bias current I_{bias} of the main output stage, since the only load it drives is the sampling capacitor C_{in}, and it is not subject to large voltage variations.

2.4. Low-Voltage SC Amplifier

Figure 7 shows the proposed low-voltage implementation of an SC amplifier with offset compensation using the multiple-output op-amp described in the previous section. The gain A in this circuit is determined by capacitors C_f and C_{in}, as stated in Equation (10). During phase ϕ, the input of the auxiliary amplifier is connected internally to the output terminal of the input stage, and its output (the auxiliary output) is connected externally to the negative input terminal of the op-amp. In this case, the circuit is configured as a voltage follower with respect to V_{oAux}. This forces the auxiliary output to settle to a voltage $V_{oAux} = V_{DDP} + V_{os}$. At the same time, C_{in} and C_f charge to voltages $V_{Cin} = V_{in} - (V_{os} + V_{DDP})$ and $V_{CF} = V_{os} + V_{DDP}$, respectively. During the following phase ϕ_{no}, the auxiliary output is disconnected from V_{oI}, and the main output is connected internally to V_{oI} and externally to C_f The charge stored in C_{in} is transferred to C_f, so that the main output voltage settles to the amplified version of the sampled input signal, $V_{oMain} = -(C_{in}/C_f)V_{in}$. This voltage is held at the main output by the compensation capacitor C_C during the entire clock cycle, even after the main output is disconnected from the input stage during phase ϕ. Therefore, the main output is not reset to zero as in conventional SC circuits. It just changes to the new sampled value every clock cycle at the beginning of phase ϕ_{no}. On the other hand, the auxiliary output remains at the constant voltage $V_{oAux} = V_{os} + V_{DDP}$ throughout the operation of the circuit, and for this reason it is not subject to voltage changes and does not require a high slew rate.

$$A = \frac{V_o}{V_i} = -\frac{C_{in}}{C_f} \tag{10}$$

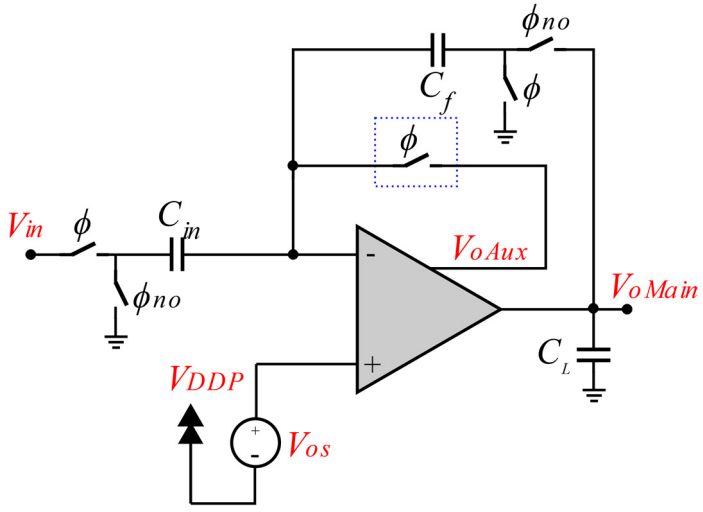


Figure 7. Proposed low−voltage SC amplifier based on op-amps with two outputs.

2.5. Low-Voltage SC Low-Pass Filter

The proposed low−voltage implementation of an SC low−pass filter using a two-output op-amp is shown in Figure 8. This implementation also performs a correlated double sampling that leads to offset compensation. The value V_{DDP} connected at the positive input terminal of the op-amp is treated as an additional offset term that is also stored and compensated for in the auxiliary output during phase ϕ_{no}. A value $V_{DDP} = V_{DD} - V_{SDsat}$ is used to allow the PMOS transistor M_{Po1} of the auxiliary output stage to remain in saturation. This allows the low-voltage operation of the circuit, since the capacitors act as floating DC sources that maintain the inputs of the op-amp to a voltage $V_{DDP} + V_{os}$ close to the positive rail, providing enough headroom for the NMOS input differential pair to operate with a low supply voltage. In this scheme, the capacitors C_f and C_{in} behave as resistors with equivalent values $R_f = 1/f_{clk}C_f$ and $R_{in} = 1/f_{clk}C_{in}$, where $f_{clk} = 1/T_{clk}$ is the clock frequency. Therefore, the cutoff frequency of the circuit is determined by the combination of the feedback capacitors C_f and C and is given by (11).

$$f_{cutoff} = \frac{f_{clk}C_f}{2\pi C} \tag{11}$$

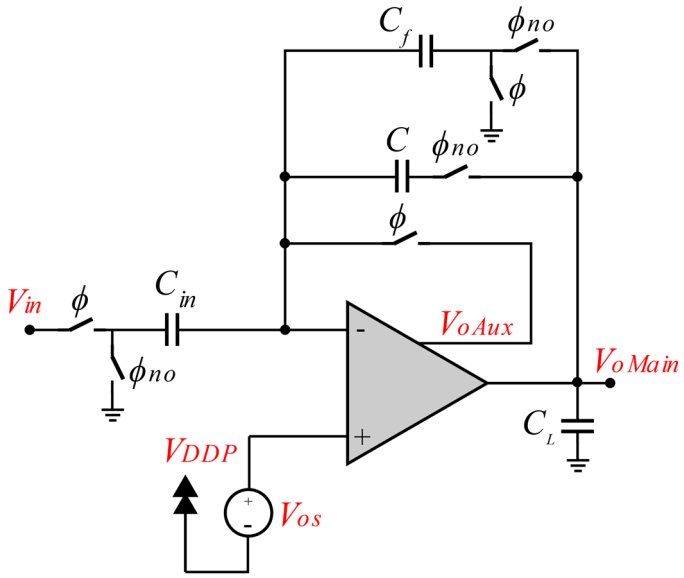


Figure 8. Proposed low−voltage implementation of an SC low-pass filter using a two-output GB-enhanced Miller op-amp.

3. Simulation Results

The proposed low-voltage SC amplifier and low-pass filter circuits of Figures 7 and 8 were simulated using Cadence Design Framework II for commercial 180 nm CMOS technology. This technology has a nominal supply voltage V_{supply} = 1.8 V and exhibits NMOS and PMOS threshold voltages of $V_{thN} \approx |V_{thP}| \approx 0.55$ V. The circuit was designed to operate with dual supplies $V_{DD} = -V_{SS} = 0.35$ V (40% of the nominal supply) and a bias current I_{bias} = 10 μA, leading to a 43.4 μW quiescent power consumption. Both output stages (main and auxiliary) use Miller compensation capacitors and resistors C_C = 2 pF, R_C = 32 kΩ. The main output stage drives a 20 pF load capacitance. A comparison of the op-amp performance with some previously reported proposals is shown in Table 1. The two-stage op-amp used to implement the proposed SC amplifier has a gain–bandwidth product GB = 23 MHz, a phase margin PM = 45° and a slew rate SR = 9.41 V/μs. Therefore, the proposed amplifier exhibits a small signal figure of merit FOM_{SS} = 10,698 (MHz*pF/mW) and a large signal figure of merit FOM_{LS} = 4376 ((V/μs)*(pF/mW)). In practice, the high speed of a circuit is determined

by both the FOM_{SS} and FOM_{LS}. A global high-speed figure of merit is determined by the geometric mean of the FOM_{SS} and FOM_{LS}s. The FOM_{Global} is 6842 for the proposed GB-enhanced class AB op-amps. All the figures of merit are described by Equations (12)–(14). From Table 1, it can be asserted that the proposed circuit has the highest FOM_{SS} and highest FOM_{Global}.

Table 1. Comparison table.

Parameters	[22] 2017	[23] 2016	[24] 2015	[25] 2015	Class AB Miller Op-Amp	This Work With Enhanced Class AB Miller Op-Amp
CMOS Tech. Process (nm)	180	180	90	65	180	180
Configuration	SE	SE [a]	FD [b]	SE [a]	SE [a]	SE [a]
Supply (V)	±0.9	0.7	1.2	0.35	±0.35	±0.35
V_{DDP} (V)		-	-	-	0.27	0.27
I_{bias} (uA)	1	4	-	-	10	10
I_{supply} (uA)	8	36.28	483.33	49	40	60
P_{diss} (uW)	14.5	25.4	580	17.15	28	43.4
A_{OLDC} (dB)	67	57.5	59.1	43	49	56
C_L (pF)	20	20	5	3	20	20
C_C (pF)		0.58 [c]	-	0.6 [c]	2	2
R_C (kOhm)		-	-	-	15	32
SR (V/us)	24.11	1.8	115.2	5.6	0.8	9.41
GB (MHz)	0.57	3	650	3.6	5.72	23
PM (°)	82	60	50	56	63	45
FOM_{LS} ([V/us*pF/mW])	37,300	2200	990	980	571	4376
FOM_{SS} (MHz*pF/mW)	900	2.360	5600	630	4085	10,698
$\frac{FOM_{Global}}{\sqrt{FOM_{LS}FOM_{SS}}}$	5794	2278	2354	785	1527	6842

[a] Single-Ended; [b] Fully Differential; [c] Total $C_C = C_{C1} + C_{C2}$.

Regarding the large signal figure of merit (FOM_{LS}), the proposed circuit exhibits a higher value than the state-of-the-art work presented in Table 1, except for reference [22]. The FOM_{LS} is important for circuits with high slew rate requirements. The proposed low-voltage switched-capacitor circuits were designed with dual-output op-amps that have true sample and hold outputs. The op-amp does not need to react fast to a long step change, which essentially relaxes the high slew rate requirements. On the contrary, in the case of the conventional sample and hold circuit with a conventional op-amp, the outputs of the op-amps reset to zero (or to another constant value) during one clock phase and excursion from zero to the new sampled value during the other phase. This leads to two significant output voltage variations every clock cycle. Thus, the conventional op-amp needs to have a high slew rate.

$$FOM_{SS} = \frac{GB * C_L}{P_{Diss}} \left[\frac{MHz * pF}{mW}\right] \quad (12)$$

$$FOM_{LS} = \frac{SR * C_L}{P_{Diss}} \left[\frac{(V/\mu s) * pF}{mW}\right] \quad (13)$$

$$FOM_{Global} = FOM_{LS} * FOM_{SS} \quad (14)$$

3.1. Low-Voltage SC Amplifier Results

The amplifier was designed for an amplification factor $G = C_{in}/C_f = 4$, where $C_{in} = 4$ pF and $C_f = 1$ pF. Figures 9 and 10 show the transient response of conventional low-voltage SC amplifier using a class A Miller op-amp and conventional low-voltage SC amplifier using the enhanced class AB single output Miller op-amp respectively. Figure 11 shows the transient simulation of the proposed low-voltage SC amplifier. For all of these circuits similar input signals a 100 mV_{pp} 100 kHz sinusoidal input, a 1 MHz clock and with

an op-amp offset voltage V_{os} = 30 mV were used. Clock voltage boosting by a factor of two was used [26] to allow switches to operate with rail-to-rail signals and a low supply voltage. The slew rate requirement was highly relaxed as compared to the transient response of the conventional low voltage SC amplifier that uses a class A Miller op-amp; this is depicted in Figure 9. Figure 10 shows the output of the conventional SC amplifier utilizing the proposed GB SR-enhanced AB/AB op-amp with no auxiliary output. The slew rate is improved, but significant distortion is present due to the large slew rate required by the low-voltage operation of the circuit. Simulations of the proposed technique using the enhanced multiple-output Miller op-amp are shown in Figure 11. It can be seen that the output is a true sample and hold signal with no reset to zero or to another constant voltage. The multiple-output technique reduces the slew rate requirements imposed on the op-amp by low-voltage SC circuits. Moreover, it also cancels the 30 mV op-amp input offset voltage. The outputs of the conventional and proposed amplifier are compared in Figures 12–15, showing the PVT simulations of the circuit. The design is robust to ss, tt and ff process variations, as well as to 0 °C, 25 °C and 85 °C temperature corners and to supply voltage variations up to 10%.

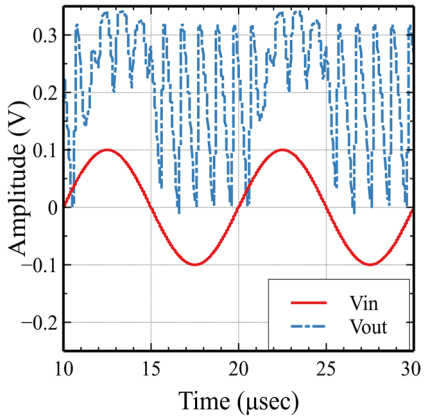


Figure 9. Transient simulation of the conventional low-voltage SC amplifier using a class A Miller op-amp. The input is a 100 mVpp 100 kHz sinusoidal with a 30 mV op-amp input offset voltage.

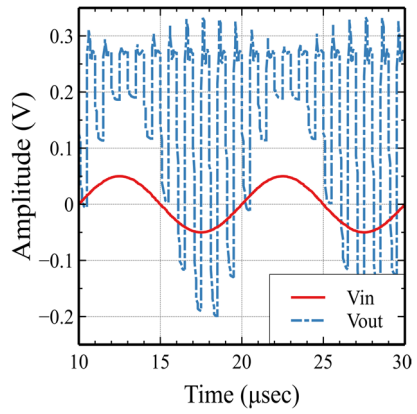


Figure 10. Transient simulation of the conventional low-voltage SC amplifier using the enhanced class AB single output Miller op-amp. The input is a 100 mVpp 100 kHz sinusoidal input with a 30 mV op-amp input offset voltage.

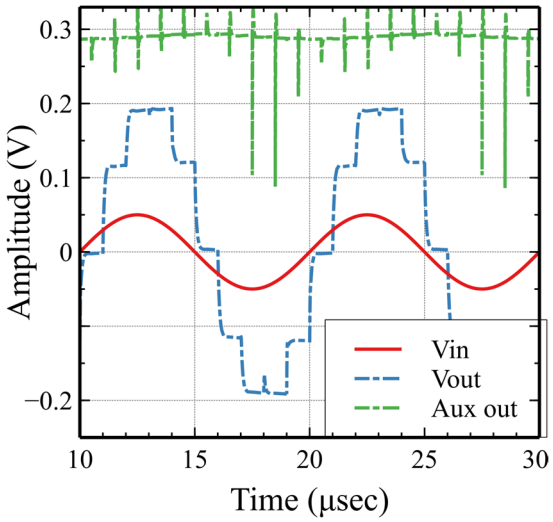


Figure 11. Transient simulation of the proposed low-voltage SC amplifier using a multiple-output enhanced AB/AB Miller op-amp. The input is a 100 mVpp 100 kHz sinusoidal and 30 mV op-amp input offset voltage.

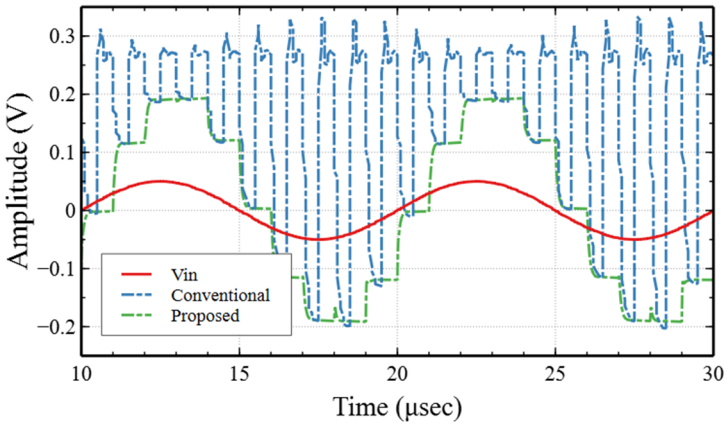


Figure 12. Comparison of transient simulations of a conventional low-voltage SC amplifier using the enhanced class AB single-output Miller op-amp and the proposed low-voltage SC amplifier using a dual-output enhanced AB/AB Miller op-amp. The input is a 100 mVpp 100 kHz sinusoidal input with a 30 mV op-amp input offset voltage.

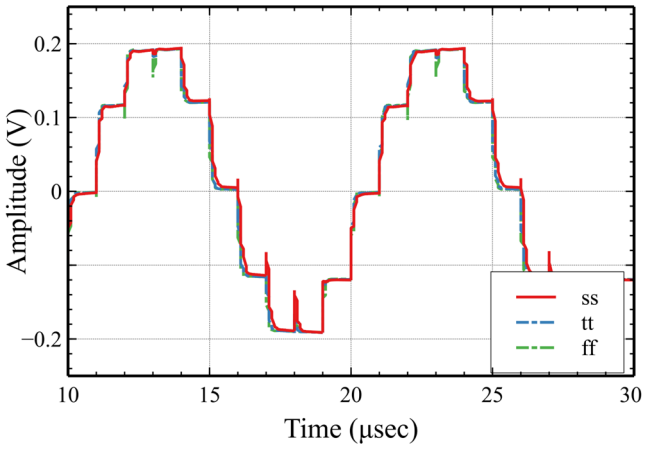


Figure 13. Process corner simulation with a 50 mVpp 100 kHz sinusoidal input that has a 30 mV op-amp input offset.

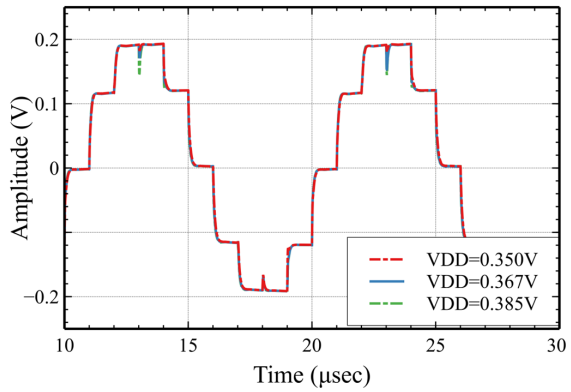


Figure 14. Supply voltage corner simulation with a 50 mVp 100 kHz sinusoidal input with a 30 mV offset.

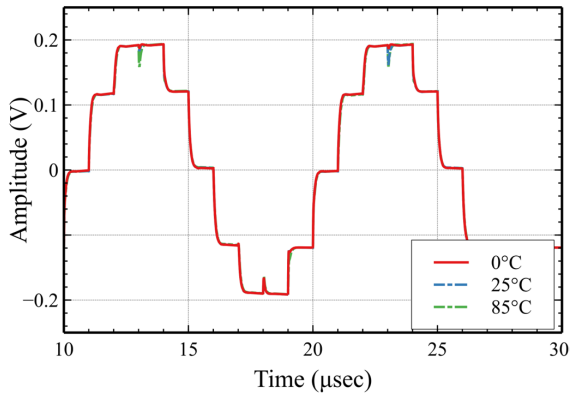


Figure 15. Temperature corner simulation with a 50 mVp 100 kHz sinusoidal input that has a 30 mV offset.

3.2. Low-Voltage SC Low-Pass Filter

The proposed low-pass filter was designed for a cutoff frequency f_{cutoff} = 50 kHz. The circuit is controlled by a non-overlapping clock generator circuit operating with a clock frequency f_{clk} = 5 MHz. The switched capacitors $C_{in} = C_f$ = 1 pF perform as resistors, with values $R_{in} = R_f$ = 200 kΩ. On the other hand, a capacitor C = 15.9 pF, in combination with the equivalent resistance value of C_f, yields to the filter's cutoff frequency f_{cutoff} = 50 kHz. The frequency response of the circuit that was extracted from transient simulations is depicted in Figure 16. The transient simulation of the low-pass filter with a 50 kHz, 400 mVpp input signal with 30 mV DC offset is depicted in Figure 17 for the proposed circuit and in Figure 18 for the conventional implementation. As opposed to the conventional one, the proposed technique cancels out the 30 mV DC offset and the V_{DDP} voltage at the input. Moreover, the conventional SC filter resets every cycle to the voltage $V_{DDP} + V_{os}$.

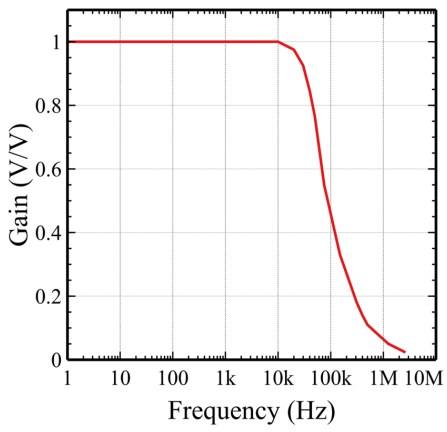


Figure 16. Frequency response of the low-voltage low-pass SC filter of Figure 8.

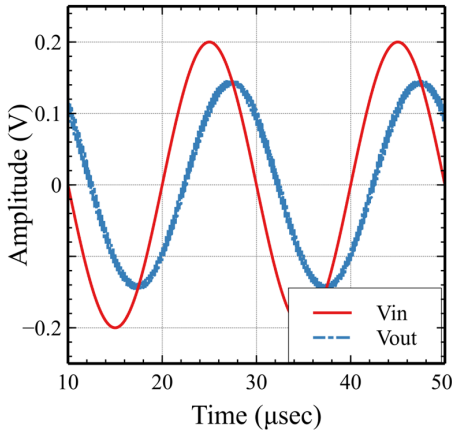


Figure 17. Low-voltage low-pass filter simulated transient response for a 50 kHz, 400 mVpp sinusoidal input signal with 30 mV input offset for the proposed LV dual-output class AB/AB op-amp with enhanced input stage.

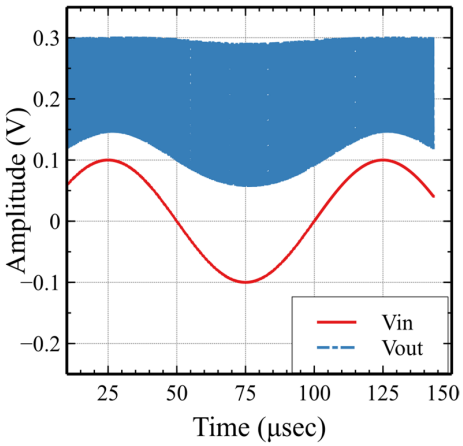


Figure 18. Conventional low-voltage low-pass filter simulated transient response for a 50 kHz, 400 mVpp sinusoidal input signal with 30 mV input offset for the LV implementation with single-output class AB op-amp.

4. Conclusions

A family of low-voltage SC circuits based on multiple-output GB-enhanced class AB/AB op-amps was introduced. The application of this concept was exemplified with a low-pass filter and an amplifier, but it can be easily extended to other SC circuits. The circuits are offset-compensated and capable of operating with dual supply voltages of ±0.35 V anda bias current I_{bias} = 10 µA in technology with a ±0.9 V nominal supply voltage. The circuits consume 43.4 µW of power. It was verified that the proposed technique is especially appropriate for low-voltage operation, since it essentially relaxes the op-amp slew rate requirements. This is due to the fact that the op-amp signal outputs are true sample and hold signals, which are not subject to a reset phase that requires large output voltage variations. The implementations were validated by the simulation of SC circuits using Cadence Design Framework II and parameters for commercial 180 nm CMOS technology.

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