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A Novel Low-Power Differential Input Current Summing Second-Generation Voltage Conveyor

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Abstract: This paper presents a novel transistor-level design of a modified second-generation voltage conveyor (VCII), which incorporates two differential current inputs ($Y+$ and $Y-$) and gives a voltage output at terminal X that mirrors the sum of these currents. The circuit operation is based on current mirrors that maintain the X terminal in a stable “quiescent” state when no differential current is applied at $Y+$ and $Y-$. When a current flows into one of the two inputs, the sum is mirrored into X , providing a summed current measurement. This design, developed in a standard $0.35\text{ }\mu\text{m}$ CMOS transistors technology, ensures circuit high accuracy and robustness. The low power consumption of $24.6\text{ }\mu\text{W}$ makes it well-suited for portable biomedical applications as in environmental fields.

Keywords: voltage conveyor; VCII; low power



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1. Introduction

In recent years, the popularity of current-mode circuits has grown substantially, driven by their good high-frequency response, simple architecture, and suitability for low-voltage operation [1–5]. Current mode approach components have become fundamental in analog signal processing, frequently replacing operational amplifiers in portable biomedical, industrial [6–13], and low-power applications [14–20], due to their improved dynamic range and efficient current-mode processing capabilities. Current and voltage conveyor performance has been further optimized by advances in CMOS scaling technology, which are now reaching the nanometer level. This has improved speed and power efficiency, even at low supply voltages.

In order to overcome the disadvantages of current conveyors, voltage conveyors (VCII) were developed. These active components offer a low-impedance voltage output suitable for applications that need both current and voltage signals [21]. Much attention has been paid to VCII recently; some of their many applications in implementing filters, gyrators, oscillators, inverting and non-inverting voltage amplifiers, current-to-voltage converters, differentiators and integrators, TIA amplifiers, and readout circuits have been reported [22–29].

This paper introduces a novel variation in VCII design: the X terminal mirrors the sum of the input currents, opening a wide range of potential applications where cumulative current measurement is required [30,31].

The proposed summing VCII is particularly well-suited for multi-sensor environmental monitoring systems [32,33]. The summed current output at X , for instance, might offer an aggregate estimate of air quality in those monitoring systems where multiple sensors

detect different contaminants [34–36]. This would simplify the overall data processing and allow for a faster response to pollution levels.

Similarly, in battery management systems, this configuration could track the total current from multiple cells, providing an accurate indicator of overall energy usage or charge state. In biomedical applications, the summing VCII could aggregate currents from multiple biosensors [37], such as those monitoring the same parameter at the same time but in different locations, providing an overall view of the physiological status.

Definitively, this paper presents the transistor-level design and standard operational principles of a summing VCII, optimized for low power consumption. CMOS technology is utilized to implement high-precision current mirrors, ensuring minimal offset and accurate summation. Through detailed simulations, we demonstrate the performance benefits of this configuration and explore its applicability in advanced sensing and monitoring technologies. The manuscript is organized as follows: Section 2 describes the general structure and operation of the VCII; Section 3 provides the analysis of the basic parameters of the summing VCII and an in-depth analysis of the design parameters and transistor-level implementation; Section 4 presents simulation results; Section 5 discusses potential applications and concludes the paper.

2. VCII Overview

A VCII can essentially be seen as the dual circuit of the Second-Generation Current Conveyor (CCII) block. VCII is increasingly used as an alternative to the traditional voltage-mode circuits and the CCII [38–40]. In VCII, as with the CCII, information is conveyed through both currents and voltages. However, VCII includes distinct input and output voltage ports, which makes voltage measurements simpler—a key advantage over the CCII. Additional benefits include higher gain-bandwidth products, faster operation, low noise, wider dynamic range, and simpler implementation. Since the VCII is the dual of the CCII, the same analysis techniques used for the CCII can be adapted for the VCII as well.

Figure 1 illustrates the symbol and equivalent circuit of the VCII, showing that an ideal VCII operates as a current buffer from the Y terminal to the X terminal and as a voltage buffer from the X terminal to the Z terminal. Specifically, Y is a low-impedance (ideally zero) current input, X is a high-impedance (ideally infinite) voltage input and current output, and Z is a low-impedance (ideally zero) voltage output. The ideal voltage–current relationships of a VCII are given by

$$\begin{bmatrix} I_X \\ V_Z \\ V_Y \end{bmatrix} = \begin{bmatrix} \pm\beta & 0 & 0 \\ 0 & \alpha & 0 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix}, \quad (1)$$

with α and β being ideally unitary gains. Depending on whether $i_X = +i_Y$ or $i_X = -i_Y$, we classify the device as VCII+ or VCII−, respectively. Given the dual nature of the CCII and VCII, Y and Z terminals of a VCII have RLC-type parasitic impedances, while X parasitic terminal impedance is of the RC type, as shown in Figure 2.

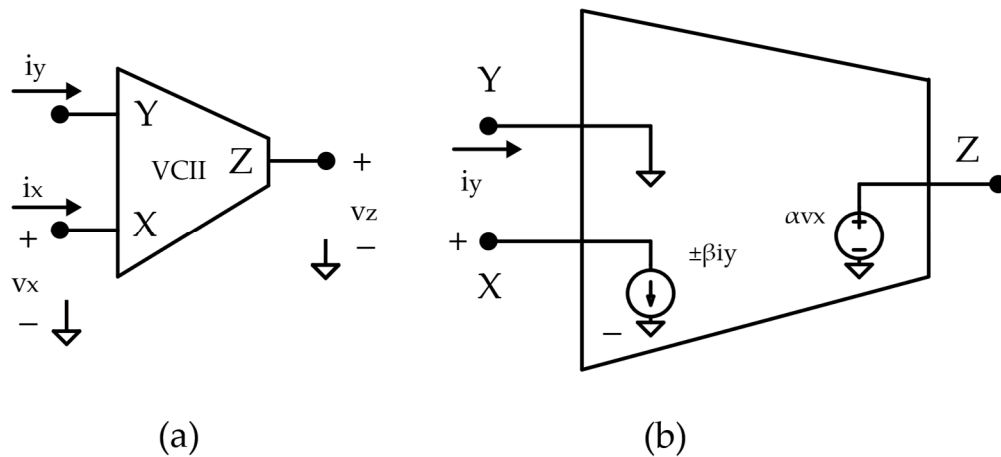


Figure 1. Second-generation voltage conveyor (a) circuit symbol (b) equivalent circuit.

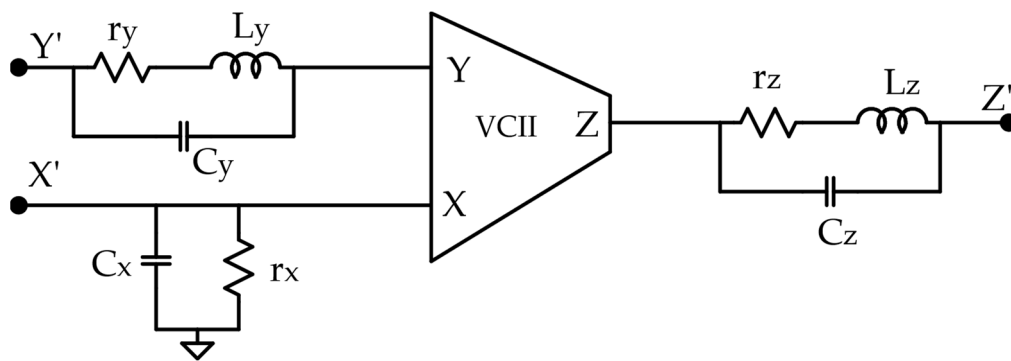


Figure 2. Second-generation voltage conveyor with typical parasitic components.

3. Proposed VCII

The design presented in this study introduces a transistor-level implementation of a VCII, specifically structured to include a voltage input terminal (X) and a voltage output terminal (Z), together with two current input terminals (Y+ and Y−).

The operation of the proposed VCII circuit is based on its current-mirroring structure, which enables it to output the sum of the input currents at terminal X. Current mirrors connected to Y+ and Y− stabilize terminal X when it is at rest.

When a current is applied to either Y+ or Y−, this current is mirrored onto X, with identical but opposite effects for Y+ and Y−, respectively. When both Y+ and Y− receive equal currents, the current at X doubles the input current on each terminal, representing the sum of the currents from Y+ and Y−.

This summed current at X is used to create an output voltage at terminal Z by taking advantage of the properties of the VCII. The output voltage is proportional to the summed current, as shown by

$$V_{OUT} = R_{GAIN}(I_{Y+} + I_{Y-}) \quad (2)$$

where R_{GAIN} is used as a gain resistor (in this case with a value of 100 k Ω) placed on terminal X. This relationship allows the VCII to produce a voltage output directly proportional to the sum of the currents on Y+ and Y−, enabling it to serve applications requiring cumulative current sensing. When an overall measurement of several sources is required, this summing function is especially helpful because it offers a practical way to translate summed current data into a corresponding voltage output at Z.

In Figure 3 the symbol of the proposed dual Y VCII is shown, and in (3) the relationships between voltages and current are reported.

$$\begin{bmatrix} V_{Y+} \\ V_{Y-} \\ I_X \\ V_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ \beta^+ & \beta^- & 0 \\ 0 & 0 & \alpha \end{bmatrix} \begin{bmatrix} I_{Y+} \\ I_{Y-} \\ V_X \end{bmatrix}. \quad (3)$$

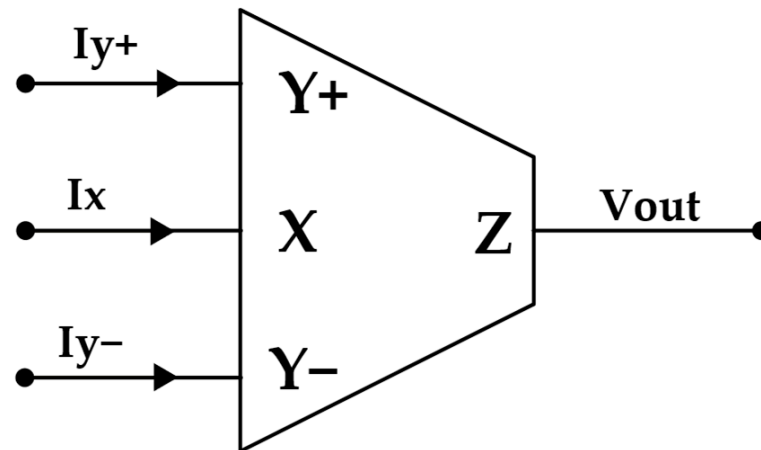


Figure 3. Proposed dual Y VCII as block scheme.

The proposed circuit is built around a dual differential pair structure. The $Y-$ terminal is defined by the first differential pair, which is made up of NMOS transistors, while the $Y+$ terminal is defined by the second differential pair, which is made up of PMOS transistors. These differential pairs serve to control the current flow and establish the mirrored behavior that enables the VCII to sum the input currents from $Y+$ and $Y-$ at the X terminal. In this configuration, each differential pair splits the input current based on the voltage difference applied to its gates. The NMOS differential pair on $Y-$ provides a low-impedance path for current, allowing it to respond quickly to variations in input current, while the PMOS pair on $Y+$ supplies a high impedance, creating complementary behavior between the two pairs. This complementary action allows the sum of the inputs on $Y+$ and $Y-$ to be appropriately converted by the mirrored current on X . Transistors $M1$ and $M2$ are in a regulated common-gate configuration, so they are biased by the differential pairs voltages, providing the virtual ground at the $Y+$ and $Y-$ terminals and reducing their impedances.

A voltage follower stage comes just after the differential pairs. Acting as a buffer, this stage keeps the output voltage at the target level without significantly loading the stages that come before it. By limiting the impact of the following stages and lowering the impedance that the remainder of the circuit perceives, the voltage follower stabilizes the output and makes sure that the summed current is accurately converted to a voltage output at terminal Z . Accurate voltage conversion and current summing are made possible by this design, which combines dual differential pairs with a voltage follower to provide exact and reliable input current summation.

The circuit configuration, at the transistor level, is shown in Figure 4.

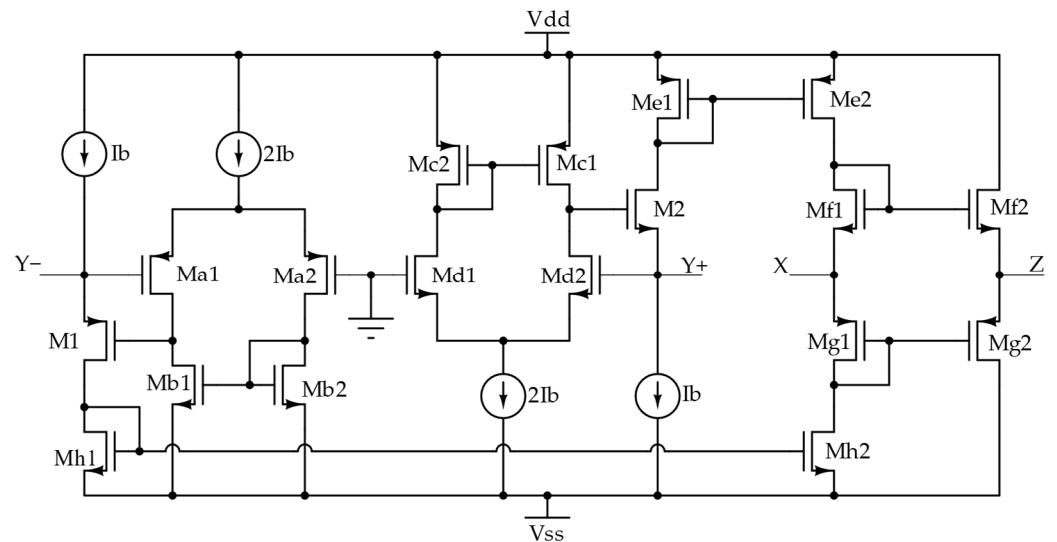


Figure 4. The proposed dual Y VCI configuration at the transistor level.

4. Simulation Results

Simulations were performed employing 0.35 μm CMOS technology through the LT-Spice simulator. Transistor dimensions are shown in Table 1; all transistors are sized for optimization of terminal impedances and mid-dynamic biasing. Supply voltages were set to ± 0.9 V, while bias current I_b was set to 3 μA . In the proposed design, the current sources in the original circuit have been replaced in simulation with current mirrors, all with an aspect ratio of 100 $\mu\text{m}/1.4$ μm , to achieve a more realistic representation of practical circuit behavior. Each differential pair receives double the input bias current thanks to the precise sizing of these current mirrors. This adjustment in mirror sizing maintains the desired operating conditions for both differential pairs, enhancing the accuracy of the simulated performance and reflecting a more practical implementation of the VCI circuit.

Table 1. Transistor sizes.

Transistor	Sizes (W, L) μm
$M_{a1}; M_{a2}$	100; 0.35
$M_{b1}; M_{b2}$	50; 0.7
$M_{c1}; M_{c2}$	50; 1.4
$M_{d1}; M_{d2}; M_2$	100; 0.7
$M_{e1}; M_{e2}$	8.9; 1.4
$M_{f1}; M_{f2}$	32.1; 0.7
$M_{g1}; M_{g2}$	30; 0.35
$M_{h1}; M_{h2}$	10.15; 0.35
M_1	100; 1.4

In Figure 5, Figure 6, and Figure 7, the DC performances of α , $\beta+$, and $\beta-$ parameters are shown, respectively. To assess the first parameter, a varying input voltage was applied at the X terminal, oscillating between the negative and positive supply voltages. The results indicate that the parameter α consistently remains linear between -300 mV and $+300$ mV, determining this range as the output operating range. Similarly, the behavior of the two β parameters was analyzed by applying a current, sweeping between -5 μA and 5 μA , to the Y correspondent port and measuring the resulting current at the X port under different input current conditions.

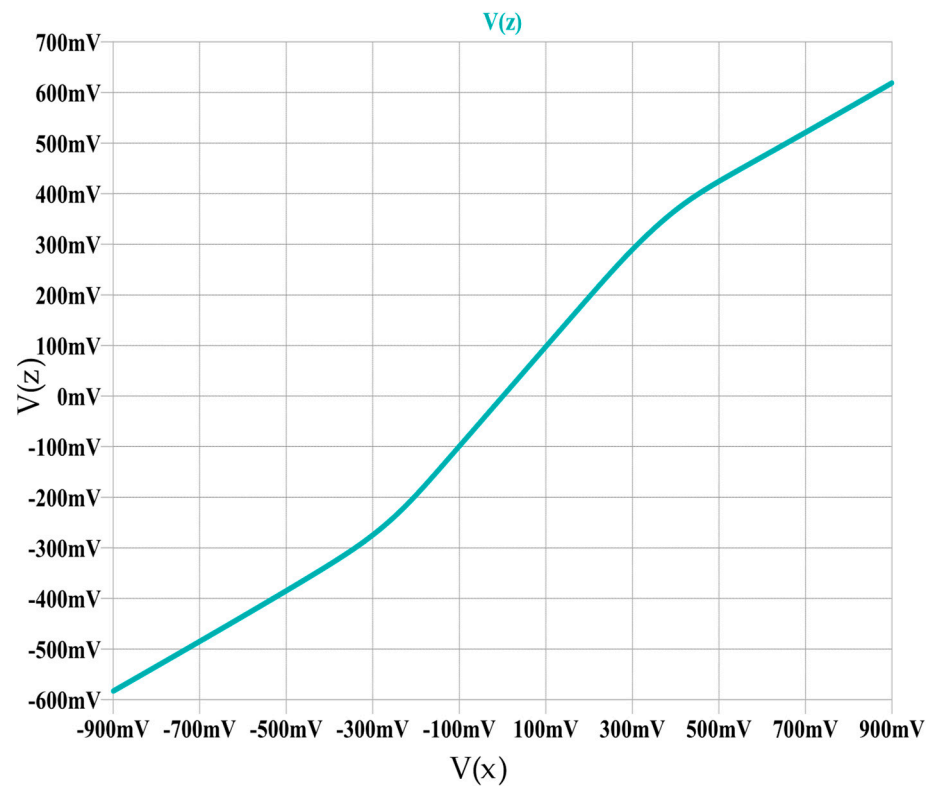


Figure 5. DC performances of the α parameter; $V(z)$ vs. $V(x)$.

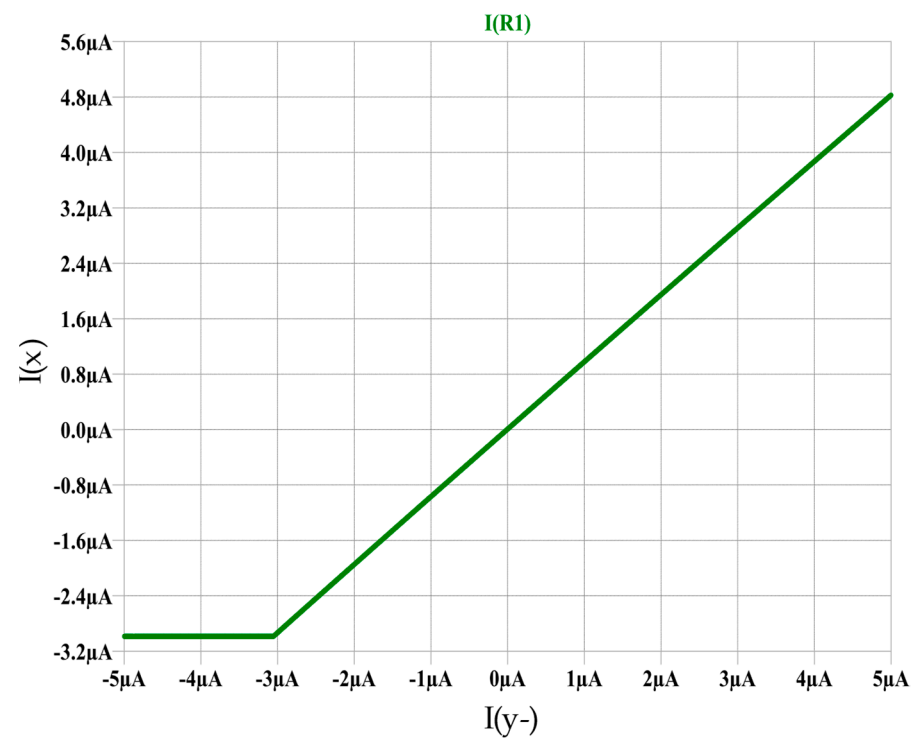


Figure 6. DC performances of the $\beta+$ parameter; $I(x)$ vs. $I(y-)$.

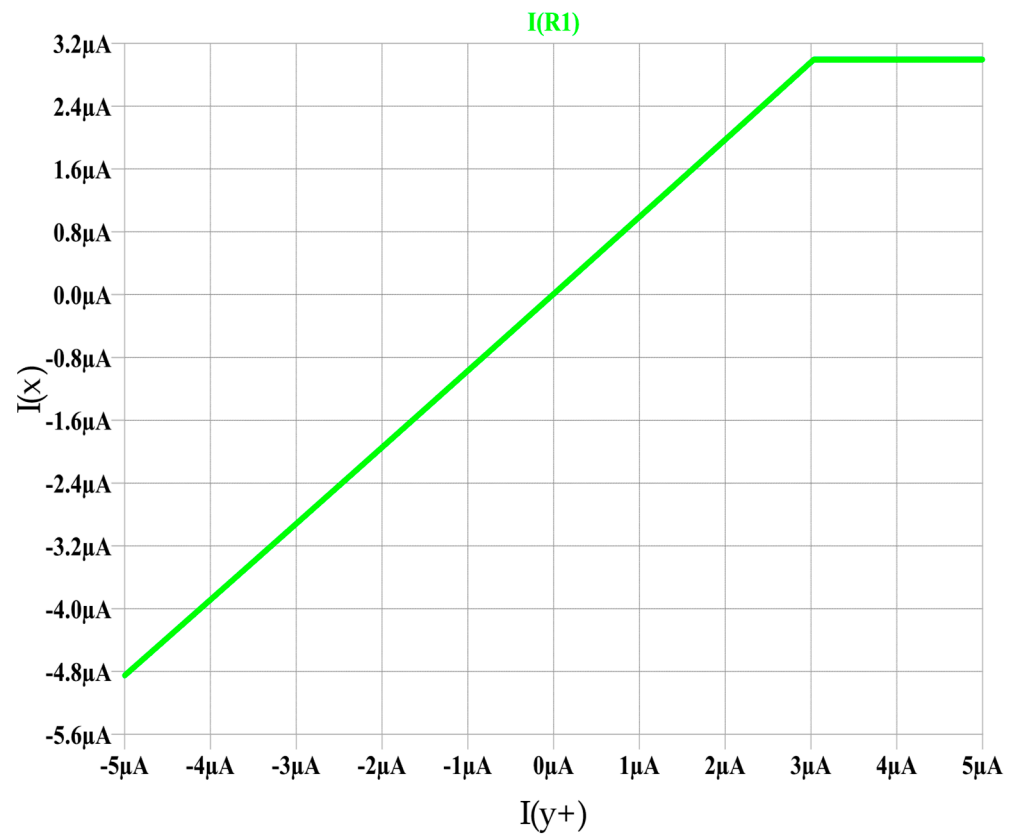


Figure 7. DC performances of the $\beta -$ parameter; $I(x)$ vs. $I(y+)$.

Frequency performances of the voltage conveyor are presented in Figure 8, Figure 9, and Figure 10, respectively. In detail, the α transfer function is reported in Figure 8 and was evaluated with a 3 pF load at the output Z terminal; the bandwidth is 20 MHz. The bandwidth for $\beta +$ and $\beta -$ is, respectively, 51 MHz and 53 MHz. Terminal impedances were also shown in Figures 11–14; the resulting impedance values are 3.7 M Ω at the X terminal, 90 Ω at the Y+ terminal, 600 Ω at the Y–, and 10.4 k Ω at Z (all impedances were evaluated at 1 a KHz frequency). All the reported parameters are summarized in Tables 2–4.

Table 2. Proposed dual Y VCII performance parameters.

Parameter	Low-Frequency Value	Bandwidth
α	0.99	20 MHz
$\beta -$	1	53 MHz
$\beta +$	1	51 MHz

Table 3. Parasitic parameters summary.

Parasitic Parameter	Value
C_X	20 fF
C_{Y+}	1.5 nF
L_{Y+}	6 nH
C_{Y-}	80 fF
L_{Y-}	10 μ H
C_Z	22 fF
L_Z	1 mH

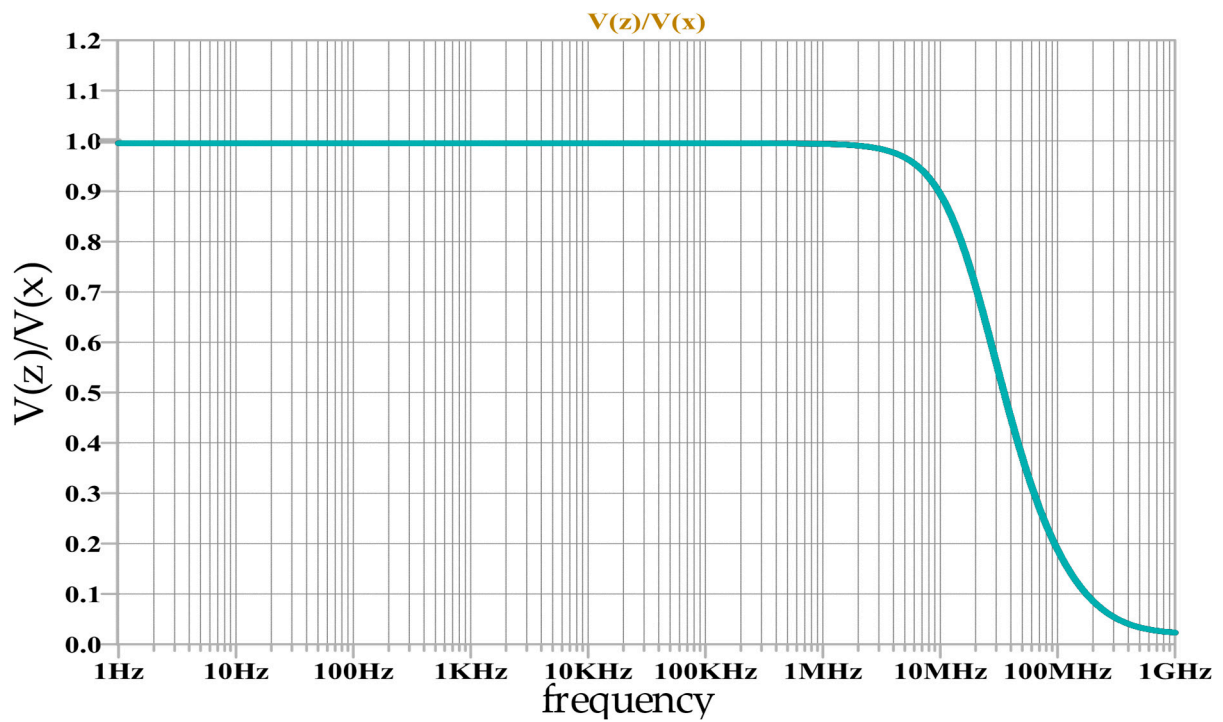


Figure 8. AC performances of the α parameter with a 3 pF capacitor connected to the Z node; $V(z)/V(x)$ vs. frequency.

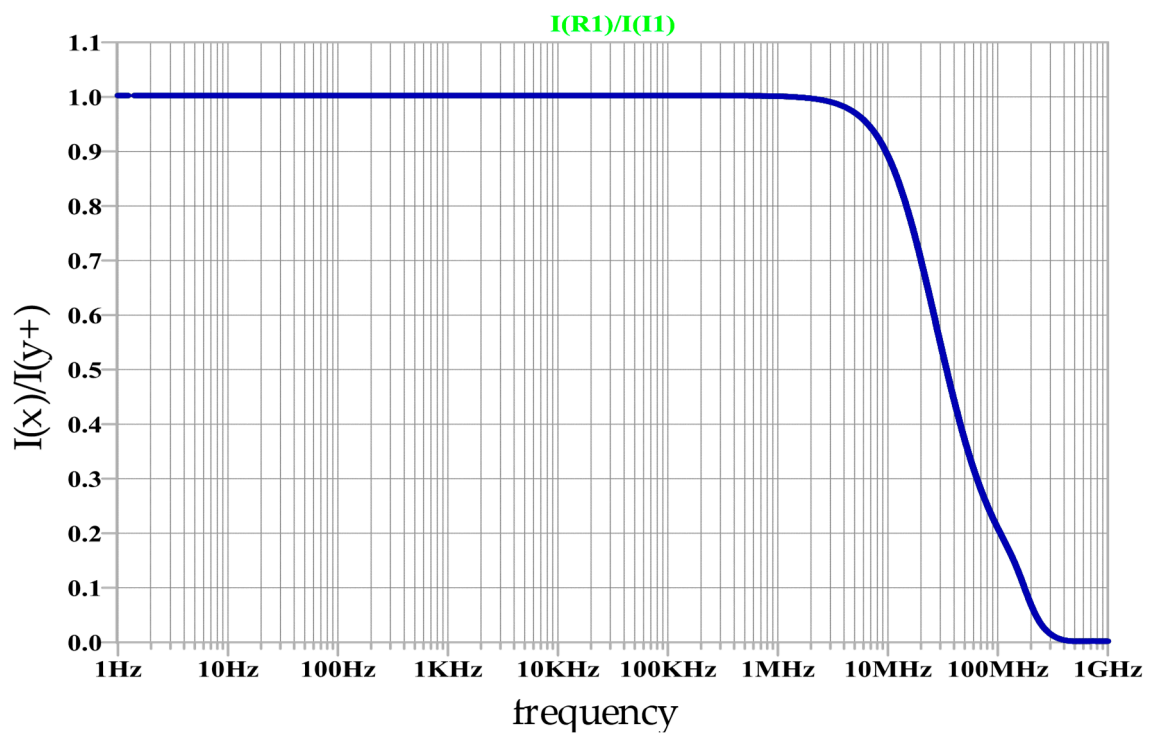


Figure 9. AC performances of the $\beta+$ parameter; $I(x)/I(y+)$ vs. frequency.

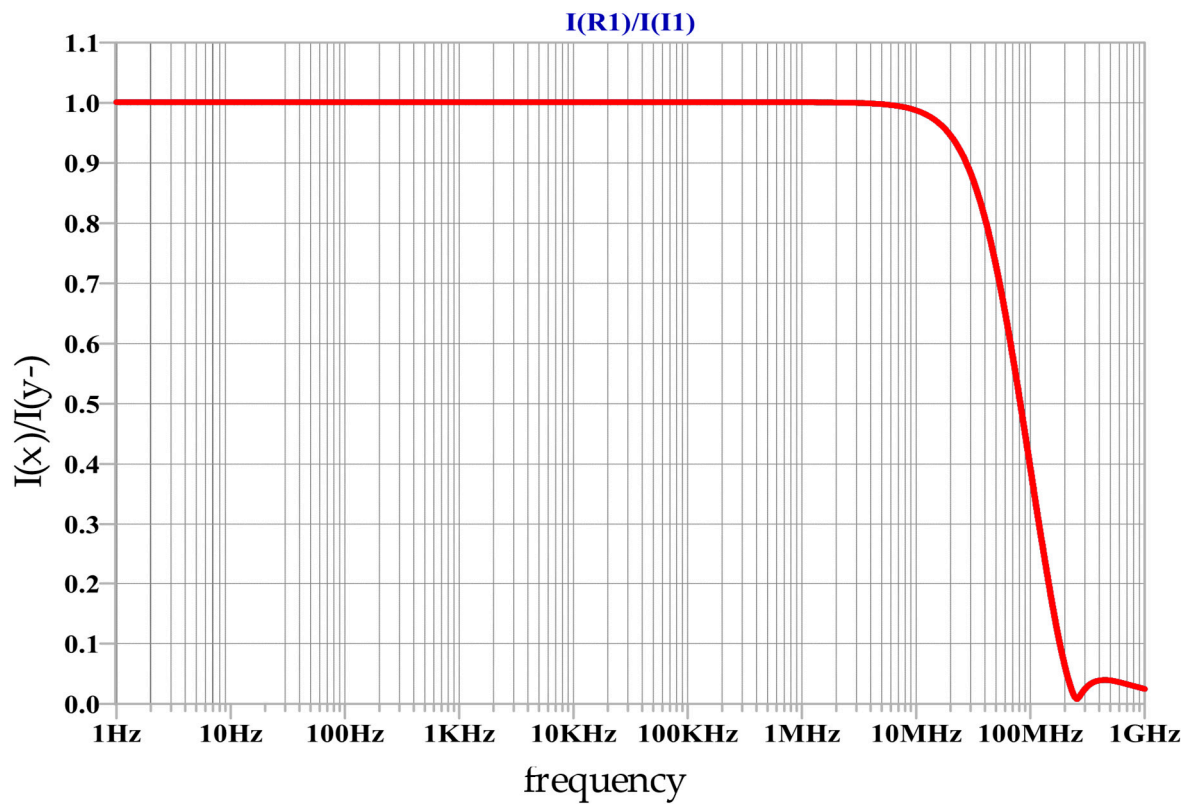


Figure 10. AC performances of the β - parameter; $I(x)/I(y-)$ vs. frequency.

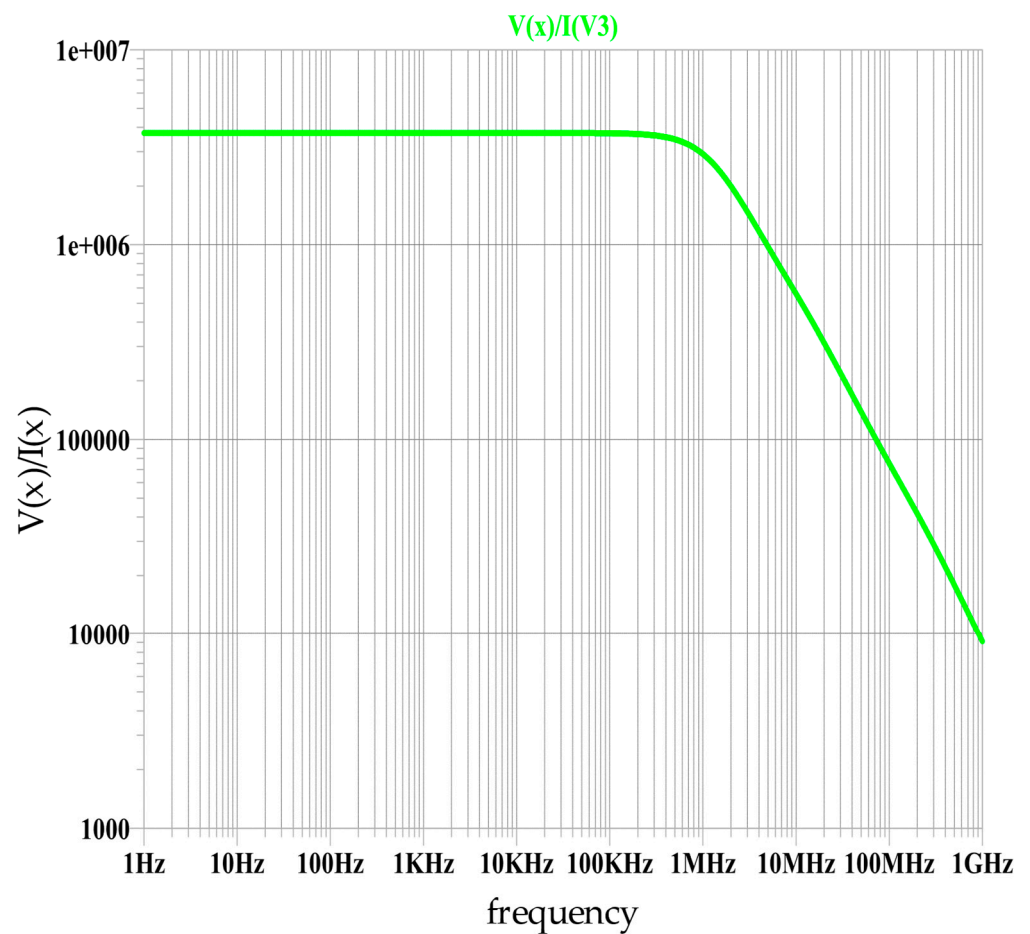


Figure 11. Proposed VCII X terminal impedance vs. frequency.

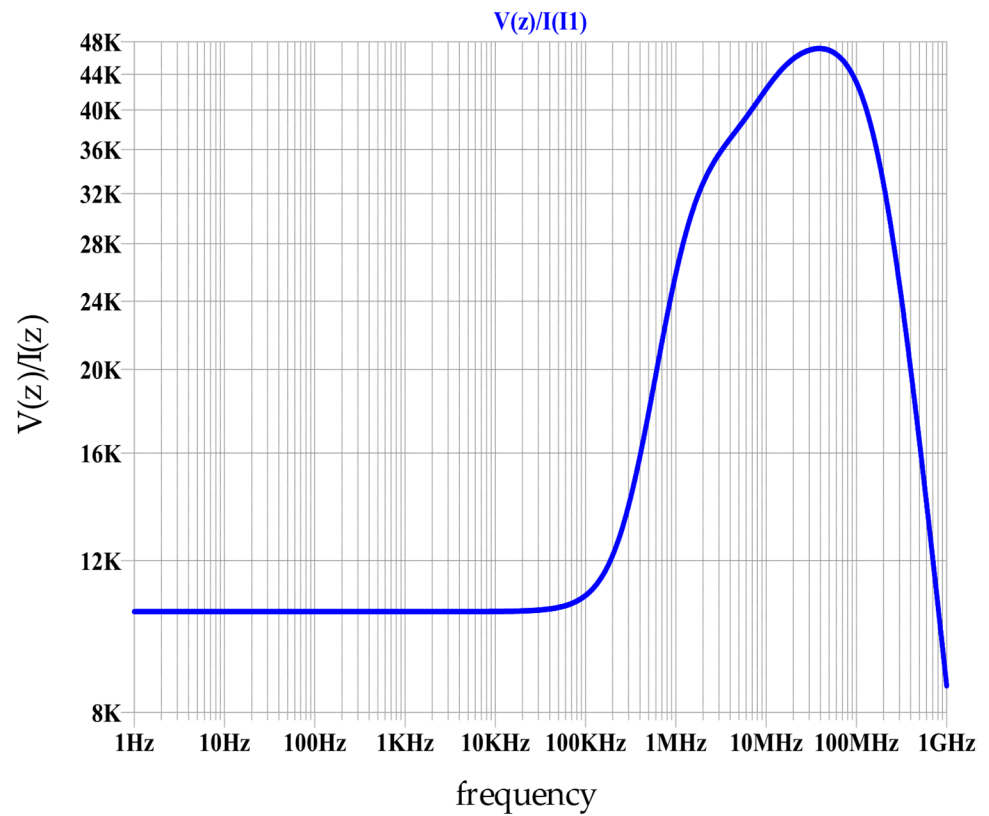


Figure 12. Proposed VCII Z terminal impedance vs. frequency.

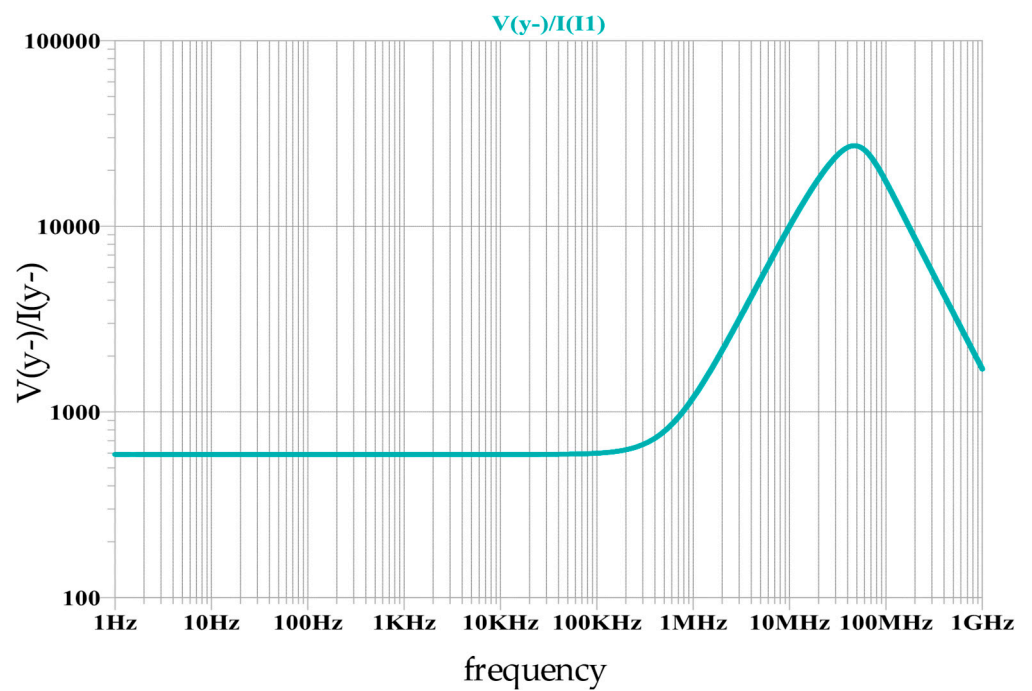


Figure 13. Proposed VCII Y-terminal impedance vs. frequency.

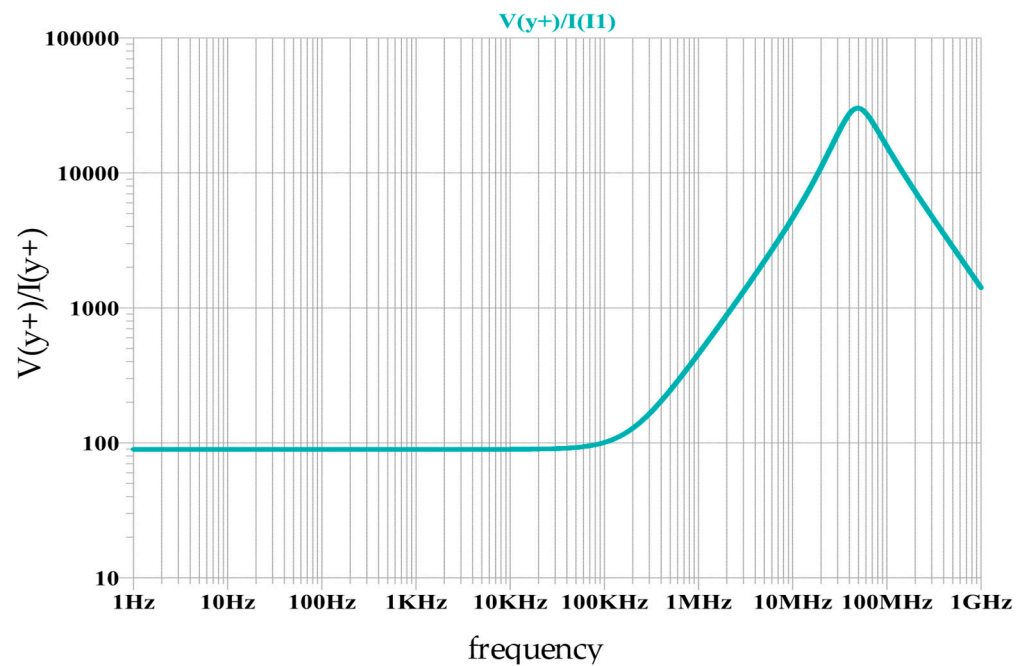


Figure 14. Proposed VCII Y+ terminal impedance vs. frequency.

Table 4. Low frequency impedance values of the proposed dual Y VCII.

Parasitic Parameter	Value
R_X	3.7 M Ω
R_Z	10.4 k Ω
R_{Y+}	90 Ω
R_{Y-}	600 Ω

The parasitic parameters of the proposed VCII were determined and reported in Table 3, considering a capacitance on terminal X, a capacitance and an inductance on the two terminals Y and Z. The terminal impedance values for low frequency are shown in Table 4. Finally, in Table 4 impedance values for low frequency are reported.

In Figures 15–21, the corner analyses on the main VCII parameters (α , $\beta+$, $\beta-$, X impedance, Z impedance, Y+ impedance, and Y– impedance, respectively) are reported.

The temperature sweep has been (–20 °C, 80 °C), while the supply voltage has been varied by $\pm 10\%$ from the nominal value. Montecarlo analysis has concerned the threshold voltages and oxide thickness of nMOS and pMOS transistors. In all the corner analyses performed, the variation in VCII parameters is low.

In Figure 22, LTspice simulations for a sample case are reported. Two current generators with input currents of 80 nA and 70 nA peak-to-peak and a 3 kHz frequency are used, connected to terminals Y+ and Y– of the VCII. The sum of the currents of the generators is evaluated on a gain resistor R_{GAIN} , placed on terminal X. The resulting conversion to voltage and the amplification by the resistor R_{GAIN} , chosen in this case to be 100 k Ω , is checked on the output terminal Z.

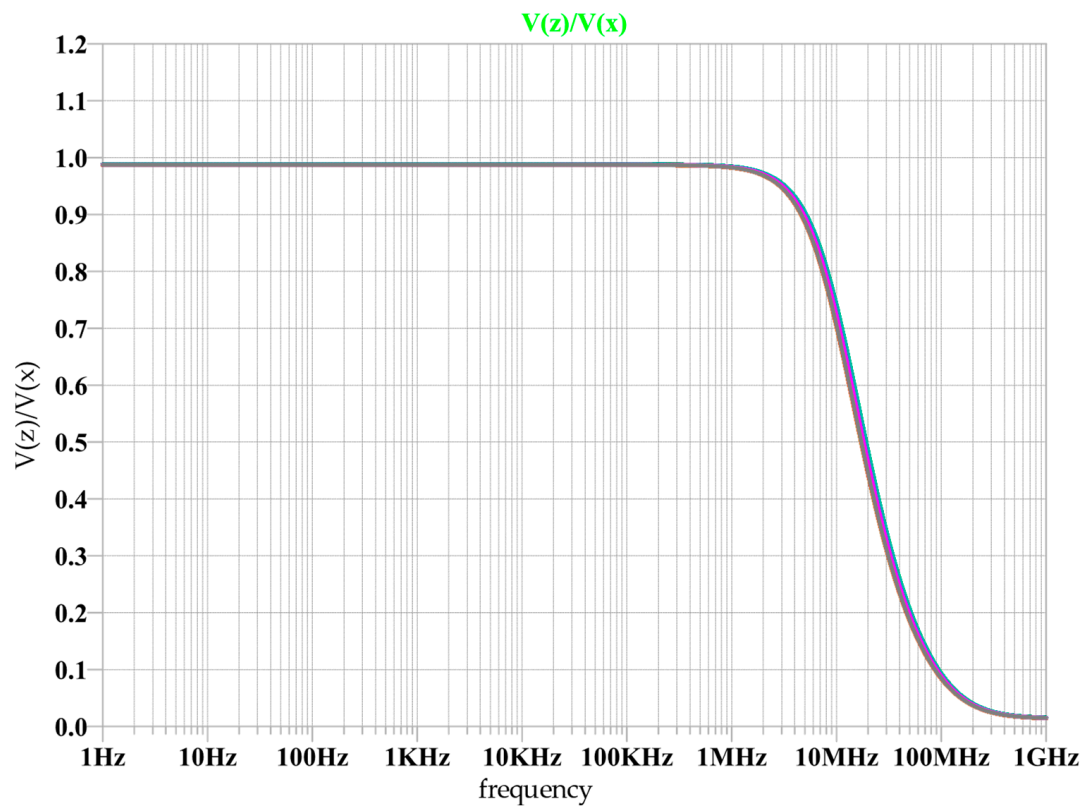


Figure 15. Corner analysis of AC performances of α parameter.

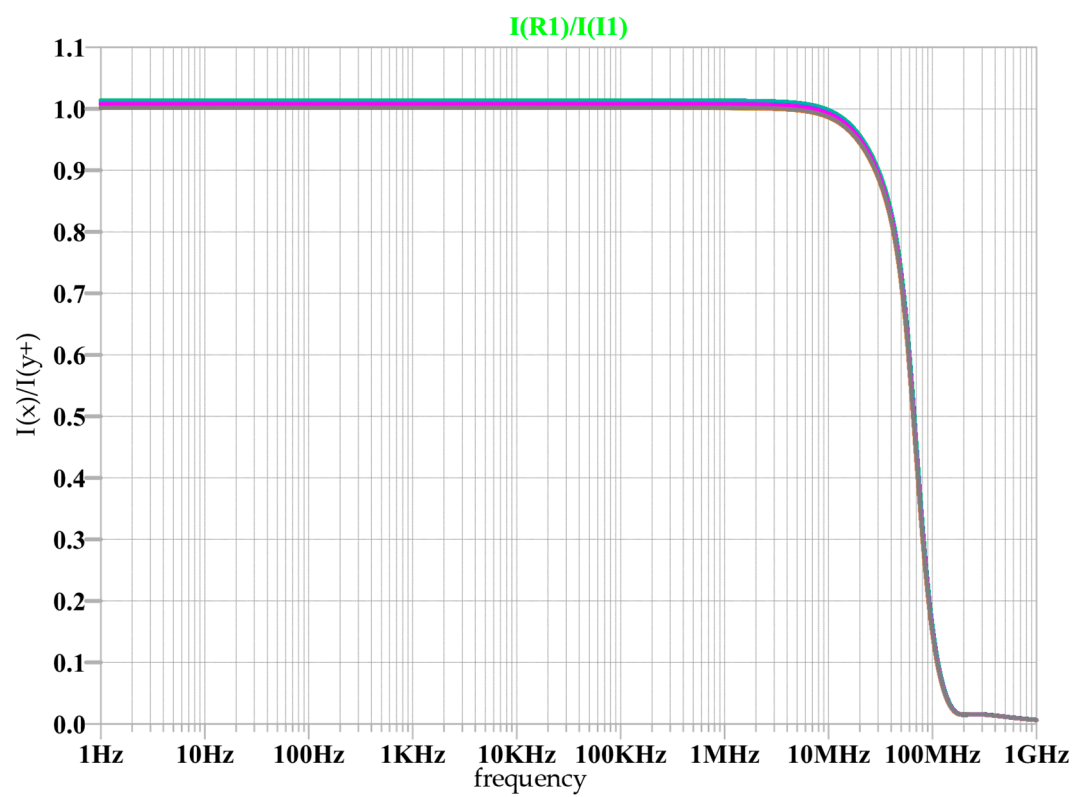


Figure 16. Corner analysis of AC performances of $\beta+$ parameter.

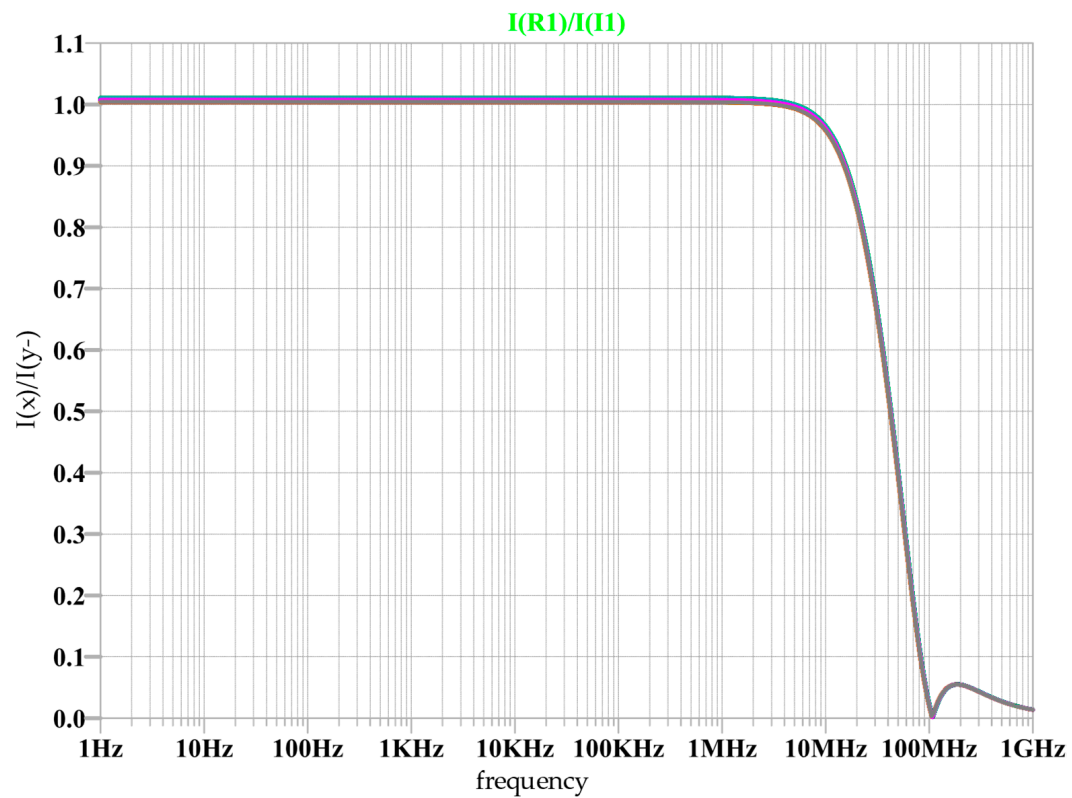


Figure 17. Corner analysis of AC performances of β – parameter.

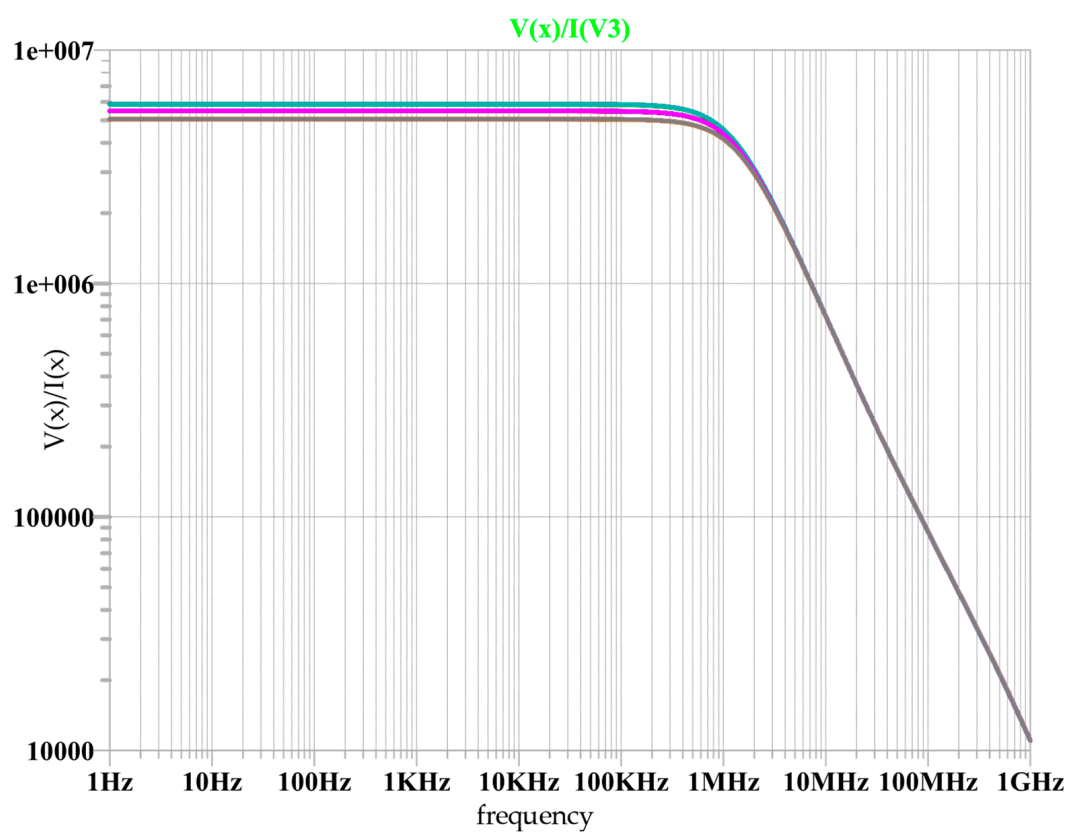


Figure 18. Corner analysis of the proposed VCII X terminal impedance.

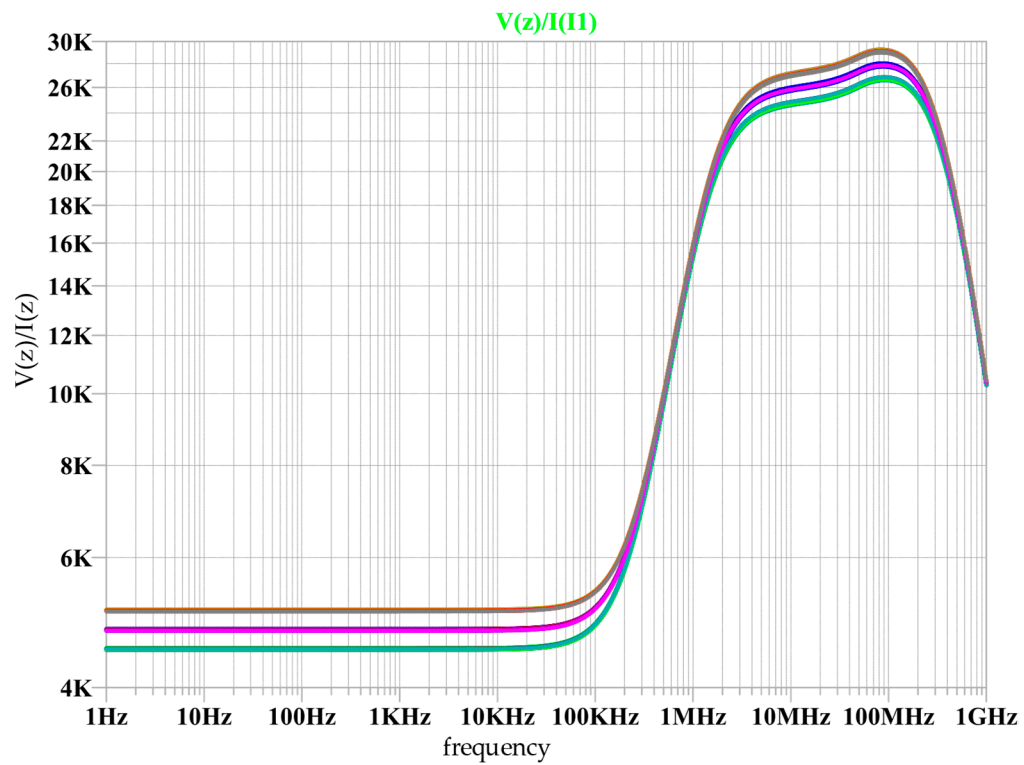


Figure 19. Corner analysis of the proposed VCII Z terminal impedance.

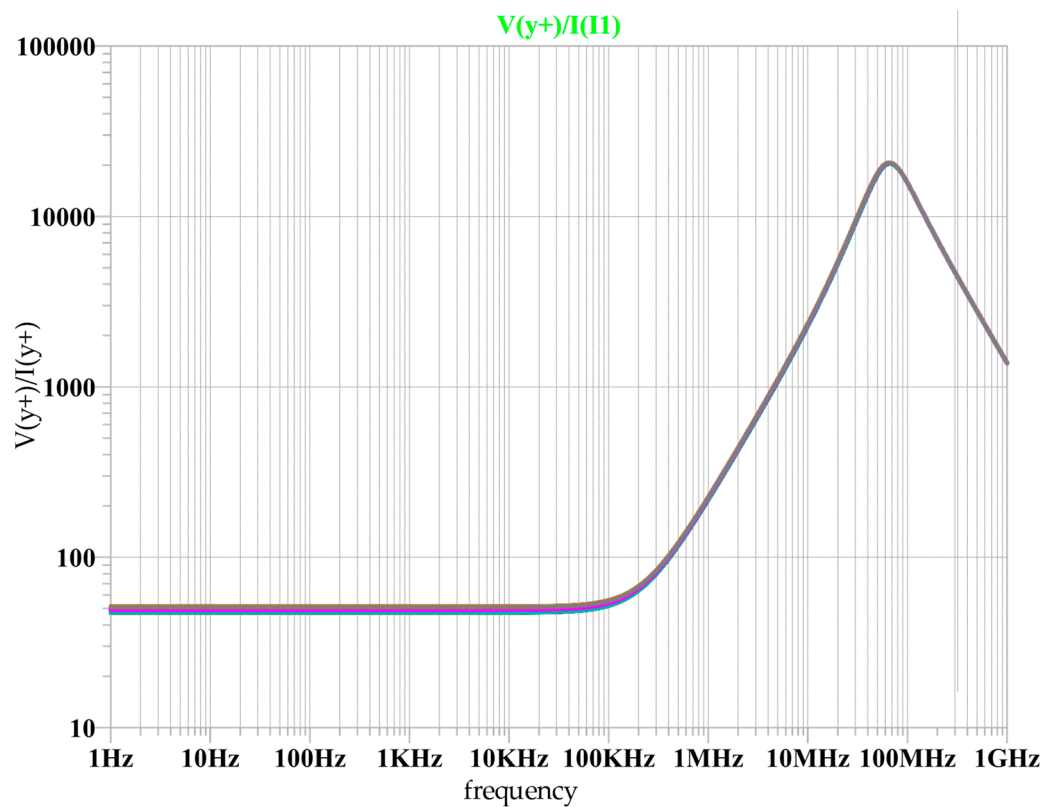


Figure 20. Corner analysis of the proposed VCII Y+ terminal impedance.

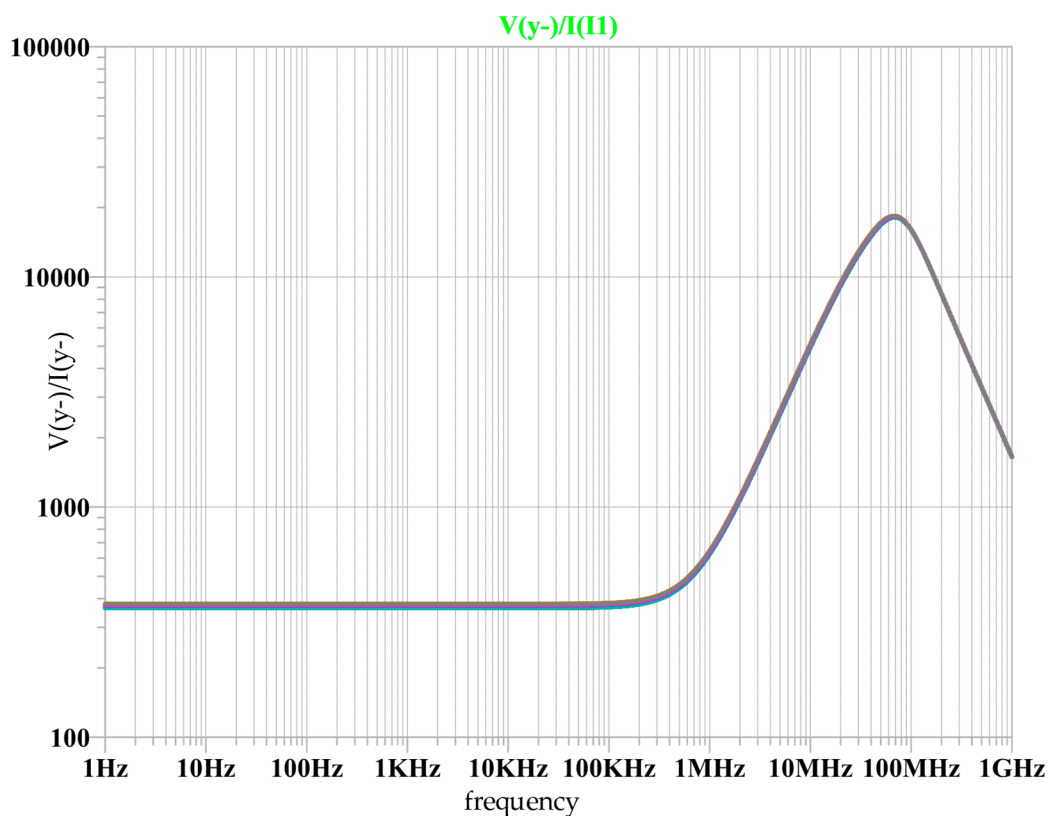


Figure 21. Corner analysis of the proposed VCII Y-terminal impedance.

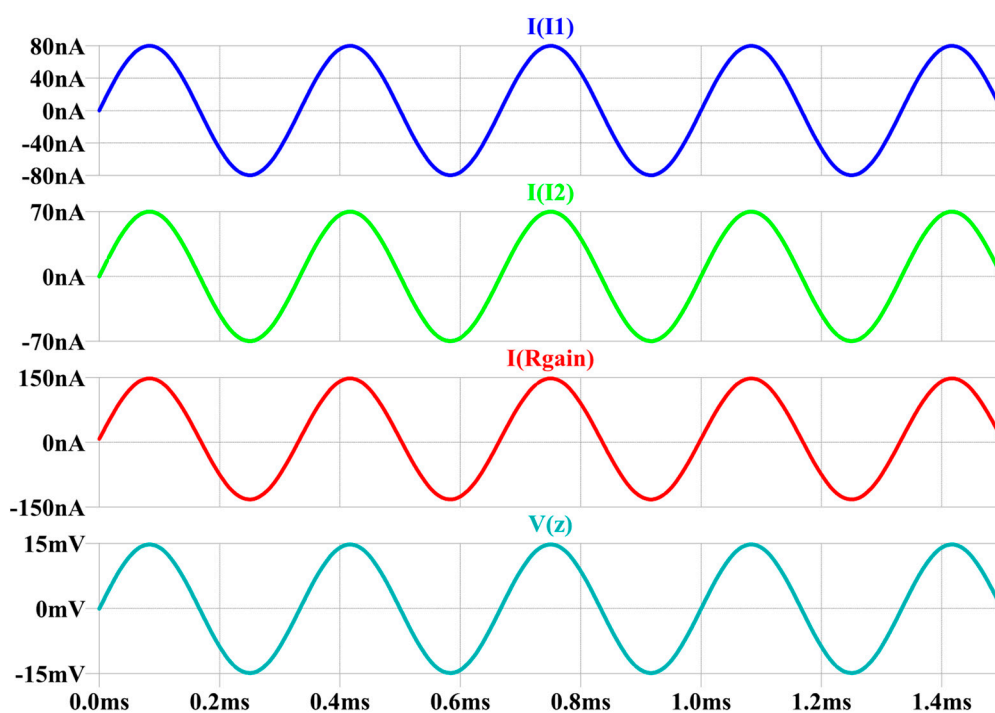


Figure 22. Summing operation of the proposed dual Y VCII.

The proposed circuit power consumption is about 24.6 μ W. This outcome highlights the circuit's suitability for low-power applications where energy efficiency is essential, like environmental monitoring systems and biomedical devices. The proposed solution can be used also as a floating dual-input amplifier or as a transimpedance amplifier (TIA).

5. Conclusions and Future Works

In applications such as power management systems, sensor array data, and environmental monitoring, where cumulative readings are helpful, this setup provides clear benefits. The proposed dual Y VCII can be successfully included in systems requiring precision and energy efficiency because of its low power consumption, high accuracy, and solid performance. Additionally, the summing capability of the VCII, demonstrated through simulations, highlights its potential to simplify circuit designs for aggregating current measurements. This novel technology is especially well-suited for applications like battery management systems, environmental pollution monitoring, and biomedical devices like glucose biosensors and EEG electrodes because in these applications it is usual to collect signals, for instance currents, from several sensors to monitor various parameters. In order to increase integration into modern electronic systems, future work may concentrate on further optimizing the circuit performance, such as increasing its bandwidth, lowering parasitic effects, and modifying the design for the newest CMOS technology.

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