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A CMOS Switched Capacitor Filter Based Potentiometric Readout Circuit for pH Sensing System

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Abstract: This work presents a potentiometric readout circuit for a pH-sensing system in an oral healthcare device. For in vivo applications, noise, area, and power consumption of the readout electronics play critical roles. While CMOS amplifiers are commonly used in readout circuits for these applications, their applicability is limited due to non-deterministic noises such as flicker and thermal noise. To address these challenges, the Correlated Double Sampler (CDS) topology is widely employed as a sampled-data circuit for potentiometric readout, effectively eliminating DC offset and drift, thereby reducing overall noise. Therefore, this work introduces a novel potentiometric readout circuit realized with CDS and a switched-capacitor-based low-pass filter (SC-LPF) to enhance the noise characteristic of overall circuit. The proposed readout circuit is implemented in an integrated circuit using 0.18 μm CMOS process, which occupies an area of $990 \mu\text{m} \times 216 \mu\text{m}$. To validate the circuit performances, simulations were conducted with a 5 pF load and a 1 MHz input clock. The readout circuit operates with a supply voltage range $\pm 1.65 \text{ V}$ and linearly reproduces the pH sensor output of $\pm 1.5 \text{ V}$. Noise measured with a 1 MHz sampling clock shows $0.683 \mu\text{V}_{\text{rms}}$, with a power consumption of $124.1 \mu\text{W}$.

Keywords: CDS; SC-LPF; potentiometric readout; CMOS; pH sensing



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1. Introduction

The accurate measurement of pH, which quantifies the acidity or alkalinity of a substance, is a fundamental analytical technique with widespread applications across various fields, including biomedicine, chemistry, agriculture, and environmental monitoring. In biomedical applications, pH measurement is critical for assessing physiological conditions such as metabolic processes, body fluid composition, and the early detection of diseases [1–13]. For example, the regulation of oral pH plays a pivotal role in maintaining oral health, as fluctuations in pH can influence the onset of dental decay, gum diseases, and other oral infections. Elevated acid levels in the mouth, often caused by sugar consumption, lead to a pH drop below 5.5, initiating demineralization of the enamel and contributing to tooth erosion and cavity formation. Over time, persistent oral pH imbalances can exacerbate conditions such as periodontitis, xerostomia, and even systemic diseases like cardiovascular issues induced by oral inflammation [9,10].

The conventional method for pH measurement in electrochemical sensing is potentiometry, which operates by detecting the potential difference between a reference electrode and an indicator electrode. Among the most widely employed potentiometric sensors, glass electrodes offer a high degree of accuracy and linearity. However, these electrodes are bulky and unsuitable for in vivo applications, particularly in clinical or wearable devices, due to their large size and fragility [11–13]. An alternative to glass electrodes is the Ion Selective Field Effect Transistor (ISFET), which has gained attention due to its compact size, high sensitivity, and suitability for miniaturization. The ISFET sensor consists of a Metal Oxide Semiconductor Field Effect Transistor (MOSFET) configuration, where the gate is modified with an ion-selective membrane that responds to pH changes in the solution [14–17]. Changes in pH induce variations in the gate potential, which, in turn, modulate the current between the source and drain terminals, enabling the conversion of pH into an electrical signal. Despite significant advancements in ISFET technology, the integration of ISFETs with analog front-end circuits presents several challenges, particularly for in vivo applications. The main difficulties lie in optimizing the noise performance, minimizing power consumption, and achieving compactness in the design. In vivo pH-sensing applications, such as continuous oral health monitoring, require the balancing of these factors while ensuring that the circuit remains small and power efficient. Traditional analog front-end circuits for potentiometric sensors often suffer from high power consumption and large noise levels, particularly due to the intrinsic “1/f noise” (flicker noise) associated with CMOS transistors at low frequencies [18–29]. Given that pH sensors typically operate in the low-frequency range, managing noise becomes a critical aspect of ensuring accurate and reliable measurements.

This paper addresses the challenges associated with ISFET-based pH sensing by proposing a novel analog front-end circuit design that minimizes noise, reduces power consumption, and ensures miniaturization. The circuit incorporates advanced compensation techniques, including a switched-capacitor low-pass filter (SC-LPF) and a Correlated Double Sampler (CDS), to improve noise performance and mitigate issues related to drift and offset. These innovations allow for accurate, low-noise pH measurements, making the circuit suitable for real-time, in vivo oral healthcare applications.

The rest of this paper is organized into the following sections. Section 2 explains the proposed design of CDS with the SC-LPF built in 0.18 μm CMOS process for the pH-sensing system. Section 3 describes the post layout simulated results of circuit compared with other existing architectures. Section 4 concludes the proposed architecture presented in this work.

2. Design of Readout Circuit

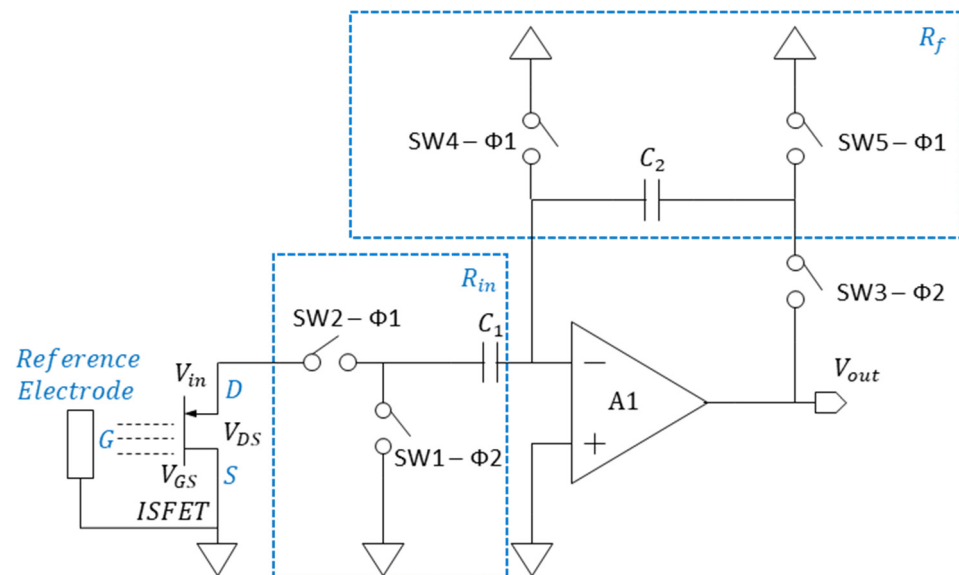
The aim of this work is to build a potentiometric readout circuit with low noise and low power consumption that can convert the output of an ideal ISFET pH sensor, which has a sensitivity of 59.16 mV/pH according to the Nernst equation with an output voltage range of ± 414 mV [30–32], or an ISFET pH sensor beyond the Nernst equation, with a sensitivity up to 200 mV/pH and a maximum output voltage range of ± 1.5 V [33–35]. The Magnachip 0.18 μm CMOS process is chosen to design the readout circuit because of its attractive features such as accurate and stable results with temperature changes, easy offset correction, rail-to-rail output, and linear voltage changes. In this work, the design of the potentiometric readout for pH sensing is accomplished in following two stages to conduct a comprehensive analysis: (a) CDS and (b) CDS followed by SC-LPF. Table 1 presents a list of abbreviations and symbols for the reader’s convenience.

Table 1. List of important abbreviations and symbols.

Symbol	Abbreviation
CDS	Correlated double sampler
SC-LPF	Switched-capacitor low-pass filter
$S_{ntotal}(f)$	OPAMP noise spectral density
V_{in}^2	Input voltage noise
V_{cds}^2	Output noise of CDS
$V_{sc_lpf}^2$	Output noise of CDS with SC-LPF
$H_{cds}(f)$	Transfer function of CDS
$H_{sc_lpf}(f)$	Transfer function of CDS with SC-LPF
f_1	Cutoff frequency of CDS
f_{2SC_LPF}	Cutoff frequency of CDS with SC-LPF
V_{in}	Input voltage of overall system
V_{out}	Output voltage of overall system
R_{in}	Input resistor
R_f	Feedback resistor

2.1. CMOS Correlated Double Sampler

A pH-sensing system using an ISFET is typically a 3-electrode system with source, drain, and gate electrodes of ISFET, as depicted in Figure 1. The reference electrode is the gate of ISFET, which is separated from the silicon dioxide, needed to establish a stable potential. Reference electrodes help to eliminate potential drifts caused by the solution itself and allow for accurate pH sensing. When the ISFET is exposed to a solution with a specific pH, the surface potential of the sensitive gate changes, altering the threshold voltage V_{th} of the ISFET, thereby changing the drain current flowing through the transistor. The voltage difference between the ISFET drain and the reference electrode is amplified by an operational amplifier (OPAMP), effectively eliminating common-mode noise and providing a high-sensitivity output signal directly proportional to the pH change.

**Figure 1.** Implementation of the CDS circuit.

The dominant noise sources in modern CMOS architectures are thermal noise and flicker noise. In CMOS transistors, thermal noise is created by the drain current fluctuations caused by a random motion of charge carriers, while flicker noise arises from the trapping of

charges as they move from source to drain of the transistor. The voltage spectra of thermal and flicker in CMOS transistors are given by Equation (1) and (2), respectively [36–39].

$$\frac{V_{th}^2}{\Delta f} = \frac{4KT\gamma}{g_m} \quad (1)$$

$$\frac{V_f^2}{\Delta f} = \frac{K_f}{C_{ox}WLf} \quad (2)$$

where K is the Boltzmann constant 1.38×10^{-23} J/K, γ is $2/3$, T is the absolute temperature in degrees Kelvin, g_m is the transconductance of the transistor, K_f is the flicker noise coefficient, which depends on the technology, C_{ox} is the gate oxide capacitance per unit area, W and L are the transistor gate width and length, respectively, f is the operating frequency, and Δf is the small bandwidth at the frequency of f . The input voltage noise spectral density increases significantly as frequency decreases below the corner frequency, which may range anywhere between a few Hz and several hundred Hz. Generally, potentiometric sensors operate at low frequencies where flicker noise is dominant. Thus, to reduce the noise of the potentiometric readout circuit, the CDS circuit is widely embarked in the process of digitizing the potentiometric sensor output [36–38].

The CDS circuit architecture consists of an input resistor (R_{in}) and a feedback resistor (R_f) designed with resistor emulators instead of passive resistors, as illustrated in Figure 1. The resistor emulators are built using a switched capacitor circuit where the switches are realized with transmission gates. Since the circuit operates at low frequency and considering that integrable capacitances are typically on the order of a few pF, the resulting resistances would range from hundreds of $K\Omega$ to $M\Omega$, making the implementation with switched capacitor circuits essential. The operation of the switched capacitor in the CDS circuit includes two steps: sampling and integration, i.e., the signal generated by the sensor (V_{in}) can be sampled in a capacitor and then amplified with the help of an OPAMP which is ‘A1’. Utilizing two non-overlapping clocks ($\Phi1$ and $\Phi2$), the signal is sampled and stored in the capacitor. When $\Phi2$ is high, the switch ‘SW1’ transfers the charge stored in the C_1 to C_2 and ‘A1’ allows the charge to be transferred to the output without loading. Meanwhile, when $\Phi1$ is high, the C_2 is discharged and prepared for the next sample transfer, while the C_1 charges.

Figure 2 illustrates the implementation of the resistor emulator circuit at the input sampling stage and the feedback stage, respectively. The resistor emulator circuit at the input sampling stage consists of ‘SW1’, ‘SW2’, and C_1 . The ON resistance of the designed switch is $10\text{ m}\Omega$. The value of the C_1 in the resistor emulator circuit is chosen based on the charge transfer rate, which is the switching frequency (f_{sw}) of the resistor emulator circuit [40]. The f_{sw} of the resistor emulator is set to 1 MHz . Based on the V_{in} and the value of C_1 , a charge (q_{in}) stored in the C_1 is given by Equation (3). The charge transfer occurs at f_{sw} , and the rate of charge transfer per unit time (I_{in}) is given by Equation (4). Thus, an equivalent R_{in} of the resistor emulator circuit in Figure 2a can be described as Equation (5), using Equations (3) and (4).

$$q_{in} = C_1 \times V_{in} \quad (3)$$

$$I_{in} = q_{in} \times f_{sw} \quad (4)$$

$$R_{in} = \frac{V_{in}}{I_{in}} = \frac{V_{in}}{q_{in} \times f_{sw}} = \frac{1}{C_1 \times f_{sw}} \quad (5)$$

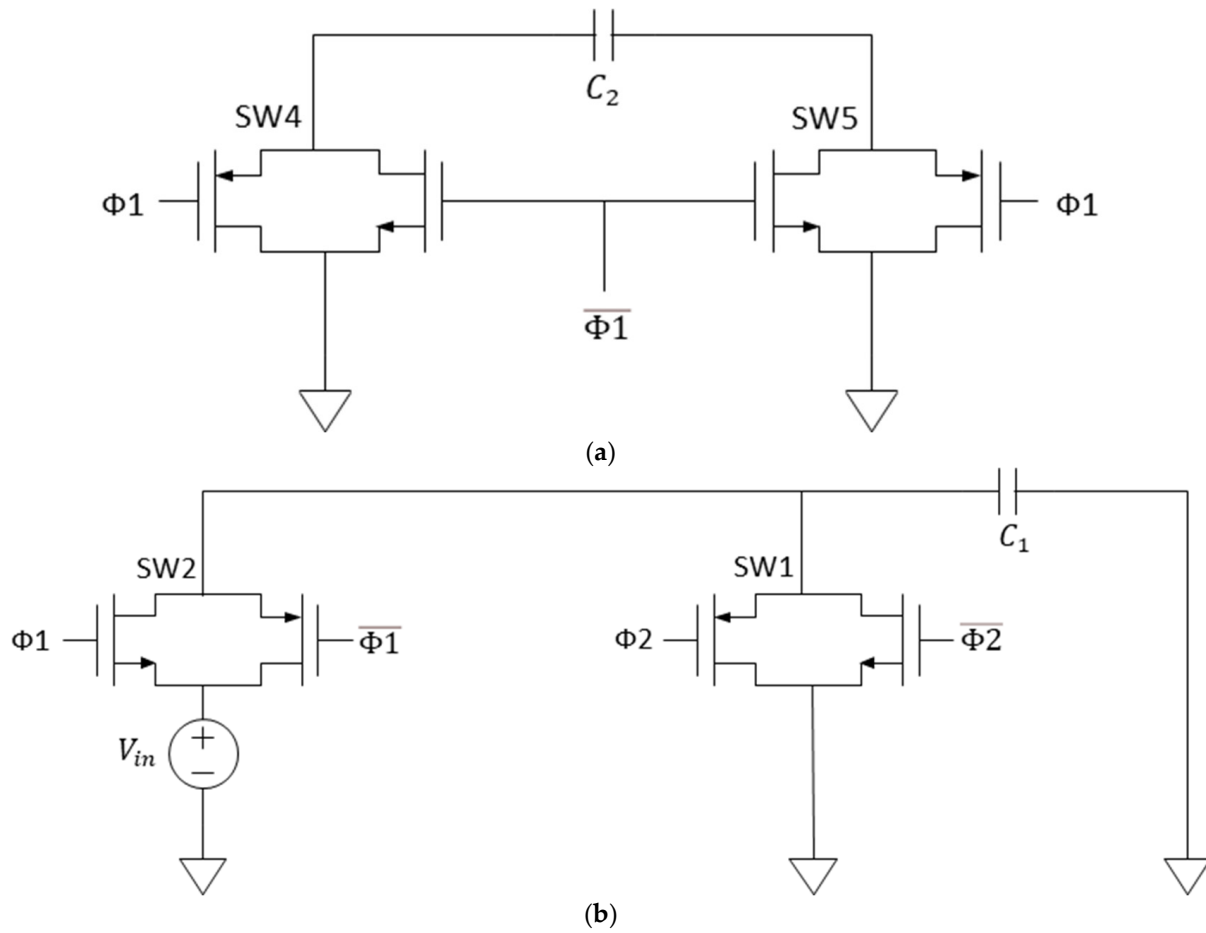


Figure 2. (a) Implementation of the resistor emulator for input sampling stage; (b) implementation of the resistor emulator for feedback stage.

The OPAMP ‘A1’ requires high gain while ensuring low power consumption and low noise. Therefore, a two-stage CMOS telescopic OPAMP using a cascode configuration is selected to meet these requirements, as in Figure 3. The two-stage OPAMP consists of a differential amplifier and a common source amplifier stage. For the pH-sensing application, the OPAMP is configured with unity gain feedback and a unity gain bandwidth of 20 MHz. The sensor bias current (I_{ds}) is 25 μ A and bias voltage (V_{ds}) is 0.3 mV.

The current noise generated by the input transistor NM1 can be calculated by Equation (6), and the corresponding voltage noise is derived as per Equation (7) [36,39].

$$\frac{i_{d1}^2}{\Delta f} = 4KT\gamma g_{mn1} + \frac{K_f}{C_{ox}W_{n1}L_{n1}f} \times g_{mn1}^2 \quad (6)$$

$$\frac{V_{d1}^2}{\Delta f} = \frac{4KT\gamma}{g_{mn1}} + \frac{K_f}{C_{ox}W_{n1}L_{n1}f} \quad (7)$$

In the telescopic OPAMP, a differential stage consists of an input NMOS transistor pair (NM1, NM2) and a load PMOS transistor pair (PM1, PM2). The bulk of all PMOS transistors are connected to VDD, and all NMOS transistors are connected to VSS. Since the pH readout is performed at relatively lower frequency or DC, the cascode device contributes negligible noise, leaving NM1–NM2 and PM1–PM2 as the primary flicker noise sources [41]. The aspect ratio of NM1–NM2 is chosen as 5 μ /1 μ and the aspect ratio of PM1–PM2 is chosen as 18 μ /1 μ . The common source amplifier stage has NMOS aspect ratio as 2.5 μ /1 μ and

PMOS aspect ratio as $35 \mu/1 \mu$. A sampling time of 20 ns is used, with a compensation capacitor (C_c) of 1 pF. By increasing the size of input NMOS transistor pair and reducing the size of load PMOS transistor pair in the differential stage, flicker noise generated by OPAMP can be reduced. The noise voltage in the signal path of the telescopic OPAMP can be represented as in Equation (8) [41].

$$S_{ntotal}(f) = 4KT \left(\frac{2\gamma}{g_{mn1,2}} + \frac{2\gamma g_{mp1,2}}{g_{mn1,2}^2} \right) + \frac{2K_f}{C_{ox}(W_n L_n)_{1,2} f} + \frac{2K_f}{C_{ox}(W_p L_p)_{1,2} f} \frac{g_{mp1,2}^2}{g_{mn1,2}^2} \quad (8)$$

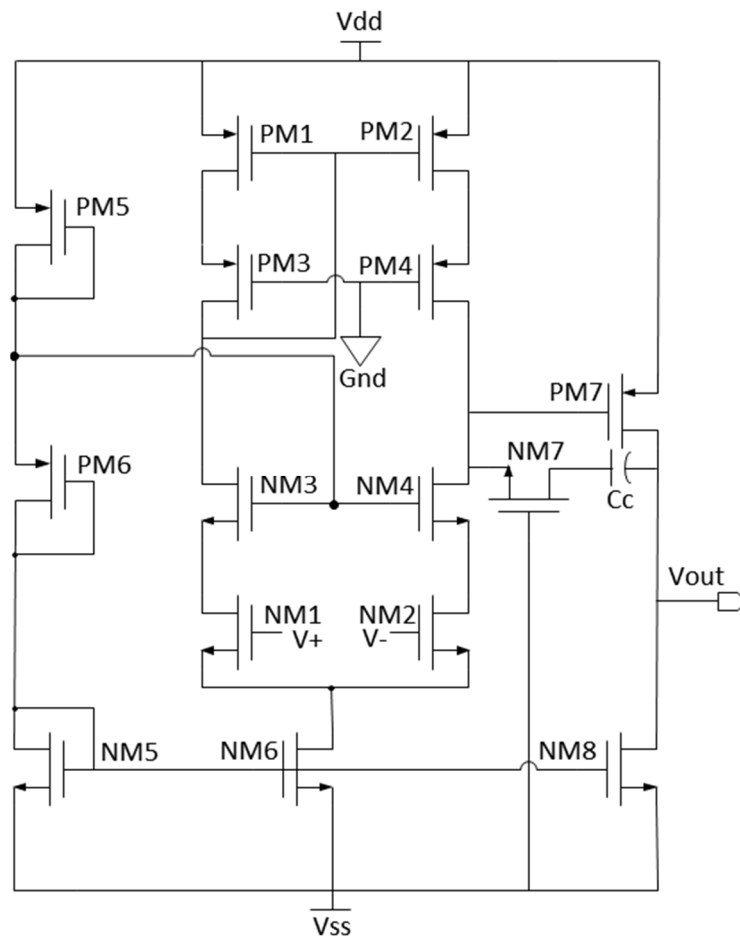


Figure 3. Telescopic OPAMP architecture.

Here, the $S_{ntotal}(f)$ is the total noise of the OPAMP including the thermal noise and the flicker noise. It can be seen that the thermal noise parameters are independent of frequency, whereas the flicker noise decreases as frequency increases. At lower frequencies, the flicker noise dominates the white noise; thus, the noise power spectral density of the two-stage OPAMP can be simplified to Equation (9). When this OPAMP is used in the closed-loop configuration shown in Figure 1, the flicker noise can be derived as Equation (10), where R_{in} and R_f determine the closed-loop gain of the OPAMP.

$$S_{nflicker}(f) = \frac{2K_f}{C_{ox} f} \left(\frac{1}{(W_n L_n)_{1,2}} + \frac{1}{(W_p L_p)_{1,2}} \frac{g_{mp1,2}^2}{g_{mn1,2}^2} \right) \quad (9)$$

$$V_{nflicker}^2 = \left(\frac{R_f}{R_{in}} \right)^2 \frac{2K_f}{C_{ox} f} \left(\frac{1}{(W_n L_n)_{1,2}} + \frac{1}{(W_p L_p)_{1,2}} \frac{g_{mp1,2}^2}{g_{mn1,2}^2} \right) \quad (10)$$

The designed OPAMP achieves an open-loop gain of 110 dB, a unity gain bandwidth of 20 MHz, and a power consumption of 44 μ W with a ± 1.65 V power supply. Figure 4a elucidates the frequency response of the OPAMP with a load capacitance of 1 pF. The DC response captured in Figure 4b is conducted in unity gain mode by shorting the inverting terminal with output and sweeping the voltage at the non-inverting terminal from -1.5 V to $+1.5$ V. It achieves an output swing of -1.5 V to $+1.5$ V. To measure the noise of the OPAMP, all the AC input voltages are set to ground potential and the Root Mean Square (RMS) noise is measured at the output of OPAMP. Noise performance of the OPAMP is shown in Figure 4c and by integrating the noise over the frequency range of 1 Hz to 20 MHz, the calculated RMS output noise of the OPAMP is 233 μ V_{rms}.

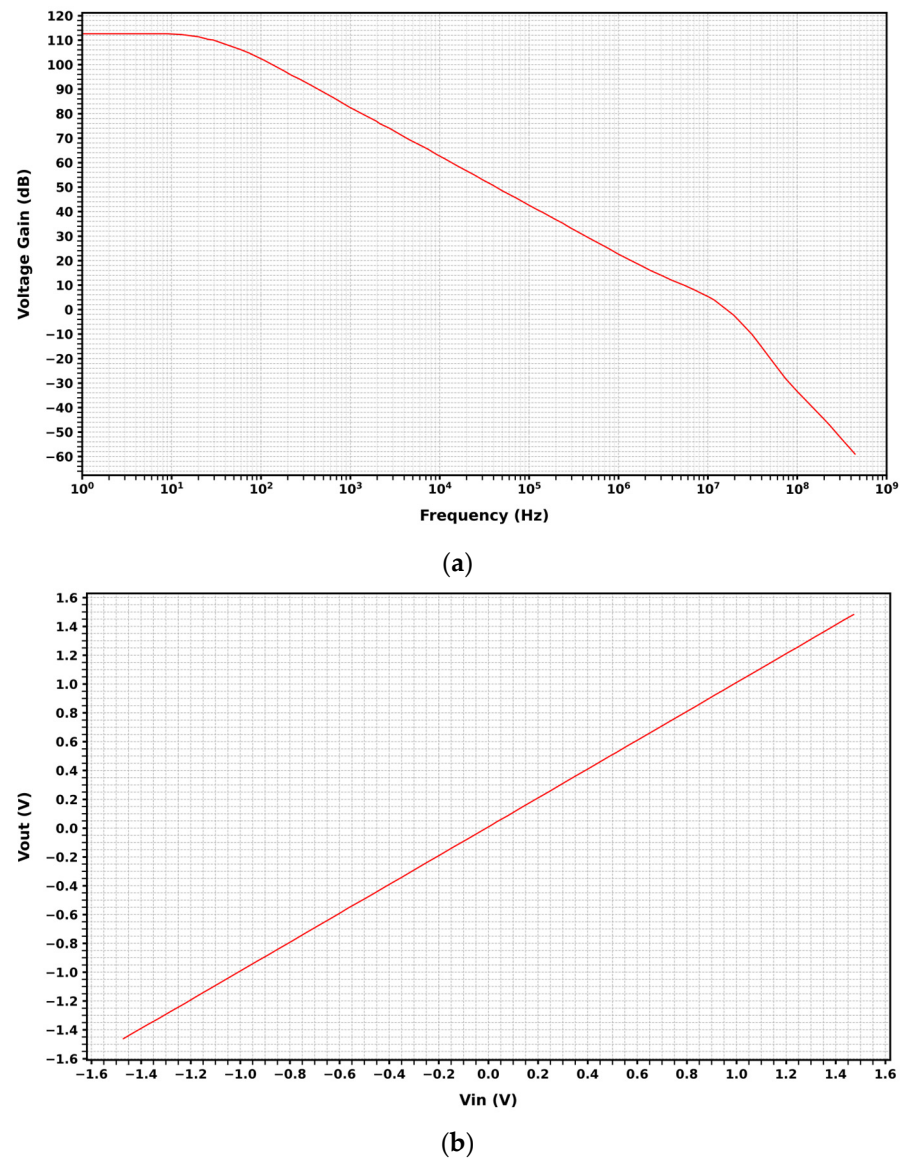


Figure 4. Cont.

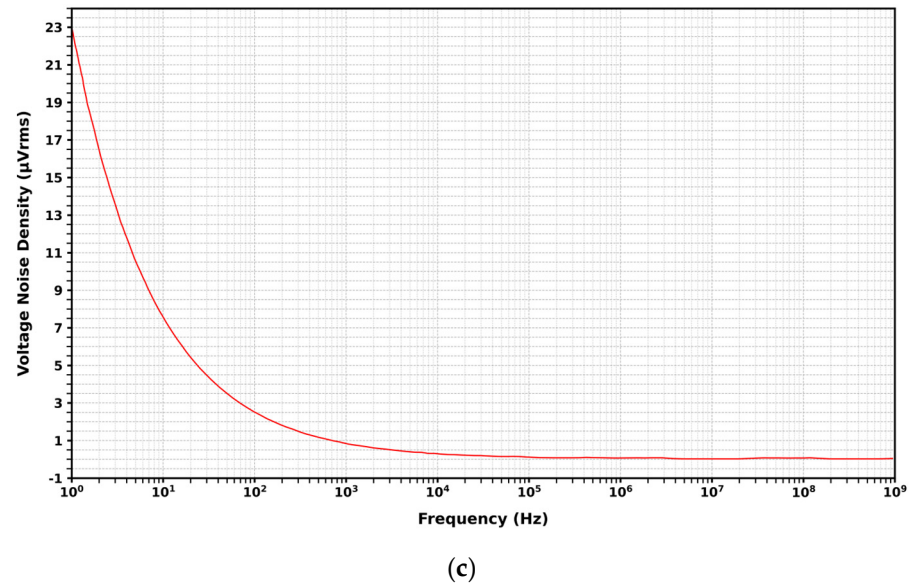


Figure 4. (a) AC response of OPAMP, voltage gain (dB) versus frequency (Hz); (b) DC response of OPAMP, V_{in} (V) versus V_{out} (V); (c) Noise analysis of OPAMP, noise (μV_{rms}) versus frequency (Hz).

2.2. CMOS Correlated Double Sampler Followed by Switched Capacitor LPF

An anti-aliasing filter, or smoothing filter, is often employed at the CDS output to remove the high frequency noise and provide a smoother signal by removing the short-term fluctuations. The filtering stage can be either a continuous time filter (conventional LPF) or a discrete time filter (switched capacitor LPF). Generally, the conventional LPF limits the noise reduction of the CDS stage, as the noise from the transistors in the signal path of the conventional LPF circuit will always appear at the output, degrading the circuit's performance since the output data is continuous in this architecture. To further reduce the noise, a CDS with SC-LPF method is proposed, as demonstrated in Figure 5.

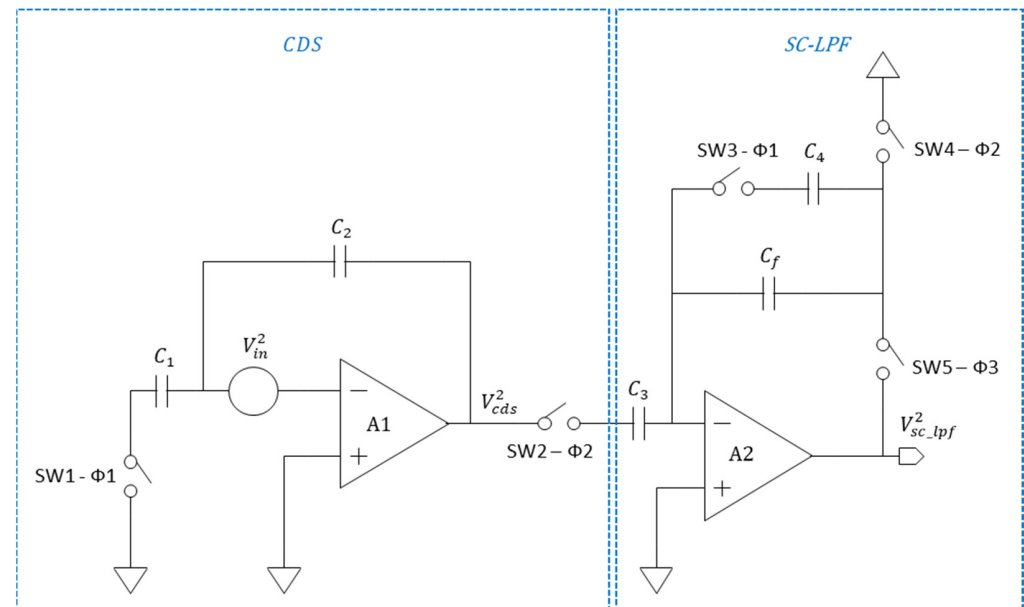


Figure 5. Design of CDS circuit with SC-LPF.

When $\Phi 1$ is high, 'SW1' transfers the charge stored in C_1 to C_2 . When $\Phi 2$ is high, 'SW2' at the output of the first stage samples the data to the input of the SC-LPF. $\Phi 3$ samples the data to the output. OPAMP design of 'A2' is identical to 'A1'. The feedback network in

SC-LPF is designed with the resistor emulator circuit instead of a passive resistor, which is in parallel with the C_f (filtering capacitor). This design makes the output data and noise discrete. In Figure 5, V_{in}^2 represents the input voltage noise of the CDS generated by 'A1'. V_{cds}^2 and $V_{sc_lpf}^2$ are the output noise of the CDS and the overall system, respectively. The transfer function of the first stage ($H_{cds}(f)$) with a—3 dB cutoff frequency (f_1) is given by Equation (11) [36]. This will be passed to the SC-LPF stage with a—3 dB cutoff frequency (f_{2SC_LPF}), and the overall transfer function of CDS with SC-LPF ($H_{sc_lpf}(f)$) is represented in Equation (12).

$$|H_{cds}(f)|^2 = \left| \frac{2}{\frac{0.3f_1}{f} + 1} \right|^2 \quad (11)$$

$$|H_{sc_lpf}(f)|^2 = \left| \frac{A_0}{\frac{jf}{0.3f_{2SC_LPF}} + 1} \right|^2 \quad (12)$$

where A_0 is the DC gain of the SC-LPF, f_1 is chosen as the frequency of interest based on the sensor output frequency which ranges between few Hz to 500 Hz, and f_{2SC_LPF} is chosen as 1 kHz. Integrating the $H_{sc_lpf}(f)$ with the noise generated by the CDS stage (V_{cds}^2) in Equation (13) would result in the overall noise of the system ($V_{sc_lpf}^2$) as per Equation (14), which indicates the final noise generated by the closed-loop system.

$$V_{cds}^2 = |H_{cds}(f)|^2 \times V_{in}^2 = \left| \frac{2}{\frac{0.3f_1}{f} + 1} \right|^2 \times V_{in}^2 \quad (13)$$

$$V_{sc_lpf}^2 = |H_{sc_lpf}(f)|^2 \times V_{cds}^2 = \left(\frac{C_l}{C_f} \right)^2 \frac{K_f}{C_{ox}WLf} \left(\frac{2 \left(\frac{f}{0.3f_1 + f} \right)}{\sqrt{1 + \left(\frac{f}{0.3f_{2SC_LPF}} \right)^2}} \right)^2 \quad (14)$$

The C_f acts as the sampler and filter for the CDS system, reducing the noise of the system compromising the bandwidth. The noise spectrum density equation clearly indicates that the system noise can be drastically reduced by the implementation of CDS with SC-LPF and by carefully choosing the C_f and f_{2SC_LPF} .

3. Results and Discussion

The proposed potentiometric readout circuit is fabricated in Magnachip 0.18 μm CMOS technology [42]. Cadence Virtuoso (Cadence Design Systems, San Jose, CA, USA) is employed to design the schematic and layout. The design rule check and post layout parasitic RC extraction are performed using Cadence Assura. Figure 6 shows the layout of full chip, where the proposed CDS with SC-LPF architecture is highlighted in yellow. The layout of the CDS with SC-LPF architecture occupies an area of 990 $\mu\text{m} \times 216 \mu\text{m}$. The chip operates at a power supply of ± 1.65 V. The utilized fabrication process supports six metal layers for an interconnection and pad with size of 67 $\mu\text{m} \times 67 \mu\text{m}$. The post layout simulation is carried out by using a 1 MHz clock with a sampling capacitor of 1 pF and a load capacitor of 5 pF. The input voltage range used for the simulation is from -1.5 V to $+1.5$ V, which is the pH sensor output.

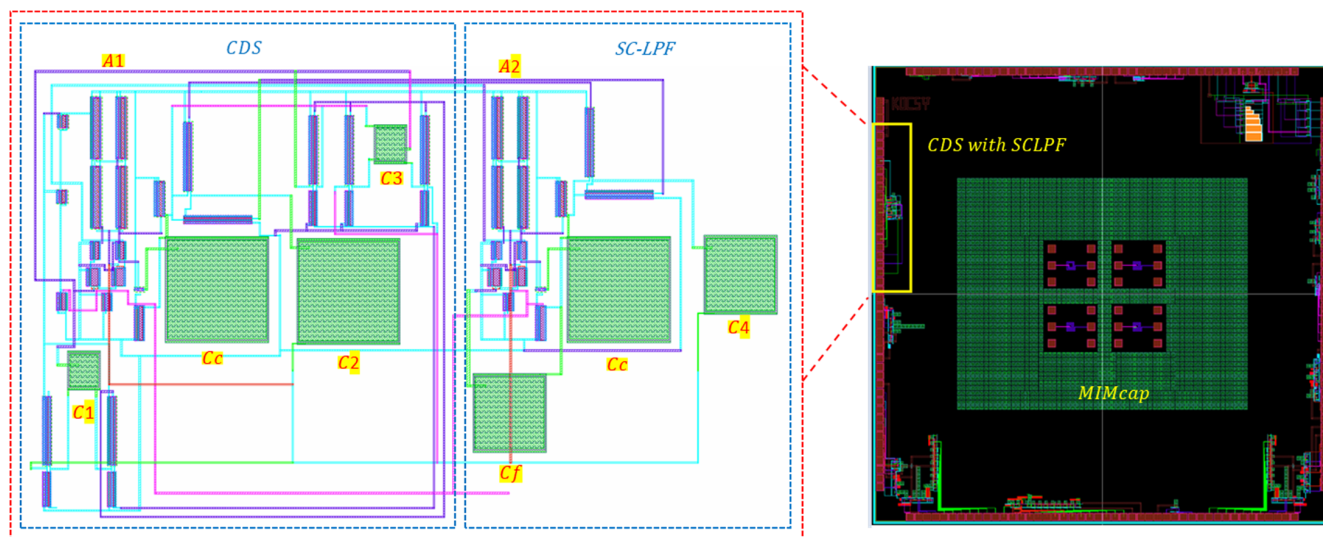


Figure 6. Full chip layout highlighting the proposed CDS with SC-LPF architecture.

Figure 7 depicts the transient response of the CDS stage when an input voltage of 1 V is applied, with a 1 MHz sampling clock frequency and a load capacitance of 5 pF. The transient response of the designed CDS is shown when it is configured with unity gain. The X-axis of the graph represents the time in units of μs , and the Y-axis corresponds to the CDS stage output voltage in units of volts. It can be seen from Figure 7 that the output voltage of the CDS circuit follow the applied input voltage, indicating that CDS circuit is acting as a potentiometric readout. The settling time of CDS output voltage depends on the value of switched capacitor in the CDS.

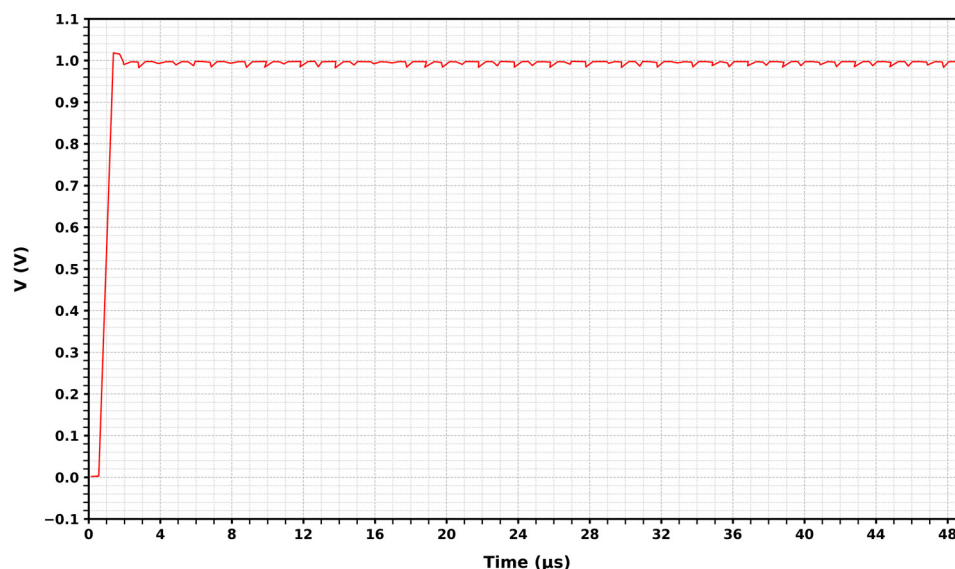


Figure 7. Transient response at the CDS output for input voltage of 1 V with 1 MHz clock and 5 pF load.

The transient response of the designed CDS with SC-LPF is presented in Figure 8. For the simulation, an input voltage (V_{in}) of 1 V is applied with a sampling frequency of 1 MHz and 5 pF load capacitance, and the output voltage of the CDS with SC-LPF stage (V_{out}) is measured. Three clocks (Φ_1 , Φ_2 , and Φ_3) are used to simulate the proposed circuit, operating at 1 MHz frequency with a duty cycle ratio of 20%, 70%, and 5%, respectively. These clocks are intended to be supplied externally using a microcontroller.

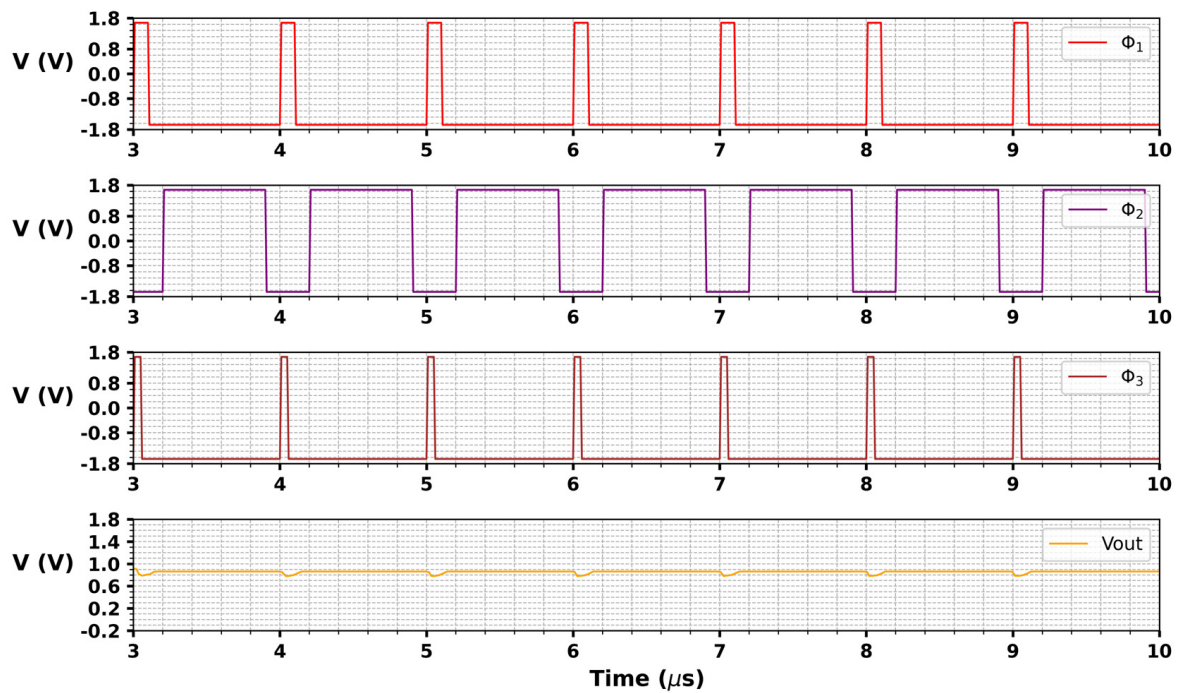


Figure 8. Transient response at the CDS and SC-LPF output for input voltage of 1 V with 1 MHz clock and 5 pF load.

The X-axis in Figure 8 represents the time in units of μs and the Y-axis is voltage in volts. As expected, V_{out} of the CDS with SC-LPF stage is following the V_{in} , which behaves as the potentiometric readout. The glitches at V_{out} is caused by the switching action of Φ_3 , that samples V_{out} . Similarly, the transient response of CDS and CDS with SC-LPF are evaluated using additional input voltages, including 500 mV, -500 mV, -1 V, 1.5 V, and -1.5 V, for verification purposes.

Figure 9 illustrates the noise response of designed CDS stage and CDS followed by SC-LPF during the circuit simulation. To measure the noise, all the AC input voltages are set to ground potential, and the RMS noise is measured at the output of each stage. The X-axis of the graphs corresponds to frequency in Hz, while the Y-axis represents noise in $\text{V}/\sqrt{\text{Hz}}$. The flicker noise dominates the thermal noise at lower frequencies, and the flicker noise gradually dies out, leaving a constant thermal noise at the higher frequencies. By integrating the noise over the frequency range of 10 Hz to 100 MHz, the RMS output noises of CDS circuit and CDS followed by SC-LPF are $1.49 \mu\text{V}_{rms}$ and $0.70 \mu\text{V}_{rms}$, with a power consumption of $60 \mu\text{W}$ and $124 \mu\text{W}$, respectively.

The post-extraction simulation is performed to measure overall DC swing of the proposed CDS with SC-LPF architecture, as captured in Figure 10a, where the X-axis and Y-axis represent V_{in} and V_{out} in volts, respectively. In the simulation, V_{in} is swept in 50 mV steps from -1.5 V to $+1.5$ V, and the corresponding V_{out} is measured. Figure 10a shows that the V_{out} of the CDS with SC-LPF follows V_{in} ranged from -1.5 V to $+1.5$ V when a 1 MHz sampling clock and a 5 pF load are used. This demonstrates that the designed potentiometric readout circuit can linearly reproduce the pH sensor response in the range ± 1.5 V. The figure further illustrates the deviation of the measured results from the ideal fitting line. Analysis of the linearity curve reveals that the error rate remains below 2.5% for the target DC swing. The overall frequency response of the CDS with SC-LPF system is shown in Figure 10b, which indicates a 3 dB pole frequency at 2.25 MHz. Here, the X-axis and Y-axis represent frequency in Hz and voltage gain in dB, respectively.

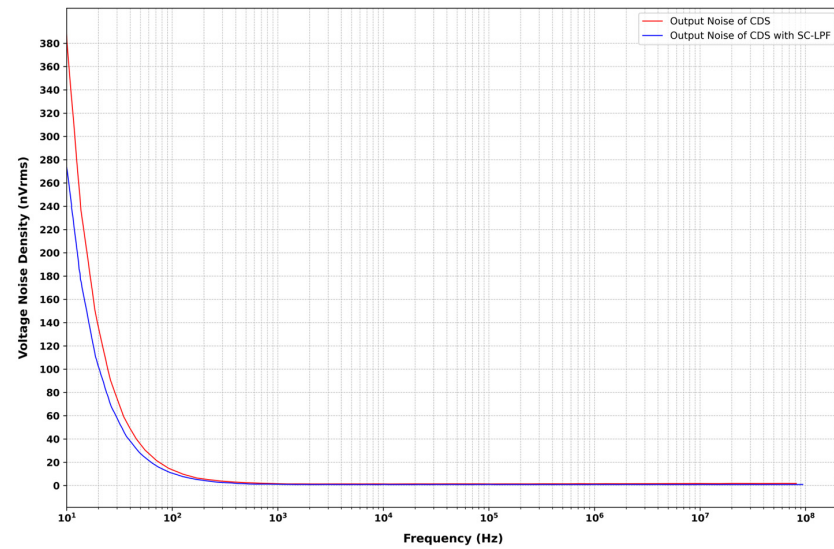
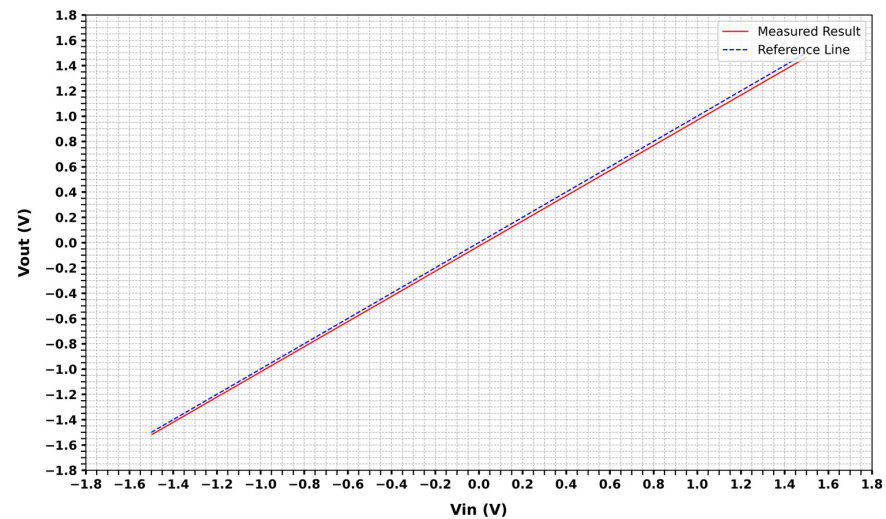
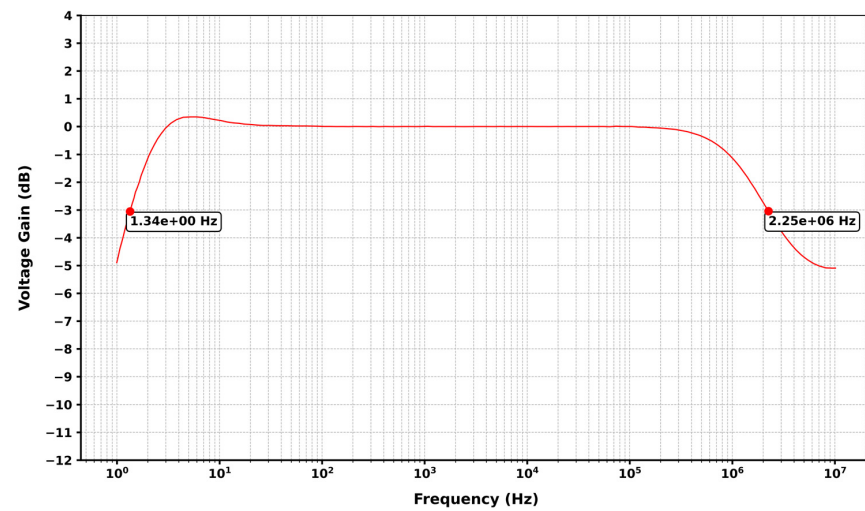


Figure 9. Output noise performance of CDS and CDS with SC-LPF at pre-layout circuit simulation, noise (V_{rms}) versus frequency (Hz).



(a)



(b)

Figure 10. Post extraction simulation of the overall system (a) V_{in} versus V_{out} linearity plot; (b) frequency response.

Table 2 presents a comparison of noise and power consumption from post layout simulation of all architectures that are discussed in this paper. The two-stage telescopic OPAMP architecture achieved a noise of $260.8 \mu V_{rms}$, which is significant. By implementing the CDS circuit with the OPAMP, the noise is reduced to a significantly lower value of $1.4 \mu V_{rms}$. The noise is further reduced to $0.683 \mu V_{rms}$ by implementing the novel SC-LPF at the CDS output.

Table 2. Post layout simulation results of various architectures.

Parameter	OPAMP	CDS	CDS with SC-LPF
Output noise (V_{rms})	260.8 μ	1.4 μ	0.683 μ
Power consumption (Watt)	44.1 μ	70.7 μ	124.1 μ

To comprehensively assess the system's performance under varying environmental conditions, corner simulations are performed at temperatures of -40°C , 27°C , and 80°C , covering a range of process variations SS, FF, FS, SF (slow–slow, fast–fast, fast–slow, slow–fast), and voltage fluctuations of $\pm 1.55\text{ V}$, $\pm 1.65\text{ V}$, and $\pm 1.85\text{ V}$. The results, including key metrics such as DC swing, noise performance, and power consumption for the different architectures, are summarized in Table 3, offering valuable insights into the system's resilience under different operating scenarios.

A comparison of the proposed readout circuit with other existing architectures is summarized in Table 4. A switched-capacitor-based transimpedance amplifier, operating at a sampling frequency of 100 kHz with a 3 V supply, has been proposed for low noise and power consumption, where the input transistors are biased in the weak inversion region to minimize both power and noise [25]. However, the performance of transistors in the weak inversion region can be sensitive to fabrication process variations, which may lead to increased chip fabrication costs. In pH-sensing applications, recent potentiometric readouts that employ the constant voltage constant current (CVCC) method [24], low-noise DC-coupled sensor amplifiers [23], and dual-sensing CMOS arrays [27] exhibit high power consumption, rendering them unsuitable for in vivo applications. Many of the other architectures are characterized by high power consumption, large spatial requirements, and significant noise generation [26,28]. In contrast, the proposed readout circuit offers a superior balance of noise performance, power efficiency, and compactness, making it a more viable option for in vivo pH-sensing systems, as detailed in Table 4.

Table 3. Post layout corner simulation results.

Parameter	Temperature (°C)			Corner Frequency				Supply Voltage (V)		
	−40	27	80	SS	FF	FS	SF	−1.55 to +1.55	−1.65 to +1.65	−1.85 to +1.85
Opamp DC swing (V)	−1.5 to +1.49	−1.5 to +1.47	−1.5 to +1.5	−1.5 to +1.49	−1.5 to +1.48	−1.5 to +1.5	−1.5 to +1.5	−1.5 to +1.49	−1.5 to +1.48	−1.5 to +1.5
Opamp noise (μV_{rms})	236.8	260.8	282.5	308.8	200.9	296.6	246	290.7	260.8	207.1
Opamp power (μW)	24.32	44.1	61.13	19.71	83.6	33.29	56.7	25.14	44.1	85.65
CDS DC swing (V)	−1.5 to +1.5	−1.5 to +1.5	−1.5 to +1.5	−1.5 to +1.5	−1.5 to +1.5	−1.5 to +1.5	−1.5 to +1.5	−1.5 to +1.5	−1.5 to +1.5	−1.5 to +1.5
CDS noise (μV_{rms})	1.45	1.4	1.87	1.2	1.23	1.22	1.21	1.29	1.39	1.41
CDS power (μW)	40.15	70.7	96.8	32.6	130.4	53.7	90.6	40.6	70.7	135.3
CDS with SC-LPF DC swing (V)	−1.5 to +1.5	−1.5 to +1.5	−1.5 to +1.5	−1.5 to +1.5	−1.5 to +1.5	−1.5 to +1.5	−1.5 to +1.5	−1.5 to +1.5	−1.5 to +1.5	−1.5 to +1.5
CDS with SC-LPF noise (μV_{rms})	0.56	0.68	0.77	0.70	0.67	0.67	0.69	0.67	0.68	0.74
CDS with SC-LPF power (μW)	71.15	124.1	170.73	57.22	232	94.9	159.1	72	124	286.34

Table 4. Architecture comparison of proposed readout circuit with existing methodologies.

Ref	Power (Watt)	Noise (V_{rms})	Area (mm^2)	Supply (V)	Technology (μm)	Application
[23]	900 μ	991.1 μ	N/A	1	CMOS 0.18	pH sensing
[24]	1.67 m	N/A	N/A	3.3 & 1.8	CMOS 0.18	pH sensing
[25]	15.17 μ	2.89 μ	N/A	3	CMOS 0.18	ECG
[26]	397.92 μ	N/A	0.44	1.5	CMOS 0.18	Uric acid sensing
[27]	3.43 m	114 μ	0.31	1.8	CMOS 0.18	pH sensing
[28]	1.67 m	N/A	1.44	1.8	CMOS 0.18	Multi-purpose
[29]	6.6 μ	26.89 μ	N/A	1.8	CMOS 0.18	Capacitive sensing
[43]	3 m	1.22 m	4	3.3	CMOS 0.35	pH sensing
[44]	7.98 m	6.57 m	3.4	3.3 & 1.8	CMOS 0.18	pH sensing
[45]	240 m	N/A	4	1.8	CMOS 0.18	pH sensing
This work	124.1 μ	0.683 μ	0.21	± 1.65	CMOS 0.18	pH sensing

4. Conclusions

This work presents the design and implementation of a potentiometric readout circuit with CDS and SC-LPF for pH-sensing applications. The proposed circuit, fabricated in Magnachip 0.18 μm CMOS technology, operates with a ± 1.65 V supply voltage and achieves a low noise performance of 0.683 V_{rms} . The design consists of two stages: the first stage, a CDS, and the second stage, an SC-LPF, operating at a 1 MHz clock frequency. The noise reduction from 260.8 V_{rms} in the OPAMP stage to 0.683 V_{rms} in the CDS with the SC-LPF demonstrates the effectiveness of the proposed architecture in mitigating noise, particularly at lower frequencies. The OPAMP used in the design is a two-stage telescopic architecture with a high gain of 110 dB, ensuring high performance for pH-sensing applications. Post-layout simulation results confirm that the circuit operates with a low power consumption of 124.1 μW while maintaining a linear response for the pH sensor's DC output in the range of -1.5 V to $+1.5$ V. The compact design, measuring 990 $\mu\text{m} \times 216 \mu\text{m}$, further demonstrates the suitability of the readout circuit for in vivo applications, such as oral healthcare devices that measure the pH of saliva using ISFET sensors. Overall, the proposed potentiometric readout circuit offers significant improvements in noise reduction, power efficiency, and area, making it a promising solution for accurate and low-power pH-sensing systems.

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