



Article

Design of Ultra-Low-Power Rail-to-Rail Input Common Mode Range Standard-Cell-Based Comparators

Antonio Manno ^{1,*} , Giuseppe Scotti ² and Gaetano Palumbo ¹

¹ Dipartimento di Ingegneria Elettrica, Elettronica e Informatica (DIEEI), Università degli Studi di Catania, 95123 Catania, Italy; gaetano.palumbo@unict.it

² Dipartimento di Ingegneria dell'Informazione, Elettronica e Telecomunicazioni (DIET), Università degli Studi di Roma "La Sapienza", 00184 Rome, Italy; giuseppe.scotti@uniroma1.it

* Correspondence: antonio.manno@phd.unict.it

Abstract: In this paper, a NOR2 standard-cell-based dynamic comparator providing rail-to-rail input common mode range (ICMR) is presented, together with a novel standard-cell oriented design methodology. The proposed topology provides better speed performance and lower power-delay-product than the previously presented standard-cell-based dynamic comparators with rail-to-rail ICMR features. The NOR2 topology, which is also better than the complementary NAND2-based topology previously presented by the authors, is even able to guarantee improvements in the order of $8\times$ – $16\times$ higher speed and $7\times$ lower PDP, with respect to the other rail-to-rail ICMR standard-cell-based topologies in the literature. Concerning the standard-cell oriented design methodology, it is focused on the impact of the cell's strength, which is the only free parameter, on delay, power consumption, ICMR and offset. The circuit performances are demonstrated for supply voltages equal to 600 mV, 300 mV and 150 mV, considering a 45 nm CMOS technology.

Keywords: CMOS; logic gates; standard cell; dynamic comparator; comparators; ultra-low voltage; ultra-low power; IoT



Academic Editor: Fabian Khateb

Received: 20 January 2025

Revised: 4 March 2025

Accepted: 5 March 2025

Published: 8 March 2025

Citation: Manno, A.; Scotti, G.; Palumbo, G. Design of Ultra-Low-Power Rail-to-Rail Input Common Mode Range Standard-Cell-Based Comparators. *J. Low Power Electron. Appl.* **2025**, *15*, 14. <https://doi.org/10.3390/jlpea15010014>

Copyright: © 2025 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (<https://creativecommons.org/licenses/by/4.0/>).

1. Introduction

Together with the introduction of smart devices, from industrial to health purposes, exploiting the Internet of Things (IoT) [1–5], the development of ultra-low-power consumption (ULP) integrated systems [6,7] has become increasingly critical to the realization of such devices.

Almost every kind of smart system relies on electronic circuits like ADCs or LDOs [8–11], for example, to interface with the environment, exploit sensors, or simply to manage the power. In all these fundamental circuits, the comparator plays a crucial role for their functionalities, speed performances and power consumption.

Since the comparator is an analog building block, its design typically requires a full-custom approach. This means that the schematic and the layout design phases have to be carried out manually, tuning the design parameters iteratively until specifications are satisfied, taking into account not only mismatch variations but also process, supply voltage and temperature (PVT) variations. Comparing the required design time and effort of the full-custom approach to the typical semi-automatic digital design flow, it becomes evident that the digital one offers lower design time and effort, even with high-complexity designs.

Recently, the possibility to exploit the standard-cell approach, and thus the semi-automatic digital design flow, to dramatically reduce the overall analog circuit design effort has been explored in [12–17]. Moreover, together with the use of standard-cells,

investigation is ongoing regarding the hard scaling of supply voltage down to the deep sub-threshold region (150–300 mV) and power consumption down to the pW-range. The same trend has been exploited not only for comparators but also to realize operational transconductance amplifiers, based on standard-cells, with minimum design effort and reduced power consumption.

Actually, the state-of-the-art offers several standard cell-based dynamic voltage comparator (SCB-DVC) topologies [18–22]. It is possible to classify the topologies depending on the offered input common mode range (ICMR): rail-to-rail ICMR and non-rail-to-rail ICMR topologies [23].

Historically, the first SCB-DVC was the non-rail-to-rail ICMR topology proposed in [18] in 2014, whose ICMR spans from $V_{DD}/2$ to V_{DD} . In 2018, a topology with complementary ICMR with respect to [18], ranging from 0 to $V_{DD}/2$, exploiting 3-input NOR gates, has been proposed in [19], and combining it with the one in [18], the first rail-to-rail topology was also presented in [19].

The solutions in [18,19] exploit only NAND, NOR and NOT standard-cells. Following the same idea in [19], a topology based on OAI (Or–And invert) and AOI (And–Or invert) standard-cells has been proposed, in 2020, in [20].

It is worth noting that the mentioned topologies need almost two or three different types of gate for each comparator, and, in 2024, a rail-to-rail topology, based on 2-input NAND gates only (subsequently referred to as NAND2), was proposed in [22]. Actually, this is the best rail-to-rail ICMR topology in the state-of-the-art, in terms of power consumption and delay.

In this work, starting from the NAND2 topology, we introduce a novel topology made up of only 2-input NOR gates and referred to as NOR2 topology in the following. Despite being complementary to the NAND2 topology proposed by the authors in [22], the NOR2 topology has neither been discussed nor presented previously. This paper presents, for the first time, an analysis and the derived design rules in term of cell strength for both the NOR2 and the NAND2 topologies. An optimized design for minimum offset and another one for minimum power consumption are also presented for the first time in the manuscript, referring to both the NOR2 and the NAND2 topologies. The proposed NOR2 topology exhibits better performance in terms of both speed and power-delay product with respect to the previously presented NAND2 topology. The following considerations are supported by simulations regarding clock-to-output delay, power consumption, ICMR and offset by means of Monte Carlo analysis, referring to a 45 nm CMOS technology. All the simulations are carried out at three different supply voltages, respectively—600 mV, 300 mV and 150 mV—to demonstrate the independence with respect to supply voltage scaling.

The paper is structured as follows. The NAND2 SCB-DVC and the proposed NOR2 working principles are first described in Section 2. In Section 3, the dependency of delay, power consumption, ICMR and offset with respect to the only editable cell design parameter will be highlighted by means of simulations. In Section 4, the NAND2 and the NOR2 topologies are compared in terms of overall performance through suitable figures-of-merit (FoMs). Concluding remarks are finally drawn in Section 5.

2. Rail-to-Rail ICMR Standard Cell-Based DVCs

In the following subsection, a simple explanation of the working principle of the NAND2 topology and of the proposed NOR2 one is provided, exploiting a simple gate-level approach.

2.1. NAND2 SCB-DVC

The gate-level structure of the NAND2 is reported in Figure 1 [22]. The architecture is multistage and is made up by 2-input NAND gates only. It is possible to recognize the first stage, also referred to as the pre-amplifier stage, with the analog input signals V_{INP} and V_{INM} , connected to the A inputs of the gates $S_{1,2}$, and the clock signal, CLK , connected to their B inputs. The pre-amplifier cell's strength is referred to as X_{pre} .

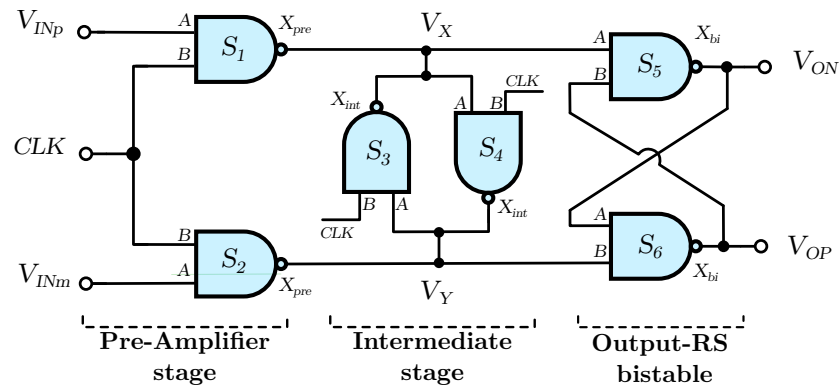


Figure 1. NAND2 SCB-DVC topology.

The pre-amplifier outputs, V_X and V_Y , also named intermediate nodes, are connected to the intermediate stage, consisting of two back-to-back NAND gates, $S_{3,4}$. The output of S_3 is fed back to the A input of S_4 , and vice-versa, to realize a positive, or regenerative, feedback loop. The remaining B inputs of each gate are connected to the clock signal. The intermediate stage cell's strength is reported as X_{int} .

The intermediate nodes directly drive the well-known RS bi-stable stage, whose function is to sample and retain, at the output nodes, V_{OP} and V_{ON} , the information extracted from the analog input differential signal, $V_{ID} = V_{INP} - V_{INM}$, amplified by the first stage and regenerated by the intermediate stage. The output bi-stable cell's strength is reported as X_{bi} .

The working principle can be explained considering that, in general, a DVC is a clocked circuit and thus its operations are related to the clock signal. In particular, during the clock period it is possible to recognize two working phases: pre-charge, or reset phase, during the first half clock period, and the evaluation phase, during the second half clock period. In the reset phase ($CLK = 0$), the parasitic capacitances at the inner nodes, V_X and V_Y , are tied to V_{DD} by gates S_{1-4} , forcing the output RS bi-stable stage into storage condition (the RS bi-stable stage is in storage condition when its inputs are both tied to V_{DD}). During this phase, as the name suggests, the charge at the inner node capacitances is restored from the previous comparison in which one of the two nodes has been tied to V_{DD} and the other to 0.

When a rising edge on the clock signal occurs, the circuit enters in evaluation phase ($CLK = V_{DD}$). In this phase, the gates S_{1-4} can be seen as simple inverters where the threshold voltage is slightly higher than $V_{DD}/2$ (i.e., the threshold voltage of a symmetrical inverter). Indeed, the Pull-Down-Network of the NAND has two series transistors, which makes it weaker than the Pull-Up-Network.

In an analog context, the two inverters can be assumed as a class AB differential amplifier. Thus, it is straightforward to observe that $S_{1,2}$ implement a differential amplification stage, biased by the input common mode voltage, V_{ICM} .

The pre-amplifier stage amplifies the input differential signal, V_{ID} , developing a differential voltage, V_{XY} , at the inner nodes. At the same time, it is responsible for the inner common mode voltage, $V_{XY,CM}$, falling from V_{DD} to an inverted version of the V_{ICM} , after

a certain amount of time, t_{amp} . After t_{amp} , the intermediate stage starts regenerating V_{XY} in a period named t_{reg} , to correctly drive the output stage. Finally, the RS bi-stable allows one to achieve the rail-to-rail output and the retention of the comparator decision during the successive reset phase.

In Figures 2–4, examples of the described voltage waveforms on each node are plotted. The examples consider V_{DD} equal to 300 mV, the input differential signal, V_{ID} , equal to 10 mV and the input common mode voltage, V_{ICM} , equal to $V_{DD}/4$, $V_{DD}/2$ and $3V_{DD}/4$, respectively. The three different values for V_{ICM} are considered in order to show the different behavior of $V_{XY,CM}$ with respect to V_{ICM} , according to the above description.

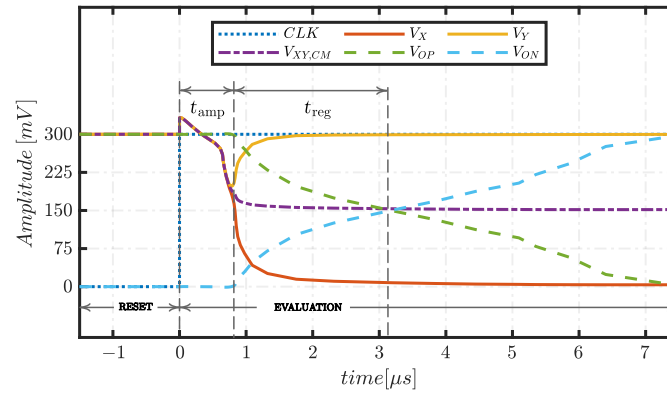


Figure 2. NAND2 node voltages with $V_{DD} = 300$ mV, $V_{ID} = 10$ mV and $V_{ICM} = V_{DD}/4$.

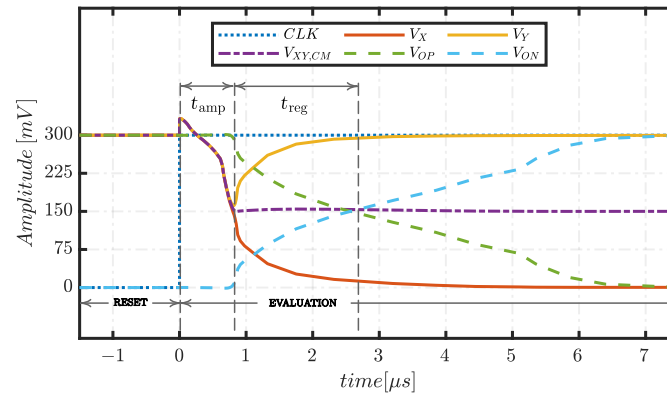


Figure 3. NAND2 node voltages with $V_{DD} = 300$ mV, $V_{ID} = 10$ mV and $V_{ICM} = V_{DD}/2$.

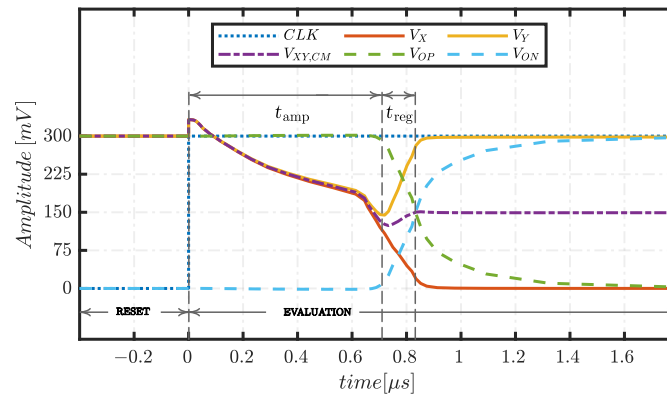


Figure 4. NAND2 node voltages with $V_{DD} = 300$ mV, $V_{ID} = 10$ mV and $V_{ICM} = 3V_{DD}/4$.

2.2. NOR2 Proposed SCB-DVC

The gate-level structure of the proposed NOR2 topology is reported in Figure 5. It exhibits a multistage architecture and is made up of 2-input NOR gates only. It is again

possible to recognize the first pre-amplifier stage, with the analog input signals V_{INP} and V_{INM} , connected to the A inputs of the gates $S_{1,2}$, and the inverted clock signal, $\overline{CLK}$, connected to their B inputs. The pre-amplifier outputs, V_X and V_Y , are connected to the intermediate stage, consisting of two back-to-back NOR gates, $S_{3,4}$. The output of S_3 is fed back to the A input of S_4 , and vice-versa, to realize a positive, or regenerative, feedback loop. The remaining B inputs of each gate are connected to the inverted clock signal. The intermediate nodes directly drive the well-known “SR bi-stable” stage, whose function is to sample and retain, at the output nodes, V_{OP} and V_{ON} , the information extracted from the analog input differential signal, V_{ID} , amplified by the first stage and regenerated by the intermediate stage, as in the NAND2. The strength of the pre-amplifier stage, intermediate stage and the output bi-stable stage cells are indicated as X_{pre} , X_{int} and X_{bi} , respectively.

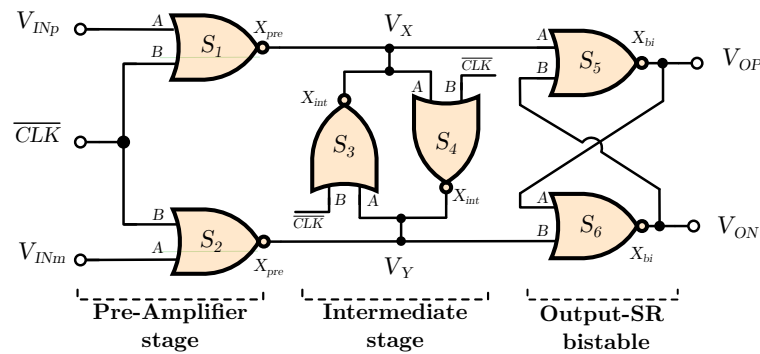


Figure 5. NOR2 SCB-DVC proposed topology.

The working principle can be explained using the same considerations previously done for the NAND2 topology. During the reset phase ($\overline{CLK} = V_{DD}$), the parasitic capacitances at the inner nodes, V_X and V_Y , are tied to 0 by gates S_{1-4} , forcing the output SR bi-stable into storage condition (the SR bi-stable is in storage condition when its inputs are both 0). During this phase, the charge at the inner nodes capacitances is restored from the previous comparison in which one of the two nodes has been tied to V_{DD} and the other to 0. When a falling edge on the clock signal occurs, the circuit enters an evaluation phase ($\overline{CLK} = 0$). In this phase, the gates S_{1-4} can be seen as simple inverters where the threshold voltage is slightly lower than $V_{DD}/2$ (i.e., the threshold voltage of a symmetrical inverter). Indeed, the Pull-Up-Network of the NOR has two series transistors, which makes it weaker than the Pull-Down-Network.

As in the NAND2, $S_{1,2}$ act as a differential amplification stage, biased by the input common mode voltage, V_{ICM} . The first stage amplifies the input differential signal, V_{ID} , developing a differential voltage, V_{XY} , at the inner nodes. At the same time, it is responsible for the inner common mode voltage, $V_{XY,CM}$, rising from 0 to an inverted version of the V_{ICM} , with respect to the threshold $V_{DD}/2$, after a time, t_{amp} . After t_{amp} , the intermediate stage starts regenerating V_{XY} in a time named t_{reg} to properly drive the output stage. Finally, the SR bi-stable allows one to achieve the rail-to-rail output and the retention of the comparator decision during the successive reset phase, as for the NAND2.

Examples of the described voltage waveforms are plotted in Figures 6–8. The examples consider V_{DD} equal to 300 mV, the input differential signal, V_{ID} , equal to 10 mV and the input common mode voltage, V_{ICM} , equal to $V_{DD}/4$, $V_{DD}/2$ and $3V_{DD}/4$, respectively. The different V_{ICM} values for V_{ICM} are considered in order to show the different behavior of $V_{XY,CM}$ with respect to V_{ICM} , according to the previous description.

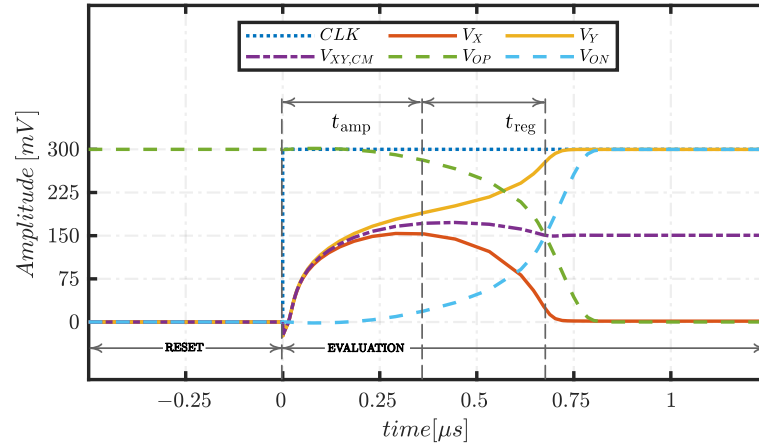


Figure 6. NOR2 node voltages with $V_{DD} = 300$ mV, $V_{ID} = 10$ mV and $V_{ICM} = V_{DD}/4$.

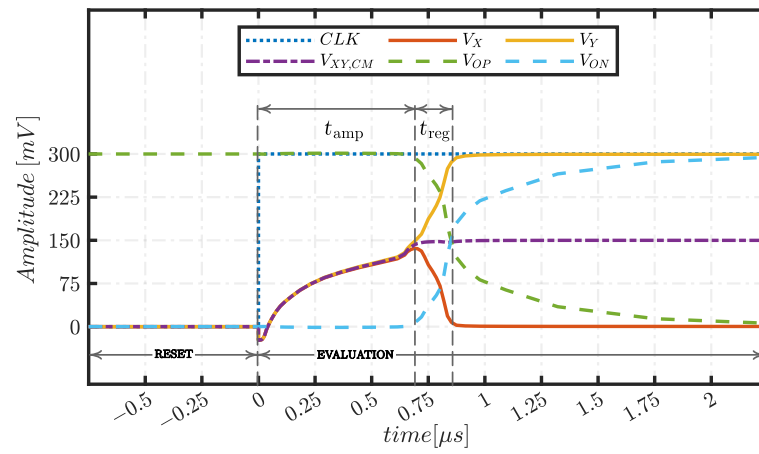


Figure 7. NOR2 node voltages with $V_{DD} = 300$ mV, $V_{ID} = 10$ mV and $V_{ICM} = V_{DD}/2$.

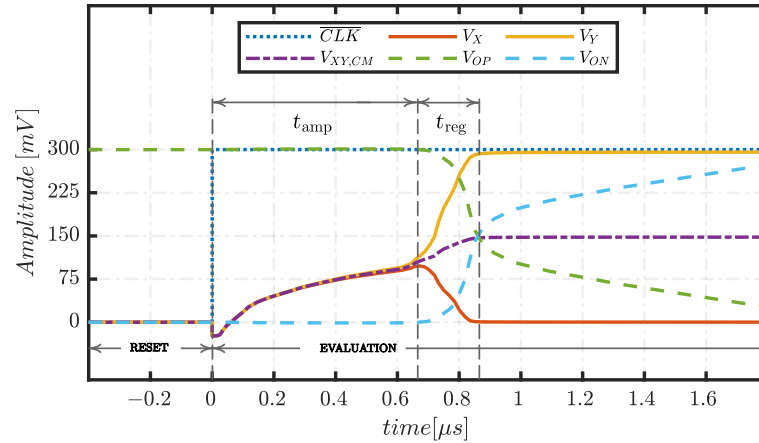


Figure 8. NOR2 node voltages with $V_{DD} = 300$ mV, $V_{ID} = 10$ mV and $V_{ICM} = 3V_{DD}/4$.

3. Standard-Cell Oriented Design

When designing a comparator, the typical requirements of the application are delay (or speed), power consumption, offset, ICMR and area occupation. In general, if the design approach is full-custom, it is possible to size each transistor to meet the requirements. On the other hand, if a standard-cell approach is used, it is not possible to access the transistor level, and thus the degrees of freedom are strongly reduced. In fact, referring to a standard-cell approach, the only parameter that can be set by the designer is the strength of the cell, which represents the multiplicity of the cell's transistors width with respect to the

minimum-sized cell (referred to as strength 1, or X1). Thus, the cell's area occupation is directly proportional to its strength.

In this section, the dependence of delay, power consumption, ICMR and offset from the cell's strength is derived and confirmed by means of simulations using a 45 nm CMOS technology. The analysis has been carried out, with 600 mV, 300 mV and 150 mV supply voltage and common mode input voltage, V_{ICM} , equal to $V_{DD}/2$. For both the NAND2 and NOR2 topologies, a minimum-sized output bi-stable stage ($X_{bi} = X1$), loaded by minimum-sized NOR gates (i.e., about 0.6 fF load capacitance at each output node) is always considered. Using minimum-sized gates for the output stage always represents the optimum design condition. The pre-amplifier and intermediate stage cell's strength, named X_{pre} and X_{int} , respectively, have been varied in the set of values X1, X2, X4, X6 and X8.

Since the same trends were found for each supply voltage, in the following we will consider only the results with 300 mV V_{DD} .

3.1. Delay

Increasing the strength of a gate means enlarging the width of all the transistors of the same quantity. In particular, depending on the X_{int} value, two kinds of behavior arise. In Figure 9a and 9b are reported the simulation results for the NAND2 and NOR2, respectively, varying X_{pre} with fixed X_{int} . The same analysis has been carried out by varying X_{int} with fixed X_{pre} , and the results are given in Figure 9c,d. By inspection of the figures, it is apparent that, for X_{int} lower than 4, an increase in X_{pre} determines a proportional increase in the delay, while for $X_{int} \geq 4$ the delay is almost independent from X_{pre} . Moreover, the relation between delay and the cell's strength implies that the speed of the comparator is mainly a topological aspect. This fundamental result, depending on the other application requirements, could allow one to minimize the area, and hence also power consumption, ensuring almost the same speed performances.

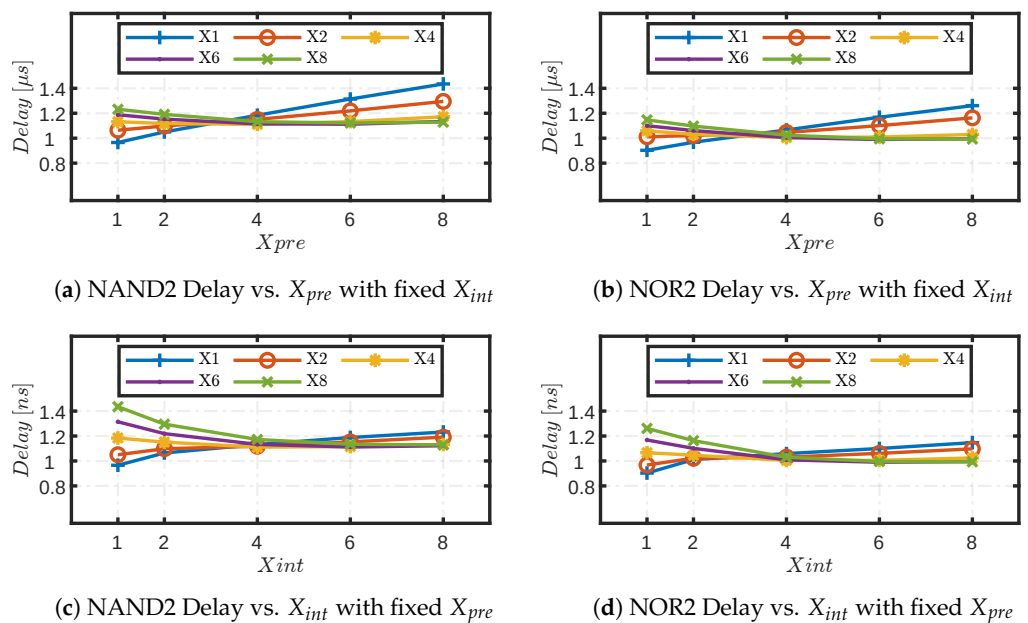


Figure 9. Delay dependence to X_{pre} and X_{int} with V_{DD} equal to 300 mV, V_{ICM} equal to $V_{DD}/2$ and V_{ID} equal to 10 mV.

3.2. Power Consumption

Since the strength is linearly related to the current capability and the total capacitance introduced by a gate, it is expected that both the static and dynamic power consumption of each gate increases with its strength. Considering that these comparators are composed by a

pre-amplifier stage, an intermediate stage and an output stage, each of them may contribute differently to the overall power consumption. However, since the output stage is considered always minimum, only the impact of the pre-amplifier stage and the intermediate stage are investigated.

In particular, the main power consumption contribution is given by the pre-amplifier stage. In fact, when the evaluation phase starts, a fast peak current is driven to the parasitic capacitances at the inner nodes whose charge has been restored in the reset phase, contributing to the dynamic power consumption. During the evaluation phase, in particular, after V_{XY} is regenerated (see Section 2), one of the two intermediate node voltages, V_X or V_Y , is tied to 0 and the other one is tied to V_{DD} by the positive feedback given by the intermediate stage. At the same time, since the input voltage is maintained at the pre-amplifier inputs, a static current is always driven to the node that is tied to 0 (i.e., to ground) by the pre-amplifier. Moreover, on the node that has been tied to V_{DD} , another static current, which can be seen as a leakage current, is sunk by the pre-amplifier. In particular, this leakage current contribution is dependent on the input common mode voltage, V_{ICM} , as will be investigated in the subsequent sections.

Hence, a variation in the strength of the pre-amplifier is expected to have a stronger impact on power consumption with respect to a variation in the intermediate stage strength, because the pre-amplifier is responsible for the main dynamic and static current contribution.

Simulation results are shown in Figures 10a and 10b for the NAND2 and NOR2, respectively. Figure 10a, where X_{pre} is varied for a fixed X_{int} , confirms the above discussed increase in power consumption versus X_{pre} . On the other hand, when X_{int} is varied for a fixed X_{pre} , the increase in power consumption is negligible, as shown in Figures 10c and 10d for the NAND2 and NOR2, respectively, thus confirming the expected impact on power consumption of the pre-amplifier strength versus the intermediate stage strength.

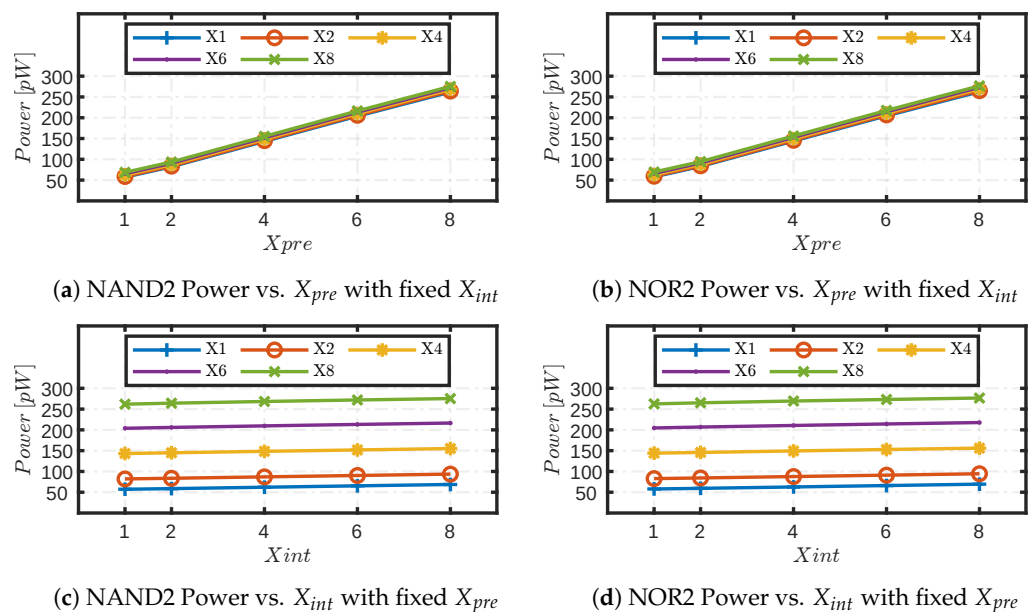


Figure 10. Power dependence to X_{pre} and X_{int} with 300 mV V_{DD} , V_{ICM} equal to $V_{DD}/2$ and V_{ID} equal to 10 mV.

3.3. Input Common Mode Range (ICMR)

The topologies under analysis are capable of offering rail-to-rail ICMR if properly sized, and in this subsection we show how the ICMR varies if different combinations of X_{pre} and X_{int} are considered at 300 mV supply voltage with a minimum differential input signal of 10 mV and 1 kHz clock signal. The ICMR is evaluated as the difference between

the maximum and minimum input common mode voltage, V_{ICM} , for which the output of the comparator is still valid (i.e., V_{OP} and V_{ON} are complementary to each other). In Table 1 and Table 2 are reported the input common mode ranges for the NAND2 and NOR2 topologies, respectively, and the combinations of X_{pre} and X_{int} that allow one to obtain rail-to-rail ICMR are highlighted in bold.

Table 1. NAND2 ICMR [mV] dependence with the cell's strength, considering $V_{DD} = 300$ mV.

	$X1_{int}$	$X2_{int}$	$X4_{int}$	$X6_{int}$	$X8_{int}$
$X1_{pre}$	30–300	10–300	0–300	0–300	0–300
$X2_{pre}$	40–300	30–300	10–300	0–300	0–300
$X4_{pre}$	70–280	50–300	30–300	20–300	10–300
$X6_{pre}$	80–260	70–290	50–300	40–300	30–300
$X8_{pre}$	90–250	80–270	60–300	50–300	40–300

Table 2. NOR2 ICMR [mV] dependence with the cell's strength, considering $V_{DD} = 300$ mV.

	$X1_{int}$	$X2_{int}$	$X4_{int}$	$X6_{int}$	$X8_{int}$
$X1_{pre}$	0–270	0–280	0–300	0–300	0–300
$X2_{pre}$	0–250	0–270	0–290	0–300	0–300
$X4_{pre}$	20–230	0–250	0–270	0–290	0–300
$X6_{pre}$	40–220	20–230	0–260	0–270	0–280
$X8_{pre}$	60–210	40–230	0–250	0–270	0–280

It is evident that, for both the topologies, the ICMR is rail-to-rail only if X_{int} is greater than 4 and X_{pre} is smaller than $X_{int}/2$; in the following, this condition will be referred to as the rail-to-rail ICMR condition. If this condition is not guaranteed, when V_{ICM} approaches V_{DD} , or 0, the intermediate stage is not able to regenerate V_{XY} and then the output bi-stable is forced into storage condition or into the undefined one (i.e., the condition in which the outputs are not complementary at all). In both cases, the output cannot be considered valid. It is worth noting that, under the rail-to-rail ICMR condition, as discussed in Section 3.1, the delay of the comparator is almost independent of the cell's strength.

In the following, the behavior of the two topologies is analyzed in the evaluation phase referring to both the case in which the rail-to-rail condition is satisfied and the one in which it is not satisfied. The starting point of the evaluation phase has been assumed at time 0 for convenience.

Regarding the NOR2, if the rail-to-rail ICMR condition is not satisfied, the intermediate stage is not able to regenerate the differential voltage, V_{XY} ; thus, after a short transient, both V_X and V_Y tend to V_{DD} , if V_{ICM} is 0 (Figure 11a), or to 0 if V_{ICM} is V_{DD} (Figure 11b). This behavior can be easily understood if we observe that the pre-amplifier is composed of two gates working as inverters; thus, $V_{XY,CM}$ is simply an inverted version of V_{ICM} . In the case when $V_{XY,CM}$ is V_{DD} , the SR bi-stable is in the undefined condition and its outputs are both tied to 0, and therefore are not complementary at all. When $V_{XY,CM}$ is 0, the SR bi-stable is in storage mode and its outputs are unvaried with respect to the previous evaluation phase. In both cases, the result of the comparison at the output of the comparator cannot be considered valid.

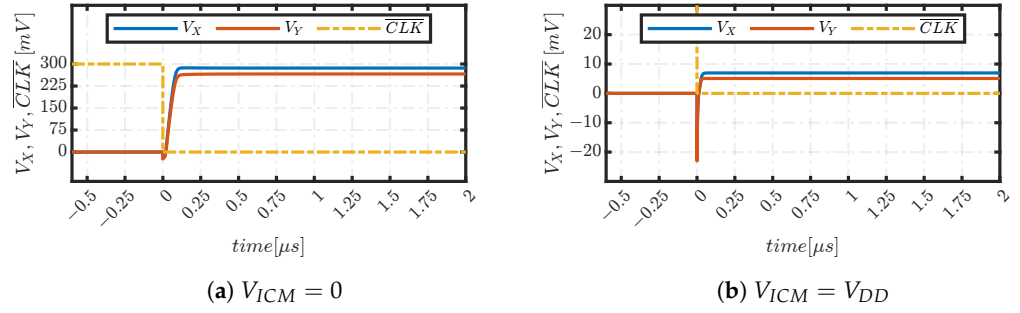


Figure 11. NOR2 intermediate nodes voltages, V_X and V_Y , when the rail-to-rail condition is not satisfied considering $V_{DD} = 300$ mV and $V_{ID} = 10$ mV.

In Figures 12a and 12b are reported the waveforms of V_X and V_Y , with V_{ICM} equal to 0 and V_{DD} , respectively, in the case when the rail-to-rail ICMR condition is satisfied. As can be seen, after the evaluation phase starts, there is a time, t_{amp} , in which both V_X and V_Y rise together with a small difference, V_{XY} , and then a time interval, t_{reg} , in which this small difference is regenerated by the intermediate stage, as introduced in Section 2.

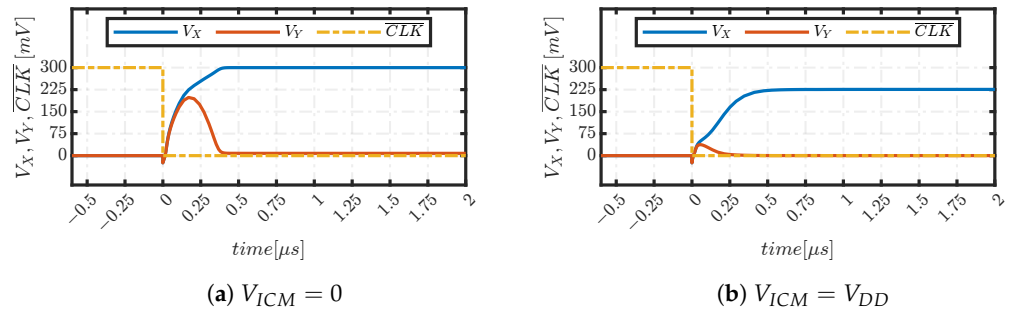


Figure 12. NOR2 intermediate nodes voltages, when the rail-to-rail condition is satisfied considering $V_{DD} = 300$ mV and $V_{ID} = 10$ mV.

Considering the NAND2, when the rail-to-rail ICMR condition is not satisfied, the intermediate stage does not regenerate V_{XY} , and, after a short transient, both V_X and V_Y tend to V_{DD} , if V_{ICM} is 0 (Figure 13a), or to 0 if V_{ICM} is V_{DD} (Figure 13b). The same observation performed for the NOR2 pre-amplifier holds for the NAND2; thus, $V_{XY,CM}$ is simply the inverted V_{ICM} . In the case when $V_{XY,CM}$ tends to V_{DD} , the RS bi-stable is in storage mode and its outputs are unvaried with respect to the previous evaluation phase. When $V_{XY,CM}$ is 0, the RS bi-stable is in the undefined condition and its outputs are both tied to V_{DD} , and are therefore not complementary at all. As for the NOR2, in both cases, the output of the comparator is not valid.

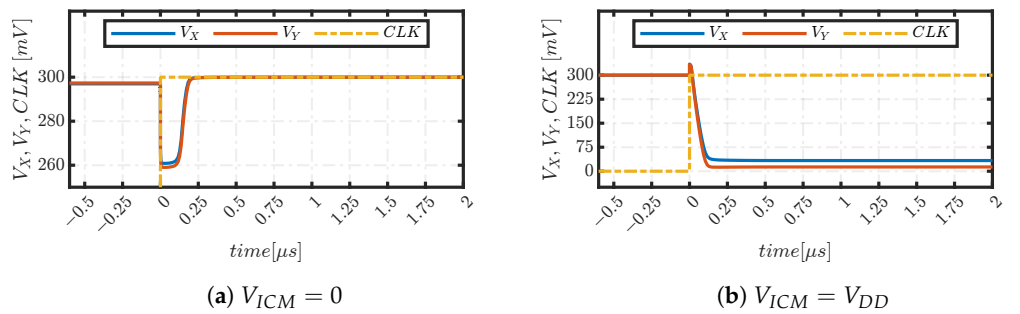


Figure 13. NAND2 intermediate nodes voltages, V_X and V_Y , when the rail-to-rail condition is not satisfied considering $V_{DD} = 300$ mV and $V_{ID} = 10$ mV.

In Figures 14a and 14b, the waveforms of V_X and V_Y , with V_{ICM} equal to 0 and V_{DD} , respectively, are reported in the case where the rail-to-rail ICMR condition is satisfied. As can be seen, after the evaluation phase starts, there is a time, t_{amp} , in which both V_X and

V_Y fall together with a small difference, V_{XY} , and then a time, t_{reg} , in which this small difference is regenerated by the intermediate stage, as explained in Section 2.

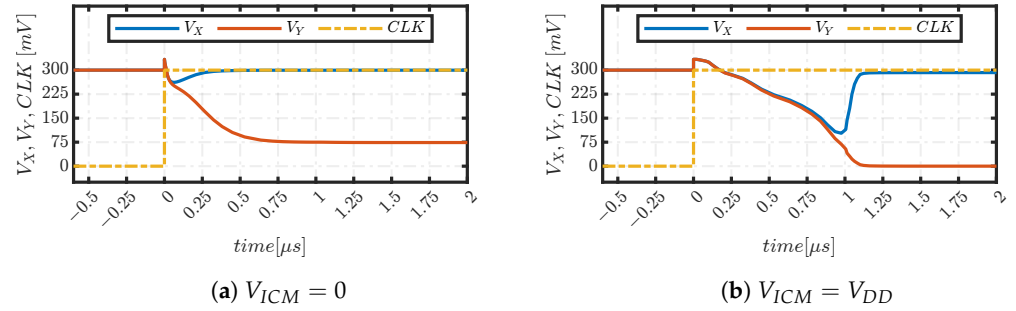


Figure 14. NAND2 intermediate nodes voltages, V_X and V_Y , when the rail-to-rail condition is satisfied considering $V_{DD} = 300$ mV and $V_{ID} = 10$ mV.

It is worth noting that t_{amp} and t_{reg} are dependent on the common mode voltage. In fact, for V_{ICM} equal to V_{DD} the NOR2 shows a low t_{amp} and, vice versa, t_{amp} is higher with V_{ICM} equal to 0. Complementary, the NAND2 exhibits a high t_{amp} when V_{ICM} is equal to V_{DD} and, vice versa, a low t_{amp} when V_{ICM} is equal to 0.

The complementarity of the topologies is simply explainable, observing that a 2-input NOR differs from a 2-input NAND since there are two series transistors in the Pull-Up-Network and only one in the Pull-Down-Network, making its low-to-high propagation delay higher with respect to the NAND. Vice versa, a 2-input NAND has two series transistors in the Pull-Down-Network and only one in the Pull-Up-Network, making its high-to-low propagation delay higher with respect to the NOR.

3.4. Offset

The offset of a comparator is related to the matching properties between transistors [24–30]. According to Pelgrom’s model [24], at the transistor level, it is known that the standard deviation of the offset, σ_{off} , is inversely proportional to the area of the transistors that have to be matched. Since standard cell comparators are multi-stage topologies, the main input referred offset contribution comes from the pre-amplifier, because the offset of the subsequent stages is reduced by the gain of the preceding blocks. This statement has been verified by simulations; thus, we will focus only on the offset dependence on the pre-amplifier strength.

In the case of a standard-cell comparator, the matching has to be guaranteed between standard cells of the pre-amplifier, which are made up of two different types of transistor, NMOS and PMOS. It is possible to demonstrate (see Appendix A) that the offset standard deviation is related to the area of the minimum-sized cell and the cell’s strength, as in (1).

$$\sigma_{off} \propto \frac{\sqrt{2}}{\sqrt{X_{pre} \cdot A_{min}}} \quad (1)$$

Despite the fact that the relationship does not take into account X_{int} , since it is fundamental to guarantee the ICMR requirement, an increase in X_{pre} implies at least an equal increase on the X_{int} value to guarantee the rail-to-rail ICMR.

4. Comparison

In a typical application that exploits one, or more, comparators, the input offset voltage is one of the key parameters that has to be taken into account. Given a topology, if there is the need to decrease the offset, the only way is to increase the area of the cells. However, when increasing the area of the cells, the decrease in the offset is paid with an increase in power consumption, as discussed in Section 3. This behavior implies that a trade-off,

between the offset and power consumption exists. To quantify this trade-off, *FOM1* is introduced in Equation (2) to take into account the offset, in terms of standard deviation, σ_{off} , and mean value, μ_{off} , and the power consumption:

$$FOM1 = \sqrt{\sigma_{off}^2 + \mu_{off}^2} \cdot Power \quad (2)$$

Another important aspect for comparators is the delay, which, in the case of standard cell-based comparators, is mainly related to the topology rather than to the design. Nevertheless, to compare the topologies, it can be useful to introduce *FOM2*, as in [23], in which the offset and power consumption are considered together with the delay:

$$FOM2 = \sqrt{\sigma_{off}^2 + \mu_{off}^2} \cdot Power \cdot Delay = \sqrt{\sigma_{off}^2 + \mu_{off}^2} \cdot PDP \quad (3)$$

This second figure of merit can also be expressed in terms of power-delay-product (PDP), thus providing information about how good the trade off is between offset and energy per comparison.

In this section, we compare the NAND2 and the proposed NOR2 by means of pre-layout simulations referring to a 45 nm CMOS process. Simulation results regarding delay, power consumption and power-delay-product (PDP) of the different topologies are presented, focusing on their performances with respect to V_{ICM} variation at three different supply voltage conditions: 600 mV, 300 mV, 150 mV. The offset related to mismatch variations has been evaluated through Monte Carlo simulations referring to the statistical models for technology mismatch provided by the manufacturer on 1000 samples. A linear ramp differential input signal in a transient simulation, with amplitude ranging from $-V_{DD}$ to V_{DD} and common mode voltage equal to $V_{DD}/2$, is considered, and the input-referred offset voltage is evaluated by taking the value of V_{ID} , which corresponds the output commutation. Moreover, the relation between offset and power consumption introduces the possibility to design the comparator in order to minimize one of them. Thus, in the following the topologies will be designed in both ways, also guaranteeing rail-to-rail ICMR.

4.1. Rail-to-Rail ICMR with Minimum Offset Design

The first requirement to guarantee is the ICMR; thus, the values of X_{pre} and X_{int} must be chosen according to the rail-to-rail ICMR condition highlighted previously in Tables 1 and 2 for the NAND2 and NOR2, respectively. In Table 3, the chosen strengths are reported together with the performance parameters evaluated with V_{ICM} equal to $V_{DD}/2$ at three different supply voltages.

Table 3. Rail-to-Rail ICMR with minimum offset design considering $V_{ICM} = V_{DD}/2$.

Topology	Supply [mV]	$X_{pre,int}$	Power [pW]	Delay [ns]	PDP [aJ]	σ_{off} [mV]	$\% \frac{\sigma_{off}}{V_{DD}}$	μ_{off} [mV]	FOM1 [V·pW]	FOM2 [V·aJ]
NOR2	150	$X_{4,8}$	12.9	16,100	207.6	14.6	9.73%	0.419	0.188	3.03
	300	$X_{4,8}$	156.1	1020	159	45.3	15.1%	−0.674	7.07	7.21
	600	$X_{4,6}$	29,200	9.36	273.3	95.4	15.9%	−0.727	2780	26.07
NAND2 [22]	150	$X_{2,6}$	9.32	19,070	177	18.3	12.2%	0.947	0.17	3.25
	300	$X_{2,6}$	90.3	1150	103.8	50.8	16.9%	0.66	4.59	5.29
	600	$X_{2,8}$	14,590	11.04	161	105.2	17.5%	−1.4	1540	16.94

As can be seen, with a hardly scaled supply voltage of 150 mV and 300 mV, the NOR2 exhibits a σ_{off} equal to 14.6 mV and 45.3 mV, respectively. These values are about 5 mV less than the σ_{off} of the NAND2. However, this difference is paid with an increased power consumption. The same holds at 600 mV, where the NOR2 offers a 10 mV smaller σ_{off} . It is worth noting that the σ_{off} of each topology increases with the supply voltage, but the ratio σ_{off}/V_{DD} is always lower than 20%.

Concerning the effects of V_{ICM} on delay and power consumption, in Figures 15 and 16 the results for both topologies are shown. As can be seen, at 150 mV the NOR2 is much faster than the NAND2 if V_{ICM} is below 70% of V_{DD} . This percentage increases at 300 and 600 mV, where the NOR2 is faster with V_{ICM} below 90% of V_{DD} . It is worth noting that the trends are complementary to each other with respect to $V_{DD}/2$, given that the topologies are complementary to each other. The increased speed of the NOR2 is paid in terms of power consumption that is higher with respect to the NAND2, at 150 mV, for every V_{ICM} . At 300 and 600 mV the NOR2 power consumption is almost the same as the NAND2, at least for V_{ICM} below 80–90% of V_{DD} , above which the NOR2 shows a higher consumption. However, for each topology it is possible to find a minimum for the power consumption when V_{ICM} is equal to $V_{DD}/2$.

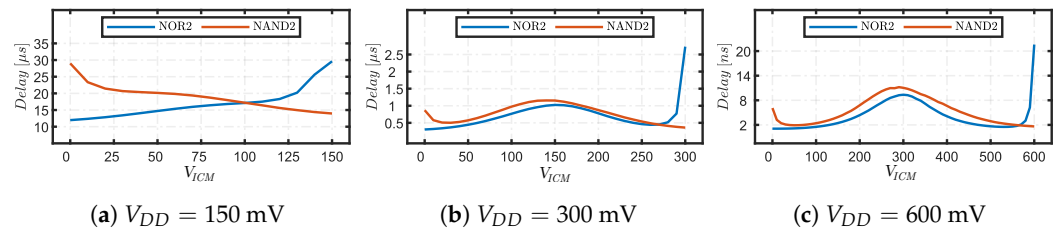


Figure 15. Delay vs. V_{ICM} with minimum offset design approach.

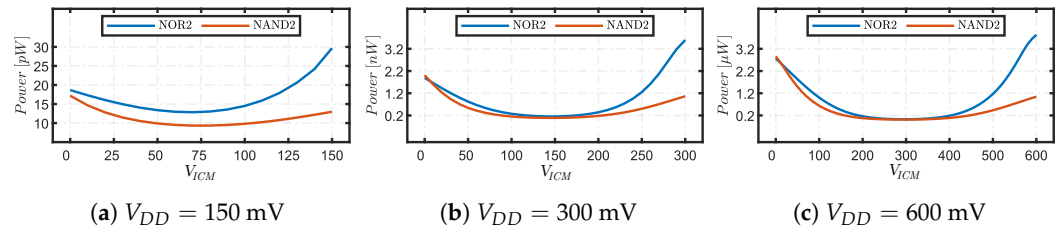


Figure 16. Power consumption vs. V_{ICM} with minimum offset design approach.

4.2. Rail-to-Rail ICMR with Minimum Power Consumption Design

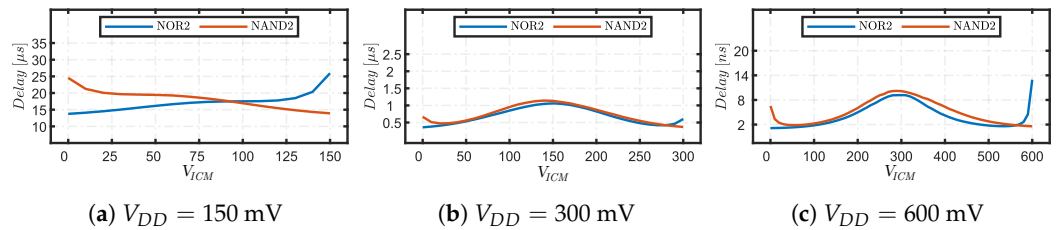
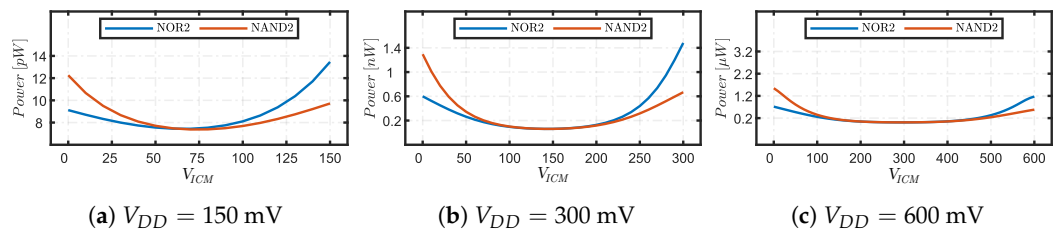
As for the minimum offset approach, the rail-to-rail ICMR has to be guaranteed; thus, the values of X_{pre} and X_{int} must be chosen according to the rail-to-rail ICMR condition, considering the values in Tables 1 and 2 for the NAND2 and NOR2, respectively. In Table 4, the chosen strengths are reported, together with the performance parameters evaluated with V_{ICM} equal to $V_{DD}/2$ at three different supply voltages.

In this case, both the topologies exhibit almost the same power consumption for each supply voltage that is consistently lower with respect to the minimum offset case. Concerning the delay, the NOR2 shows a slightly lower delay with respect to the NAND2 when the PDP is lower. Regarding the offset, the NAND2 offers a lower σ_{off} than the NOR2, with increased σ_{off}/V_{DD} ratio with respect to the minimum offset design. It is worth noting that, in this case, the topologies exploit smaller cells with respect to the minimum offset case; thus, the offset standard deviation is higher, as expected.

Table 4. Rail-to-Rail ICMR with minimum power consumption design with $V_{ICM} = V_{DD}/2$.

Topology	Supply [mV]	$X_{pre,int}$	Power [pW]	Delay [ns]	PDP [aJ]	σ_{off} [mV]	$\% \frac{\sigma_{off}}{V_{DD}}$	μ_{off} [mV]	FOM1 [V·pW]	FOM2 [V·aJ]
NOR2	150	$X_{1,4}$	7.48	17,200	128	29.6	19.7%	0.942	0.22	3.82
	300	$X_{1,4}$	62.7	1050	65.8	75.4	25.1%	0.108	4.72	4.96
	600	$X_{1,2}$	8770	9.18	80.58	145.3	24.2%	4.2	1270	11.7
NAND2 [22]	150	$X_{1,4}$	7.37	18,600	137	24.6	16.4%	0.986	0.18	3.38
	300	$X_{1,4}$	62	1130	70	62.6	20.8%	0.133	3.88	4.39
	600	$X_{1,4}$	8760	10.1	88.4	119.7	19.95%	−2.7	1040	10.59

The same considerations about the effects of V_{ICM} on delay and power consumption, done for the minimum offset case, hold for the minimum power one. In Figures 17 and 18, the results for both topologies are shown. Again, at 150 mV the NOR2 is much faster than the NAND2 if V_{ICM} is below 70% of V_{DD} . For V_{DD} equal to 300 and 600 mV, the NOR2 is slightly faster. Also in this case, the trends are complementary to each other with respect to $V_{DD}/2$, given the complementarity of the topologies.

**Figure 17.** Delay vs. V_{ICM} with minimum power design approach.**Figure 18.** Power consumption vs. V_{ICM} with minimum power design approach.

It is worth noting that, regardless of the design strategy, both of the topologies show a complementary parabolic-like power consumption trend with respect to V_{ICM} (see Figures 16 and 18). It is possible to find a minimum for V_{ICM} equal to $V_{DD}/2$, at which the topologies are perfectly equivalent. In this condition, after V_{XY} is regenerated, V_{ICM} drives the pre-amplifier's transistors in the saturation region and the static current is limited. On the other hand, if V_{ICM} tends to 0 or V_{DD} , the pre-amplifier's transistors are driven in the triode region; thus, a low-resistance path from V_{DD} to ground is realized. In these cases, the power consumption is higher than the case in which V_{ICM} is equal to $V_{DD}/2$.

The complementarity of the topologies is also evident in terms of power consumption. In fact, if V_{ICM} tends to 0, the NOR2 offers a lower power consumption with respect to the NAND2. Vice versa, if V_{ICM} tends to V_{DD} , the power consumption of the NOR2 is higher with respect to the one of the NAND2. This duality comes from the duality between the Pull-Up-Network of the NOR2 and the Pull-Down-Network of the NAND2, as described in Section 3.3. In fact, the path from V_{DD} to ground offered by the NOR2, when V_{ICM} is

equal to 0, is made up of two series transistors with respect to the NAND2, in which the path is given by only one transistor. Thus, the NOR2 static current is lower. Conversely, the path from V_{DD} to ground offered by the NOR2, when V_{ICM} is equal to V_{DD} , is made up of only one transistor with respect to the NAND2, in which the path is given by two series transistors. In this case, the NOR2 static current will be higher.

4.3. Comparison with the State-of-the-Art of rail-to-rail Topologies

In this subsection, we compare the proposed topology, designed with both minimum offset and minimum power methods, with the rail-to-rail ICMR topologies in [19,20,22]. The results are given considering V_{ICM} equal to $V_{DD}/2$ and V_{ID} equal to 10 mV and are reported in Table 5, where the NOR2 is designed for minimum offset, and Table 6, where the NOR2 is designed for minimum power. It is worth noting that the NOR2 is faster than the NAND2, with V_{ICM} equal to $V_{DD}/2$.

Table 5. Rail-to-Rail ICMR and minimum offset design with $V_{ICM} = V_{DD}/2$.

Topology	Supply [mV]	Power [pW]	Delay [ns]	PDP [aJ]	σ_{off} [mV]	$\% \frac{\sigma_{off}}{V_{DD}}$	μ_{off} [mV]	FOM1 [V·pW]	FOM2 [V·aJ]
NOR2	150	12.9	16,100	207.6	14.6	9.73%	0.419	0.188	3.03
	300	156.1	1020	159	45.3	15.1%	−0.674	7.07	7.21
	600	29,200	9.36	273.3	95.4	15.9%	−0.727	2780	26.07
NAND2 [22]	150	9.32	19,070	177	18.3	12.2%	0.947	0.17	3.25
	300	90.3	1150	103.8	50.8	16.9%	0.66	4.59	5.29
	600	14,590	11.04	161	105.2	17.5%	−1.4	1540	16.94
[19]	150	7.9	134,000	1060	12.1	8.06%	18.6	0.175	23.5
	300	30.3	8530	258.8	10.3	3.43%	1.2	0.31	2.68
	600	8290	152.1	1260	10.21	1.7%	0.53	80	12.89
[20]	150	15.2	50,600	770	13.83	9.22%	6.49	0.23	11.75
	300	99.1	4460	442	11.9	3.87%	1.98	1.19	5.33
	600	8300	70.8	587	11.61	1.93%	2.01	97	6.92

As can be seen from Table 5, the NOR2 designed for minimum offset shows a much lower delay, with higher power consumption; nevertheless, the PDP is greatly reduced with respect to [19,20]. From the offset point of view, the NOR2 exhibits a slightly higher σ_{off} and a much lower μ_{off} , at 150 mV. The σ_{off} becomes higher as the supply increases, with respect to the values of [19,20], which are almost constant. In fact, the FOM1 of the NOR2 is higher than [19,20], unless at 150 mV supply, and increases with supply voltage. However, if the FOM2 is considered, the NOR2 offers the best trade-off between offset, power consumption and delay, at 150 mV.

The results when minimum power design is considered for the NOR2 are reported in Table 6. It is possible to see that the topology is able to offer a $8\times$ higher speed with respect to the [19], with V_{DD} equal to 150 and 300 mV, and almost $16\times$ higher with V_{DD} equal to 600 mV. With respect to [20], the increase is $4\times$, with V_{DD} equal to 150 and 300 mV, and $8\times$, with V_{DD} equal to 600 mV. Moreover, the great increase in speed is obtained with a lower power consumption, with respect to [19,20], at 150 mV. This does not hold with V_{DD} equal

to 300 mV, where the power consumption is $2\times$ higher with respect to [19], but is $0.6\times$ lower than [20]. Considering V_{DD} equal to 600 mV, the increase in power consumption is very small, making the case with V_{DD} equal to 300 mV the worst case in terms of power consumption. However, the NOR2 exhibits meanly a $7\times$ lower PDP, at various supply voltages. From the offset point of view, at 150 mV the NOR2 has a higher σ_{off} , with a much lower μ_{off} , with respect to [19,20]; thus, comparing the three topologies through FOM1, the trade-off between power and offset is better than [20] and slightly worse than [19]. This trade-off is worsened with higher supply voltages. Finally, if the FOM2 is considered, it is possible to state that the best trade-off between offset, power consumption and delay is obtained by the NOR2. If the supply is increased, the topology is able to stay at least in between [19,20].

Table 6. Rail-to-Rail ICMR and minimum power consumption design with $V_{ICM} = V_{DD}/2$.

Topology	Supply [mV]	Power [pW]	Delay [ns]	PDP [aJ]	σ_{off} [mV]	$\% \sigma_{off} / V_{DD}$	μ_{off} [mV]	FOM1 [V·pW]	FOM2 [V·aJ]
NOR2	150	7.48	17,200	128	29.6	19.7%	0.942	0.22	3.82
	300	62.7	1050	65.8	75.4	25.1%	0.108	4.72	4.96
	600	8770	9.18	80.58	145.3	24.2%	4.2	1270	11.7
NAND2 [22]	150	7.37	18,600	137	24.6	16.4%	0.986	0.18	3.38
	300	62	1130	70	62.6	20.8%	0.133	3.88	4.39
	600	8760	10.1	88.4	119.7	19.95%	−2.7	1040	10.59
[19]	150	7.9	134,000	1060	12.1	8.06%	18.6	0.175	23.5
	300	30.3	8530	258.8	10.3	3.43%	1.2	0.31	2.68
	600	8290	152.1	1260	10.21	1.7%	0.53	80	12.89
[20]	150	15.2	50,600	770	13.83	9.22%	6.49	0.23	11.75
	300	99.1	4460	442	11.9	3.87%	1.98	1.19	5.33
	600	8300	70.8	587	11.61	1.93%	2.01	97	6.92

5. Conclusions

In this paper, a NOR2-based rail-to-rail ICMR DVC has been presented, as a complementary version of the NAND2-based one in [22]. The topology provides better speed performance and lower PDP with respect to the NAND2 topology. Moreover, in the paper is also proposed and discussed a standard-cell oriented design approach that makes use of the cell's strength (unique free parameter) and overcomes the difficulties of the transistor level design. In particular, the impact of the cell's strength on delay, power consumption, ICMR and offset has been investigated through gate-level modeling and simulations for supply voltages equal to 600 mV, 300 mV and 150 mV, considering a 45 nm CMOS technology. After a first analysis, having the aim of finding the cell's strength conditions that guarantee a rail-to-rail ICMR, it was also found that the delay of the NAND2 and NOR2 is almost independent from the cell's strength. Hence, as expected, it can be assumed that the speed of the comparator is mainly a topological feature. Regarding the power consumption, the impact of each stage has been investigated, and it was found that its variation is mainly due to the cell's strength variation of the pre-amplifier stage. As expected, the same also holds for the offset variation. On the other hand, the cell's strength variation of the intermediate

stage plays a crucial role in guaranteeing the rail-to-rail ICMR. The highlighted behaviors allow the designer to design for minimum power target, or minimum offset target. For both of the two design targets, the performance of the NOR2 has been compared with the NAND2, and a higher speed with lower PDP was found. Moreover, the proposed topology, which is able to guarantee high speed performance with reduced power-delay product, allows improvements in the order of $8\times$ – $16\times$ higher speed and $7\times$ lower PDP, with respect to the other state-of-the-art rail-to-rail standard-cell-based comparators [19,20]. In conclusion, the results demonstrate that the proposed NOR2 topology offers a high performance option for ultra-low voltage, ultra-low power circuits where rail-to-rail ICMR is required. Moreover, the introduced standard-cell oriented approach allows a simple and fast design methodology, which further justifies the use of the standard-cell approach.

Author Contributions: Conceptualization, A.M., G.P. and G.S.; data curation, A.M.; investigation, A.M. and G.P.; software, A.M. and G.S.; validation, A.M., G.P. and G.S.; supervision, G.P. and G.S.; writing—original draft preparation, A.M. and G.P.; writing—review and editing, G.P. and G.S. All authors have read and agreed to the published version of the manuscript.

Funding: This work was supported in part by the Italian Minister of Research PON Ricerca e innovazione 2014–2020, Azione n. IV.6 and in part by the European Union (NextGeneration EU) through the MUR-PNRR Project SAMOTHRACE under Grant ECS00000022.

Data Availability Statement: The original contributions presented in this study are included in the article. Further inquiries can be directed to the corresponding authors.

Conflicts of Interest: The authors declare no conflict of interest.

Appendix A

Since the offset introduced by the pre-amplifier's cells is of concern during the evaluation period, and in this condition the gates can be seen as simple inverters, the analysis will start from the offset of a simple inverter. In the ideal case of a symmetric inverter, the threshold voltage is equal to $V_{DD}/2$. However, in a real case, due to process variation, the threshold voltage slightly differs from $V_{DD}/2$, since the mismatch between transistors introduces an offset effect that can be modeled with a generator, as in Figure A1.

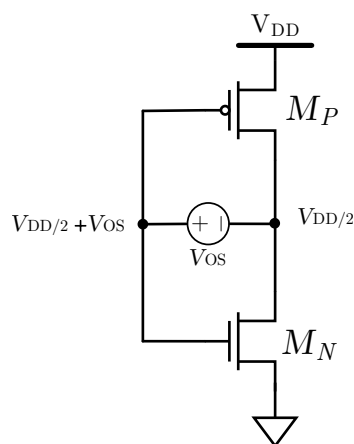


Figure A1. Inverter offset voltage modeling.

Considering the transistors working in sub-threshold, as it is the common case for ULV topologies, the drain current is given by

$$I_D = I_{D0} \frac{W}{L} \exp\left(\frac{|V_{GS}| - V_{TH}}{nV_T}\right) \quad (A1)$$

Therefore, taking into account the offset voltage, from the current balance we get

$$I_{N0} \left(\frac{W_N}{L_N} \right) \exp \left(\frac{V_{DD}/2 + V_{OS} - V_{TN}}{nV_T} \right) = I_{P0} \left(\frac{W_P}{L_P} \right) \exp \left(\frac{V_{DD}/2 - V_{OS} - |V_{TP}|}{nV_T} \right) \quad (A2)$$

and solving for V_{OS} we obtain

$$V_{OS} = \frac{nV_T}{2} \left[\ln \left(\frac{\mu_P}{\mu_N} \right) + \ln \left(\frac{W_P}{W_N} \right) + \ln \left(\frac{L_N}{L_P} \right) \right] + \frac{1}{2} (V_{TN} - |V_{TP}|) \quad (A3)$$

The offset variance, σ_{off}^2 , with respect to process variation, is calculated as

$$\sigma_{off}^2 = \left(\frac{\partial V_{OS}}{\partial \frac{\mu_P}{\mu_N}} \right)^2 \sigma_{\frac{\mu_P}{\mu_N}}^2 + \left(\frac{\partial V_{OS}}{\partial \frac{W_P}{W_N}} \right)^2 \sigma_{\frac{W_P}{W_N}}^2 + \left(\frac{\partial V_{OS}}{\partial \frac{L_N}{L_P}} \right)^2 \sigma_{\frac{L_N}{L_P}}^2 + \left(\frac{\partial V_{OS}}{\partial V_{TN}} \right)^2 \sigma_{V_{TN}}^2 + \left(\frac{\partial V_{OS}}{\partial V_{TP}} \right)^2 \sigma_{V_{TP}}^2 \quad (A4)$$

which can be rewritten as

$$\sigma_{off}^2 = \left(\frac{nV_T}{2} \right)^2 \left[\frac{\sigma_{\mu_P}^2}{\mu_P^2} + \frac{\sigma_{\mu_N}^2}{\mu_N^2} + \frac{\sigma_{W_P}^2}{W_P^2} + \frac{\sigma_{W_N}^2}{W_N^2} + \frac{\sigma_{L_P}^2}{L_P^2} + \frac{\sigma_{L_N}^2}{L_N^2} \right] + \frac{1}{4} (\sigma_{V_{TN}}^2 + \sigma_{V_{TP}}^2) \quad (A5)$$

From Pelgrom's model in [24], the variance of mobility and threshold voltage are inversely proportional to the area occupied by the transistor, while the variance of the length and the width are inversely proportional to the width and the length of the transistor, respectively. Moreover, in the case of an inverter, the area of the PMOS transistor, $Area_P$, is equal to $\beta Area_N$, where $Area_N$ is the area of the NMOS transistor and β is a multiplying factor. Hence, considering that the area of the inverter, $Area_{INV}$, is equal to $Area_P + Area_N$, each transistor area can be expressed as

$$Area_N = \frac{1}{(1 + \beta)} Area_{INV} \quad (A6)$$

$$Area_P = \frac{\beta}{(1 + \beta)} Area_{INV} \quad (A7)$$

Substituting (A7) and (A6) into (A5), it is straightforward to relate σ_{off}^2 with the area of the inverter, $Area_{INV}$, through Pelgrom's model [24]. Highlighting the strength of the inverter, X_{INV} , with respect to the minimum one, we get

$$\sigma_{off}^2 \propto \frac{1}{Area_{INV}} = \frac{1}{X_{INV} \cdot Area_{INV,min}} \quad (A8)$$

Finally, in the case of two matched inverters, as in the case of the pre-amplifier of the discussed comparators, the overall offset variance is the sum of each single inverter contribution:

$$\sigma_{off,tot}^2 = \sigma_{off,1}^2 + \sigma_{off,2}^2 \propto \frac{2}{X_{INV} \cdot Area_{INV,min}} \quad (A9)$$

Then, the offset standard deviation is given by the square root of the variance

$$\sigma_{off} \propto \frac{\sqrt{2}}{\sqrt{X_{INV} \cdot Area_{INV,min}}} \quad (A10)$$

References

1. Volkmann, J. Deep Brain Stimulation for the Treatment of Parkinson's Disease. *J. Clin. Neurophysiol.* **2004**, *21*, 6. [[CrossRef](#)] [[PubMed](#)]
2. Hannan, M.A.; Mutashar, S.; Samad, S.A.; Hussain, A. Energy harvesting for the implantable biomedical devices: Issues and challenges. *BioMed Eng. Online* **2014**, *13*, 79. [[CrossRef](#)] [[PubMed](#)]
3. Hong, Y.J.; Jeong, H.; Cho, K.W.; Lu, N.; Kim, D.H. Wearable and Implantable Devices for Cardiovascular Healthcare: From Monitoring to Therapy Based on Flexible and Stretchable Electronics. *Adv. Funct. Mater.* **2019**, *29*, 1808247.
4. Karthick, R.; Ramkumar, R.; Akram, M.; Vinoth Kumar, M. Overcome the challenges in bio-medical instruments using IOT—A review. *Mater. Today Proc.* **2021**, *45*, 1614–1619. [[CrossRef](#)]
5. Aledhari, M.; Razzak, R.; Qolomany, B.; Al-Fuqaha, A.; Saeed, F. Biomedical IoT: Enabling Technologies, Architectural Elements, Challenges, and Future Directions. *IEEE Access* **2022**, *10*, 31306–31339.
6. Privitera, M.; Ballo, A.; Ali, K.; Grasso, A.D.; Alioto, M. Sub- μ W Battery-Less and Oscillator-Less Wi-Fi Backscattering Transmitter Reusing RF Signal for Harvesting, Communications, and Motion Detection. *IEEE J. Solid-State Circuits* **2024**, 1–12.
7. Catania, A.; Gagliardi, F.; Piotto, M.; Bruschi, P.; Dei, M. Ultralow-Power Inverter-Based Delta-Sigma Modulator for Wearable Applications. *IEEE Access* **2024**, *12*, 80009–80019.
8. Van Elzakker, M.; Van Tuijl, E.; Geraedts, P.; Schinkel, D.; Klumperink, E.A.M.; Nauta, B. A 10-bit Charge-Redistribution ADC Consuming 1.9 μ W at 1 MS/s. *IEEE J. Solid-State Circuits* **2010**, *45*, 1007–1015. [[CrossRef](#)]
9. Majidzadeh, V.; Silay, K.M.; Schmid, A.; Dehollain, C.; Leblebici, Y. A fully on-chip LDO voltage regulator with 37 dB PSRR at 1 MHz for remotely powered biomedical implants. *Analog Integr. Circ. Signal Process.* **2011**, *67*, 157–168. [[CrossRef](#)]
10. Wang, S.H.; Hung, C.C. A 0.3V 10b 3MS/s SAR ADC with Comparator Calibration and Kickback Noise Reduction for Biomedical Applications. *IEEE Trans. Biomed. Circuits Syst.* **2020**, *14*, 558–569. [[CrossRef](#)]
11. Di Patrizio Stanchieri, G.; Aiello, O.; De Marcellis, A. A 0.4 V 180 nm CMOS Sub- μ W Ultra-Compact and Low-Effort Design PWM-Based ADC. In Proceedings of the 2024 IEEE International Symposium on Circuits and Systems (ISCAS), Singapore, 19–22 May 2024; pp. 1–5. ISSN 2158-1525. [[CrossRef](#)]
12. Toledo, P.; Rubino, R.; Musolino, F.; Crovetto, P. Re-Thinking Analog Integrated Circuits in Digital Terms: A New Design Concept for the IoT Era. *IEEE Trans. Circuits Syst. II Express Briefs* **2021**, *68*, 816–822.
13. Toledo, P.; Crovetto, P.; Klimach, H.; Bampi, S. A 300mV-Supply, 2nW-Power, 80pF-Load CMOS Digital-Based OTA for IoT Interfaces. In Proceedings of the 2019 26th IEEE International Conference on Electronics, Circuits and Systems (ICECS), Genoa, Italy, 27–29 November 2019; pp. 170–173. [[CrossRef](#)]
14. Toledo, P.; Crovetto, P.; Aiello, O.; Alioto, M. Fully Digital Rail-to-Rail OTA with Sub-1000- μ m² Area, 250-mV Minimum Supply, and nW Power at 150-pF Load in 180 nm. *IEEE Solid-State Circuits Lett.* **2020**, *3*, 474–477. [[CrossRef](#)]
15. Palumbo, G.; Scotti, G. A Novel Standard-Cell-Based Implementation of the Digital OTA Suitable for Automatic Place and Route. *J. Low Power Electron. Appl.* **2021**, *11*, 42. [[CrossRef](#)]
16. Centurelli, F.; Giustolisi, G.; Pennisi, S.; Scotti, G. A Biasing Approach to Design Ultra-Low-Power Standard-Cell-Based Analog Building Blocks for Nanometer SoCs. *IEEE Access* **2022**, *10*, 25892–25900. [[CrossRef](#)]
17. Privitera, M.; Crovetto, P.; Grasso, A.D. A Novel Digital OTA Topology With 66-dB DC Gain and 12.3-kHz Bandwidth. *IEEE Trans. Circuits Syst. II* **2023**, *70*, 3988–3992. [[CrossRef](#)]
18. Weaver, S.; Hershberg, B.; Moon, U.K. Digitally Synthesized Stochastic Flash ADC Using Only Standard Digital Cells. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2014**, *61*, 84–91.
19. Aiello, O.; Crovetto, P.; Alioto, M. Fully Synthesizable, Rail-to-Rail Dynamic Voltage Comparator for Operation down to 0.3 V. In Proceedings of the 2018 IEEE International Symposium on Circuits and Systems (ISCAS), Florence, Italy, 27–30 May 2018; pp. 1–5, ISSN 2379-447X. [[CrossRef](#)]
20. Li, X.; Zhou, T.; Ji, Y.; Li, Y. A 0.35 V-to-1.0 V synthesizable rail-to-rail dynamic voltage comparator based OAI&AOI logic. *Analog Integr. Circ. Signal Process.* **2020**, *104*, 351–357. [[CrossRef](#)]
21. Aiello, O.; Crovetto, P.; Toledo, P.; Alioto, M. Rail-to-Rail Dynamic Voltage Comparator Scalable Down to pW-Range Power and 0.15-V Supply. *IEEE Trans. Circuits Syst. II Express Briefs* **2021**, *68*, 2675–2679.
22. Della Sala, R.; Centurelli, F.; Scotti, G.; Palumbo, G. Rail to Rail ICMR and High Performance ULV Standard-Cell-Based Comparator for Biomedical and IoT Applications. *IEEE Access* **2024**, *12*, 4642–4659. [[CrossRef](#)]
23. Della Sala, R.; Centurelli, F.; Scotti, G.; Palumbo, G. Standard-Cell-Based Comparators for Ultra-Low Voltage Applications: Analysis and Comparisons. *Chips* **2023**, *2*, 173–194. [[CrossRef](#)]
24. Pelgrom, M.; Duinmaijer, A.; Welbers, A. Matching properties of MOS transistors. *IEEE J. Solid-State Circuits* **1989**, *24*, 1433–1439.
25. Croon, J.; Rosmeulen, M.; Decoutere, S.; Sansen, W.; Maes, H. An easy-to-use mismatch model for the MOS transistor. *IEEE J. Solid-State Circuits* **2002**, *37*, 1056–1064.
26. Yuan, X.; Shimizu, T.; Mahalingam, U.; Brown, J.S.; Habib, K.Z.; Tekleab, D.G.; Su, T.C.; Satadru, S.; Olsen, C.M.; Lee, H.; et al. Transistor Mismatch Properties in Deep-Submicrometer CMOS Technologies. *IEEE Trans. Electron Devices* **2011**, *58*, 335–342.

27. Sheikholeslami, A. Process Variation and Pelgrom's Law [Circuit Intuitions]. *IEEE Solid-State Circuits Mag.* **2015**, *7*, 8–9.
28. T Hart, P.A.; Babaie, M.; Charbon, E.; Vladimirescu, A.; Sebastiano, F. Subthreshold Mismatch in Nanometer CMOS at Cryogenic Temperatures. *IEEE J. Electron Devices Soc.* **2020**, *8*, 797–806.
29. T Hart, P.A.; Babaie, M.; Charbon, E.; Vladimirescu, A.; Sebastiano, F. Characterization and Modeling of Mismatch in Cryo-CMOS. *IEEE J. Electron Devices Soc.* **2020**, *8*, 263–273.
30. Borgmans, J.; Rombouts, P. The Mismatch Performance of Pseudo Digital Ring Oscillators Used in VCO ADCs: PSRR and CMRR. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2023**, *70*, 579–592.

Disclaimer/Publisher's Note: The statements, opinions and data contained in all publications are solely those of the individual author(s) and contributor(s) and not of MDPI and/or the editor(s). MDPI and/or the editor(s) disclaim responsibility for any injury to people or property resulting from any ideas, methods, instructions or products referred to in the content.