



Article

Investigation of Short Channel Effects in $\text{Al}_{0.30}\text{Ga}_{0.60}\text{As}$ Channel-Based Junctionless Cylindrical Gate-All-Around FET for Low Power Applications

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Abstract: In this work, a cylindrical gate-all-around junctionless field effect transistor (JLFET) was investigated. Junctions and doping concentration gradients are unavailable in JLFET. According to the results, the suggested device has a novel architecture that significantly enhances transistor performance while exhibiting a decreased vulnerability to short-channel effects (SCEs). The Atlas 3D device simulator has been used to analyze the proposed JLFET's performance, especially for low-power applications for different channel lengths ranging from 10 nm to 60 nm with $\text{Al}_{0.30}\text{Ga}_{0.60}\text{As}$ as III-V materials. The comparative simulated study has been based on various performance parameters, including subthreshold slope (SS), drain-induced barrier lowering (DIBL), transconductance, threshold voltage, and I_{ON} to I_{OFF} ratio. The results of the simulations demonstrated that the III-V JLFET exhibited a favorable SS and decreased DIBL compared to other circuit topologies. In the suggested study, gallium arsenide (GaAs) and its compound materials have demonstrated a strong correlation between the SS and DIBL values. The SS is approximately 63 mV/dec, extremely near the ideal 60 mV/dec value. Gallium arsenide (GaAs) and aluminum gallium arsenide (AlGaAs) exhibit DIBL of approximately 30 mV/V and an SS value of around 64 mV/dec.



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Keywords: gate-all-around junctionless FET; III-V compound materials; drain-induced barrier lowering; subthreshold slope

1. Introduction

Device miniaturization has been an essential technique over the past years to meet the electronics industry's low-power, high-speed, and high-density chip needs [1,2]. Due to aggressive scaling, transistors have been scaled down to nanometer dimensions close to physical limits [3,4]. Industries utilize Moore's law to establish goals for R&D and direct long-term planning. Nonetheless, in the current context, Moore's law is approaching its limits, and conventional transistors (CTs) are becoming nanoscale in size, making the challenge of minimizing short-channel effects (SCEs) more important. To control the massive leakage currents and SCEs and pave the way further for transistor scaling, researchers have been looking into new technologies for non-conventional transistors (NCTs), such as SOI (Silicon on Insulator) MOS architecture, FinFET, Double Gate MOSFET (DG-MOSFET), and various Multigate MOSFET configurations [5].

CTs are replaced with novel transistors to meet the constant demand for high-frequency and low-power devices. Moore's law illustrates the exponential curve's decreasing size,

where the number of transistors doubles every two years. This law was modified after a few years, increasing the number of transistors roughly every 18 months. The semiconductor companies have adopted his prognosis, which has been proven accurate. The International Technology Roadmap for Semiconductors (ITRS), a standard for the semiconductor industries, is updated using this regulation. It illustrated how the ITRS roadmap has changed over the years and demonstrated how this curve is saturating and leveling off at very high frequencies and in the current environment [6].

SCEs that impede the performance improvement of CMOS technology, such as SS, DIBL, mobility issues, parasitic capacitance, reliability, and breakdown phenomena, are becoming increasingly important to overcome in VLSI technology due to the shrinking CTs. There is a severe need to search for other architectures of various NCTs. Current research shows that in today's landscape, there are several performance benefits such as reduced DIBL, leakage current reduction, improved I_{ON}/I_{OFF} , better SS, low cost, and low power consumption of NCTs.

Various channel materials are used to enhance the performance of MOS devices, including strained silicon and germanium [7]. Lateral field diffusion is reduced, and the conducting channel is completely under gate control when MOS devices reach a specific scale in the submicron range. The lateral field is decreasing due to an increase in substrate doping. As the doping in the substrate grows, a strong bond between the substrate and the channel is formed, and the size of the depletion layer beneath the channel shrinks. A small amount of oxide is decreased in size to enhance the gate-channel interaction. Because of the gate oxide's shrinkage, threshold voltage control is required. The threshold voltage fluctuates more with a strongly doped substrate [7]. This process creates devices by placing tiny silicon pieces on a substrate, often an insulator such as SiO_2 . By using an insulating substrate to separate the Si layer from the wafer body, SOI lessens the impact of parasitic capacitances, which are caused by junction capacitances. Due to the presence of an insulator in SOI, the depletion region cannot be extended into the substrate. Hence, the capacitance at the junction is reduced, reducing RC delays and providing the high-speed performance of SOI devices at lower V_{DD} [8].

Two primary ways to obtain SOI devices are partially depleted SOI MOSFETs (PDSOI) and fully depleted SOI MOSFETs (FDSOI) [9]. PDSOI features a doped channel and a broad insulating buried oxide. Top Si typically has a thickness of 50–90 nm. For a partially depleted MOSFET, the silicon film thickness is more than the bulk depletion width; for a fully depleted MOSFET, it is less than the gate depletion width. Fully depleted MOSFETs are essentially free from KINK effects, although partially depleted MOSFETs are frequently affected by them; in PDSOI MOSFETs, a phenomenon known as the "kink effect" results in an abrupt rise in drain current. Injecting holes into the MOSFET's floating substrate causes this effect, which lowers the threshold voltage and raises the body potential. The cycle is repeated when more holes are created due to the increased drain current. In logic circuits, the kink effect helps with speed and current drive but hinders analog circuits' linearity [10]. Low V_{DD} , which leads to low power consumption, less changeable V_{th} , low leakage, high logic density, minimal SCEs, low DIBL, excellent SS, diode leakage, and minimum junction capacitance, is one of the many benefits of FDSOI [11].

DG-MOSFETs are one of the most promising device topologies for future advancements in immunity against SCEs because of their capacity to regulate electrostatic integrity, or SCEs, in ultra-scaled MOS structures [12,13]. FinFET's optimal gate length to fin width ratio has made it a better choice with enhanced SS and DIBL [14,15]. According to several research publications, FinFETs exhibit superior gate controllability, a lower SS, a larger I_{ON}/I_{OFF} ratio, and an improved DIBL compared to its regular planar equivalent. FinFET's non-planar characteristic promotes investigation of the multigate structure [16,17].

Due to device miniaturization technique or scaling, submicron and deep submicron technology have evolved, and simultaneously, SCEs are increasingly becoming more prominent in CTs. Source/drain, substrate, and gate engineering have provided solutions for addressing the leakage currents and reducing SCEs and narrow channel effects (NCEs). Geometrical edge effects are used to explain this narrow channel phenomenon. The transition from the field oxide depletion zone to the gate oxide depletion region becomes comparable to the gate width as the channel width decreases, making it impossible to ignore while determining the threshold voltage equation. The advent of the new device, JLFET, as a potential substitute for CTs, has come about due to the aggressive scaling of CTs during the era of nano-engineering or nanowires. In this work, cylindrical gate-all-around JLFETs have been thoroughly examined, and their performance has been evaluated compared to CTs. The outcomes of the study of JLFET hold significant relevance to the field of semiconductors and superconductors, especially in the context of energy-efficient electronic devices and integrated circuits. Due to device miniaturization, implanting junctions with doping concentrations ranging from 10^{19} to 10^{20} cm^{-3} within the nanoscale gate length is challenging [18]. Researchers have proposed the innovative idea of JLFET replacing CT. Since conventional MOSFETs cannot regulate SCEs, non-conventional JLFET architecture has emerged, and the findings indicate that JLFETs are more resistant to SCEs than CT [19].

2. Mathematical Modelling of JLFET

JLFET is a kind of device fully depleted in the subthreshold region and moderately accumulated in the ON state. For both long- and short-channel cases, theoretical investigations have been performed on modeling cylindrical gate-all-around JLFETs. Notably, long-channel models lack the accuracy for short-channel cases. The advent of profound submicron technology has led to the increased requirement of integration density. The proposed study employs an analytical model based on the two-dimensional Poisson equation's estimated solution and subthreshold properties [20]. The mathematical solutions for drain current under various bias conditions are shown in Tables 1 and 2.

Table 1. Drain Current Equations for JLFET with Different Bias Conditions [21].

Bias	Drain Current
$V_{GS} > V_{po}$ $V_{GS} < V_{FB}$ $V_{DS} < V_{DSat1}$	$I_D = \frac{q\mu_{bND}}{L_{effb}} \left(\frac{1}{n+1} \frac{S_{max}-S_{min}}{(V_{FB}-V_{po})^n} \left((V_{GS} - V_{po})^{n+1} - (V_{GS} - V_{DS} - V_{po})^{n+1} \right) + S_{min} V_{DS} \right)$
$V_{GS} > V_{po}$ $V_{GS} < V_{FB}$ $V_{DS} > V_{DSat1}$	$I_D = \frac{q\mu_{bND}}{L_{effb}} \left(\frac{1}{n+1} \frac{S_{max}-S_{min}}{(V_{FB}-V_{po})^n} \left((V_{GS} - V_{po})^{n+1} \right) + S_{min} V_{DS} \right)$
$V_{GS} > V_{FB}$ $V_{DS} < V_{DSat2}$	$I_D = \frac{q\mu_{bND}}{L_{effb}} S_{max} C_{ox} + \frac{\mu_{acc} C_{ox} W_{eff}}{L_{effacc}} \left(V_{DS} (V_{GS} - V_{FB}) - \frac{1}{2} V_{DS}^2 \right)$

Table 2. The description of the symbol used in Table 1 [21].

Symbol	Value
V_{po0}	Linear pinch-off voltage at $V_D = 0V$
V_{po}	Pinch-off voltage $V_{po} = V_{po0} - \eta V_{DS}$
η	DIBL coefficient
W_{eff}	Channel Perimeter
S	Neutral (non-depleted) cross-section of the channel: $S = S_{min}$ When the surface is inverted and $S = S_{max}$ When the surface is accumulated.

Table 2. Cont.

Symbol	Value
V_{DSat1}	Drain Saturation Voltage for the neutral bulk channel $V_{DSat1} = \frac{V_{GS} - V_{p00}}{1 - \eta}$
V_{DSat2}	Drain Saturation Voltage for the accumulation channel $V_{DSat2} = V_{GS} - V_{FB}$
L_{effb}	The effective length of the neutral bulk channel
L_{effacc}	The effective length of the accumulation channel
μ_{acc}	Accumulation mobilities
μ_b	Bulk mobilities

3. Theoretical and Simulation Framework

A junctionless transistor is a novel device that eliminates junctions and gradients in doping concentration. JLFET assists in resolving the difficulty of producing high-quality junctions in the semiconductor industry. A gate electrode modulates the resistivity of a strongly doped semiconductor bar in JLFETs, which can be considered a gated resistor. Metal-oxide-semiconductor field effect transistors (MOSFETs), the mainstay of the contemporary semiconductor industry, feature metallurgical junctions at the source-channel and channel-drain interfaces. In contrast, JLFETs are evenly doped and lack these junctions. In addition to a low thermal budget production procedure that is cheaper and easier, this results in several intriguing electrical features. Notably, the researchers have put forth several analytical and numerical approaches to solve the current transport mechanism in JLFET. The approach provides an analytical connection between surface potential models and gate voltage, focusing on Boltzmann statistics and the closed-form solution of Poisson's equation. The behavior of the device, including motion quantization, sub-band splitting, fermi statistics, quasi-ballistic transport, surface and channel orientation, and band structure, has been analyzed using numerical models.

Quasi-ballistic transport in nanowire field-effect transistors has been studied by Gnani et al. They used the one-dimensional Boltzmann transport equation to address the analytical solution for any possible profile while considering elastic scattering. They concluded that the kT layer has no bearing on one-dimensional quasi-ballistic carrier transport, and those inelastic collisions have little effect on nanowires [21,22]. The idea of the kT layer has caused criticism in the device modeling community because of the empirical character of the reasons that introduced it, even though Monte Carlo simulations provided quantitative validity. The theoretical foundation of the kT layer notion has been examined to improve comprehension [22]. It has been demonstrated that the Boltzmann Transport equation can be simplified to a formalism known as the “Quasi Ballistic drift-diffusion” formalism by taking into account one dimension in space, assuming non-degenerate statistics, one single isotropic band, and treating the collision integral by a simple “relaxation length” approximation. The distribution function could be artificially divided into two functions, one for positive velocity and one for negative velocity, both of which have a Maxwellian (thermal) shape and represent the concentration of carriers flowing from source to drain (or, more accurately, from drain to source), according to the BTE solution within these approximations. This method, which approximates semi-classical transport inside the relaxation length approximation framework, incorporates the effects of both arbitrary fields and isotropic scattering, making it a more comprehensive formalism than the kT layer model. E. Gnani et al. explored band effects on the transport characteristics of ultra-scaled silicon nanowires, and the proposed model was validated by a tight binding approach and

fitted transport effective masses [23]. Lenzi et al. have also used deterministic and Monte Carlo methodologies to solve the transport properties of nanowires. They have solved the coupled Schrodinger–Poisson equation to extract the potential profiles for one-dimensional and multi-dimensional sub-bands along the channel [24].

Using the non-equilibrium Green's function formalism, Poli et al. [25] offered insights into the solutions to the 3D Poisson–Boltzmann equation for comprehensive quantum treatment of Coulomb scattering in silicon nanowire FETs. JLFET is a multigate FET with no doping concentration gradients. Due to less and more manageable fabrication steps involved in JLFET, it is the best replacement for traditional CTs [26–28]. Tyndall's lab has created junctionless nanowire transistors with gate lengths as small as 50 nm [29]. The nanowires and the gates were patterned using electron beam lithography, and the gate oxide thickness was 5 nm. Diffusion does not occur in JLFETs because there are no junction gradients between the source and drain. It dramatically reduces costs and eliminates the need for pricey annealing processes. The doping concentration in JLFETs typically varies from 10^{19} to 10^{20} cm^{-3} and is consistent and uniform throughout the device. Rather than relying on surface conductivity, the JLFET uses bulk conduction. The significant concern regarding the fabrication of JLFET is to make the semiconductor layer as thin and narrow to support the complete depletion of carriers in OFF condition, and the doping concentration should be as high to provide an excellent current drive in ON condition [30].

In the present scenario, researchers have provided evidence that III-V materials are more immune to SCEs than other CTs. These materials have become an essential substitute for silicon, and they play a massive role in the replacement of silicon and support the fabrication industry in the future. They have excellent current drive capability and high mobility without increasing gate capacitances. The influence of III-V material during manufacturing allows for precise bandgap and control over doping, compositions, and device dimensions. Using quantum mathematical simulations and suppression of source-drain tunneling, some researchers demonstrated the electrical performance of III-V materials, such as GaAs, and obtained currents of up to $100 \text{ nA}/\mu\text{m}$ using a 0.65 V power supply. According to certain studies, indium arsenide (InAs) is the ideal alternative to silicon channels because it has a low DIBL and an excellent SS. Over the past fifty years, advancements in logic performance and an increase in the density of silicon complementary metal-oxide-semiconductor (CMOS) transistors have propelled the exponential growth in electronics power. However, silicon transistor scaling is currently at its limit and might end the revolution in microelectronics. Due to this, the focus is shifting to a family of materials called group III-V compound semiconductors. The construction of the first logic transistors at the nanometer scale may be greatly aided by these materials' exceptional electron transport capabilities [31–33].

Nobrega et al. have compared silicon and III-V nanowire gate-all-around field effect transistors for different gate oxides. They simulated GaAs-based gate-all-around JLFET and reported SS with 58.2 mV/dec at 293.15 K, near the ideal 60 mV/dec [34]. Many research articles consider III-V material as a channel composition, such as germanium, gallium arsenide, indium arsenide, and indium phosphide [35]. Arefin et al. have discussed the impact of III-V material on the threshold voltage sensitivity of the device. They have provided results based on minimum and maximum threshold voltage variations for indium arsenide and silicon [36].

4. Device Structure of JLFET with III-V Materials

The three-dimensional JLFET with cylindrical gate-all-around design and III-V materials has undergone a thorough subthreshold study [37]. As shown in Figure 1, this proposed architecture has been comparatively studied with varying gate lengths of 10 nm,

20 nm, 30 nm, 40 nm, 50 nm, and 60 nm with a constant radius of 10 nm $\text{Al}_{0.30}\text{Ga}_{0.60}\text{As}$ semiconductor. As shown in Figure 1, this proposed device structure has been developed with the $\text{Al}_{0.30}\text{Ga}_{0.60}\text{As}$, Aluminium Gallium Arsenide (in composite form) as channel material having gate length varying from 10 nm to 60 nm and constant radius of 10 nm $\text{Al}_{0.30}\text{Ga}_{0.60}\text{As}$ semiconductor. The ITRS road plan has led to geometrical settings and mesh design, and this important work has ultimately produced the required technology node and feature size [38]. With the help of extensive 3D simulations conducted with SILVACO TCAD (ATLAS Device Simulator version: atlas 5.22.1.R) tools, it is shown here that the presented device exhibits better performance than the other NCTs and CTs with silicon.

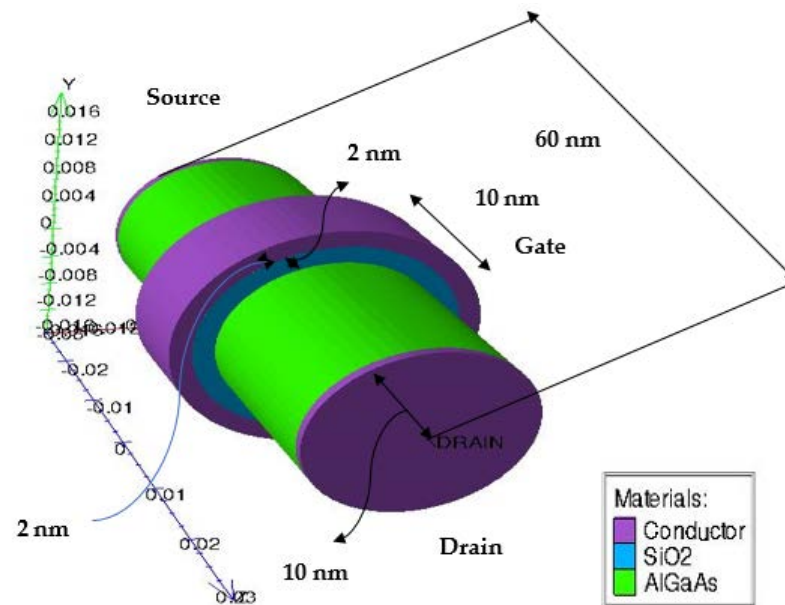


Figure 1. 10 nm structure of $\text{Al}_{0.30}\text{Ga}_{0.60}\text{As}$ Channel-based JLFET.

The 3D cylindrical design has a Radius mesh (R in μm), Angle mesh (A in degrees), and Length mesh (Z in μm). In TACD simulation for 3D design, the radial dimension of the device is discretized using the Radius mesh (R in μm). For junctionless FETs, the electrical behavior mostly depends on surface potential charges and quantum confinement effects. A finer Radius mesh is preferred for mesh density selection, and all the numerical solutions for Poisson's and Schrödinger's equations depend on mesh density selection. Angle mesh (A in degrees) is used for discretization azimuthally into an angular position in a cylindrical 3D device. This segmentation simulates non-uniformities in carrier transport, charge distribution, fringing fields, and azimuthal changes in current flow with high angular resolution. Length mesh (Z in μm) provides discretization along the longitudinal axis of the device from the source to the drain terminals. The selection of this segmentation influenced the SCEs, carrier transport processes, and channel potential changes. Finer Length mesh is essential for high resolution and accuracy of the electric field profile, velocity saturation, ballistic transport, and scattering effects simulation. The 3D cylindrical design has five regions with different materials, i.e., 1— $\text{Al}_{0.30}\text{Ga}_{0.60}\text{As}$ used as a semiconductor/channel material, 2— SiO_2 as an insulator, 3. P^+ polysilicon is used as the gate electrode (metal gate), P^+ polysilicon is used as a source contact (metal source), and P^+ polysilicon is also used as a drain contact (metal drain).

The Shockley–Read–Hall and AUGER recombination models were used to analyze recombination effects for high current densities. NEWTON and GUMMEL models were incorporated into equations with coupled and decoupled forms. This paper describes the simulation of the electrical characteristics of novel transistor JLFET with gate-all-

around architecture using ATLAS 3-D device simulator for different channel materials such as Gallium Arsenide (GaAs), Indium Phosphide (InP), Gallium Nitride (GaN), Gallium Phosphide (GaP), Aluminium Gallium Arsenide Phosphide (AlGaAsP), Indium Gallium Arsenide Phosphide (InGaAsP), Aluminium Gallium Arsenide (AlGaAs) and their different compositions such as $\text{Al}_{0.20}\text{Ga}_{0.80}\text{As}$ and $\text{Al}_{0.30}\text{Ga}_{0.60}\text{As}$. The coordinates for the cylindrical structure involved three electrodes: Drain, Source, and Gate. The device parameters of the proposed device are noted in Table 3.

Table 3. Device parameters related to Figure 1.

Parameters	for Cylindrical Gate-All-Around JLFET
Channel Material	$\text{Al}_{0.30}\text{Ga}_{0.60}\text{As}$, Aluminium Gallium Arsenide (in composite form)
Channel region with Doping Concentration	N-type— 10^{19} cm^{-3}
Source region with Doping Concentration	N-type— 10^{19} cm^{-3}
Drain region with Doping Concentration	N-type— 10^{19} cm^{-3}
Gate material	P^+ Polysilicon
Gate Workfunction	5.4 eV
Oxide Permittivity	3.9
Channel Length	10 nm
Gate Conductor Thickness	2 nm
Oxide Thickness	2 nm
Semiconductor ($\text{Al}_{0.30}\text{Ga}_{0.60}\text{As}$, Substrate)	10 nm (radius)
Device Length	60 nm

Properties of AlGaAs

AlGaAs has numerous uses in the semiconductor industry. Since it is almost lattice-matched with GaAs, it is utilized in heterostructures to enable the development of heterostructures with low mechanical stresses. Fermi-level pinning at the nanowire surface can be lessened by the AlGaAs shell [39]. It is also employed in GaAs-based heterostructure devices as a barrier material. For instance, electrons are confined to a GaAs region by the AlGaAs layer in a quantum well-infrared photodetector (QWIP). With the combination of gallium arsenide and aluminum, the semiconductor material $\text{Al}_x\text{Ga}_{1-x}\text{As}$ has a larger bandgap than gallium arsenide but nearly the same lattice constant. It is an alloy between gallium arsenide and aluminum arsenide, which is indicated by the x in the formula, which is a value between 0 and 1. AlGaAs is a zincblende crystal with a bandgap that ranges from 2.16 eV (AlAs) to 1.42 eV (GaAs). When x is less than 0.4, the bandgap is direct. One of the most significant alloy systems in terms of technology is the $(\text{Al}_x\text{Ga}_{1-x}\text{As})$ system, particularly when paired with gallium arsenide (GaAs). It is the foundation for single-barrier, quantum-well, and superlattice device topologies, significantly impacting high-speed electronic gadgets. Thus, having the constants n and k spanning a broad spectral range and over the concentration range from $x = 0$ to $x = 1$ would be crucial. Fundamental parameters and electrical characteristics of AlGaAs are explained in Tables 4 and 5.

Table 4. Fundamental Parameters of AlGaAs at 300 K.

Crystal Structure	Zinc Blende
Number of atoms in 1 cm ³	$(4.42 - 0.17x) \cdot 10^{22}$
Debye temperature	$370 + 54x + 22x^2$ K
Density	$5.32 - 1.56x$ g·cm ⁻³
Dielectric constant (static)	$12.90 - 2.84x$
Dielectric constant (high frequency)	$10.89 - 2.73x$
Effective electron mass (me)	$0.063 + 0.083x$ mo ($x < 0.45$)
Density-of-states electron mass (mcd)	$0.85 - 0.14x$ mo ($x > 0.45$)
Conductivity effective mass (mcc)	0.26 mo ($x > 0.45$)
Effective hole masses (mh)	$0.51 + 0.25x$ mo
Effective hole masses (mlp)	$0.082 + 0.068x$ mo
Electron affinity	$4.07 - 1.1x$ eV ($x < 0.45$)
	$3.64 - 0.14x$ eV ($x > 0.45$)
Lattice constant	$5.6533 + 0.0078x$ Å

Table 5. The electrical characteristics of AlGaAs.

Electrical Parameters	Values
Breakdown field	$\approx (4 \div 6)$ 105 V/cm
Mobility electrons	
$0 < x < 0.45$	$8 \cdot 10^3 - 2.2 \cdot 10^4 x + 10^4 \cdot x^2$ cm ² V ⁻¹ s ⁻¹
$0.45 < x < 1$	$-255 + 1160x - 720x^2$ cm ² V ⁻¹ s ⁻¹
Mobility holes	$370 - 970x + 740x^2$ cm ² V ⁻¹ s ⁻¹
Diffusion coefficient electrons	
$0 < x < 0.45$	$200 - 550x + 250x^2$ cm ² /s
$0.45 < x < 1$	$-6.4 + 29x - 18x^2$ cm ² /s
Diffusion coefficient holes	$9.2 - 24x + 18.5x^2$ cm ² /s
Electron thermal velocity	
$0 < x < 0.4$	$(4.4 - 2.1x) \cdot 10^5$ m/s
$0.45 < x < 1$	$2.3 \cdot 10^5$ m/s
Hole thermal velocity	$(1.8 - 0.5x) \cdot 10^5$ m/s

5. Results and Discussion

In this study, JLFET is usually an ON-gated resistor, and due to the work function difference between the gate and silicon nanowire, the threshold voltage is positive. Figure 2 presents the simulated transfer characteristics of JLFET architecture with Al_{0.30}Ga_{0.60}As, III-V material for different channel lengths ranging from 10 nm to 60 nm, and P⁺ Polysilicon has been used to fulfill the requirement of high gate work function to achieve appropriate V_{th} value. It can be observed here that the rapidness of the drain current against the gate voltage increases as the channel length decreases. The threshold voltage value decreased as the channel length decreased, as shown in Figure 3. These I_D-V_{GS} characteristics of the cylindrical gate-all-around Al_{0.30}Ga_{0.60}As channel-based JLFET have been plotted at V_{DS} = 0.01 V, spanning a range of V_{GS} from −0.4 to 1.2 V. The threshold voltages for different

channel lengths have been observed to be $V_{th} = 0.71864309$ V (at 10 nm), 0.92221857 V (at 20 nm), 0.95883678 V (at 30 nm), 0.9691365 V (at 40 nm), 0.97815102 V (at 50 nm) and 0.98420158 V (at 60 nm). The result shows that JLFET can be a potential candidate for ultra-low power applications. It is because, in JLFET, complete depletion can be easily achieved for the OFF state by controlling the work function of gate material, and for the ON state, high doping levels in the nanowire-type substrate support a high current drive [39].

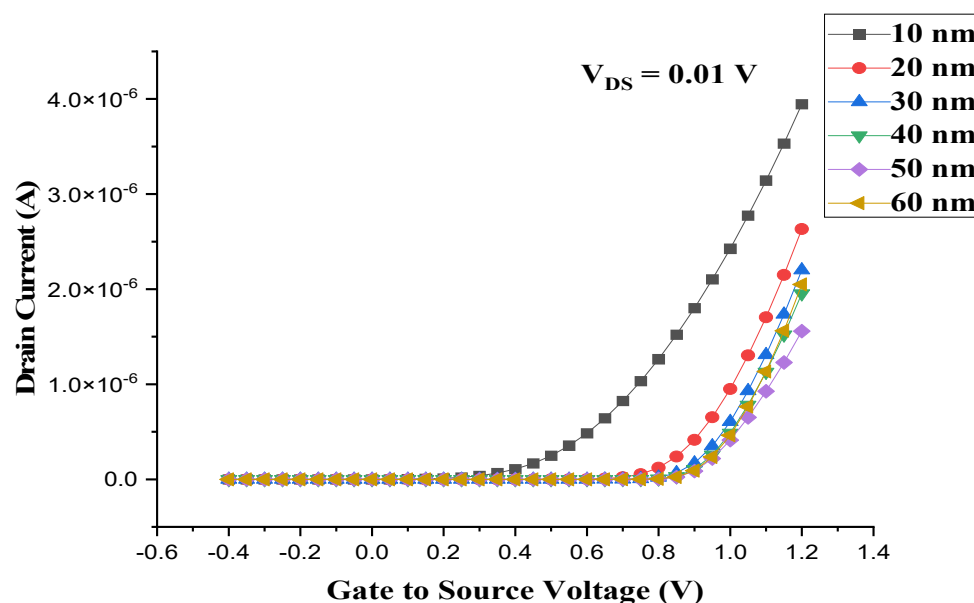


Figure 2. Transfer characteristics of $\text{Al}_{0.30}\text{Ga}_{0.60}\text{As}$ channel-based JLFET with different channel lengths.

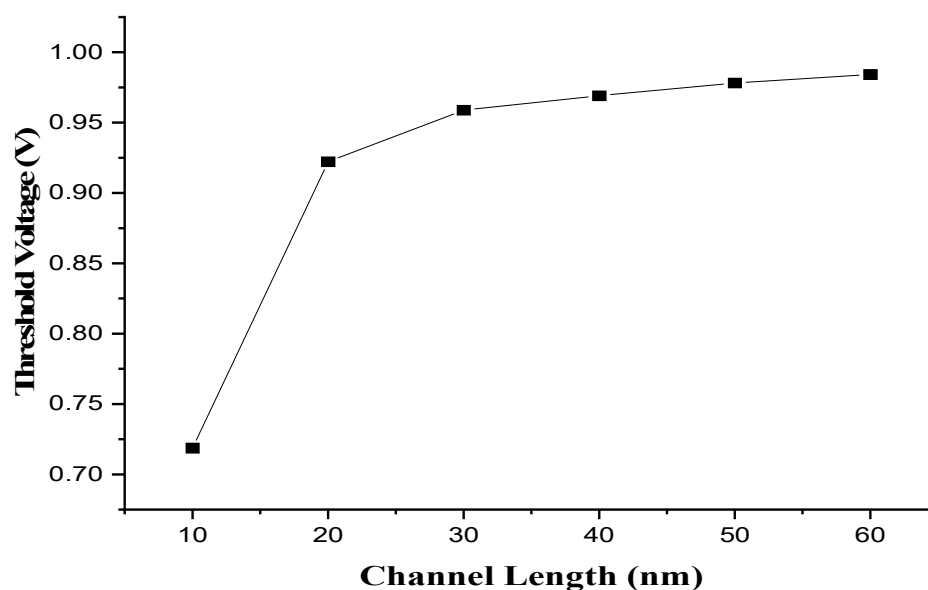


Figure 3. Threshold voltage variation of $\text{Al}_{0.30}\text{Ga}_{0.60}\text{As}$ channel-based JLFET with different channel lengths.

JLFET behaves as a close relative of accumulation mode FET. In heavily doped silicon (about 10^{19} cm^{-3}), the bulk mobility of electrons is low (approximately $60\text{--}80 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$) and can be increased by applying gate voltage. Academic research papers show that JLFET can achieve higher mobility and is currently derived in moderate accumulation mode compared to CTs. Coulomb Scattering can be reduced by screening ionized impurities by the accumulation of electrons. In JLFET, the electric field perpendicular to the current flow is significantly lower than CTs. In CTs, this electric field reduces the inversion channel

mobility, but the lower electric field in JLFET and the absence of carrier scattering lead to a significant breakthrough in high current drive [40].

Figure 4 shows the plot of the electric field distribution versus the distance from the gate electrode along the nanowire for 10 nm and 40 nm $\text{Al}_{0.30}\text{Ga}_{0.60}\text{As}$ channel-based JLFETs. The electric field strength at a particular distance from the gate electrode is proportional to the voltage applied to the gate electrode. The electric field profile is a critical parameter for understanding the behavior of electrons in JLFET. The distribution of the electric field is an essential factor in analyzing any device's performance, and it depends on material properties, doping profiles, and the structure of that device. In AlGaAs JLFET, the electric field lines are more concentrated and sharply defined due to higher current mobility. AlGaAs JLFET has a less diffused electric field distribution and is more concentrated around the gate region, resulting in a more tightly controlled conduction process [41]. For a 10 nm device, the electric field is stronger with a steeper gradient near the surface of the nanowire. This stronger electric field forces the electrons to flow in the nanowire. The result shows that 10 nm JLFET has more current drive than 40 nm JLFET.

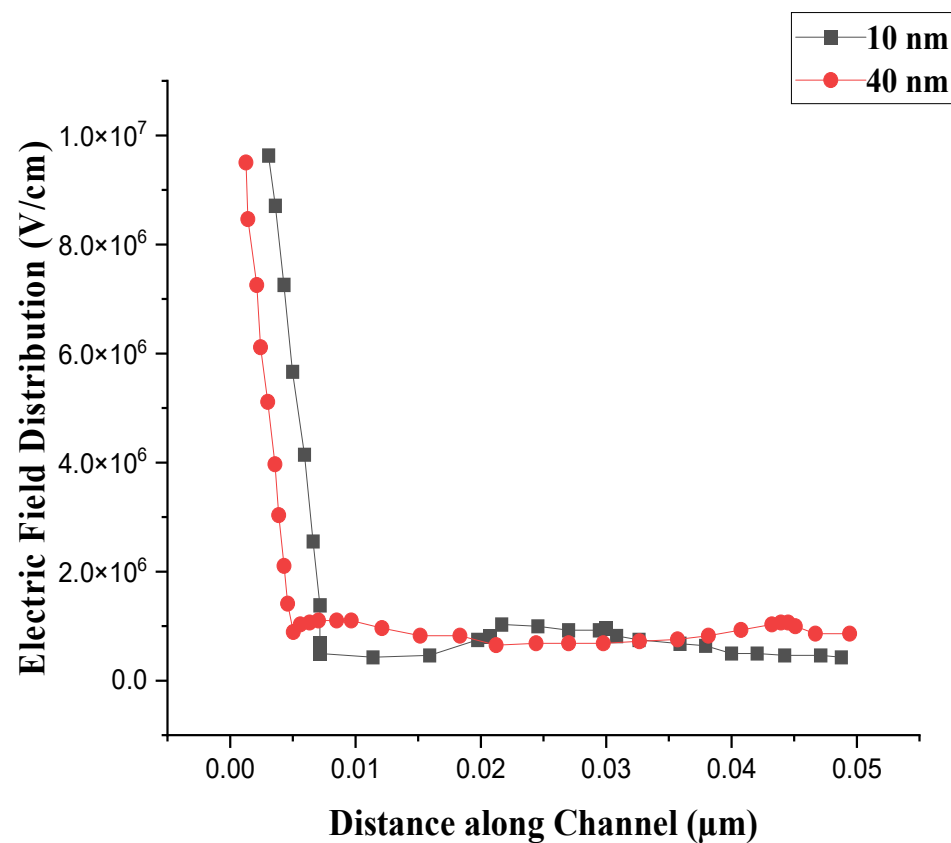


Figure 4. Electric field distribution along the channel for $\text{Al}_{0.30}\text{Ga}_{0.60}\text{As}$ channel-based JLFET.

Figures 5 and 6 show the energy band diagrams for 10 nm and 40 nm $\text{Al}_{0.30}\text{Ga}_{0.60}\text{As}$ channel-based JLFETs. The energy band diagram consists of a conduction band and a valence band. The conduction band is empty at zero bias, and all the electrons occupy only the valence band. The energy levels of the valence and conduction bands shift after applying some external voltage. The result shows that at 40 nm JLFET, the conduction and valence bands are wider than 10 nm JLFET. Due to increasing channel length, the electrons are more tightly coupled with the gate voltage. More energy is required for the current drive. In contrast, for 10 nm JLFET, both energy bands are narrower than 40 nm JLFET and have higher current drives in 10 nm device architecture [42].

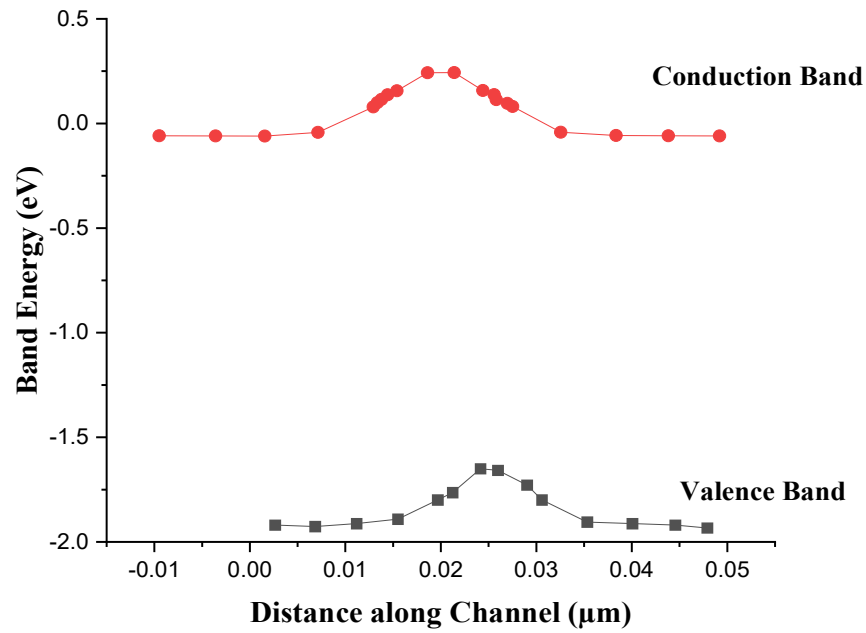


Figure 5. Energy band diagram of $\text{Al}_{0.30}\text{Ga}_{0.60}\text{As}$ Channel-based 10 nm JLFET.

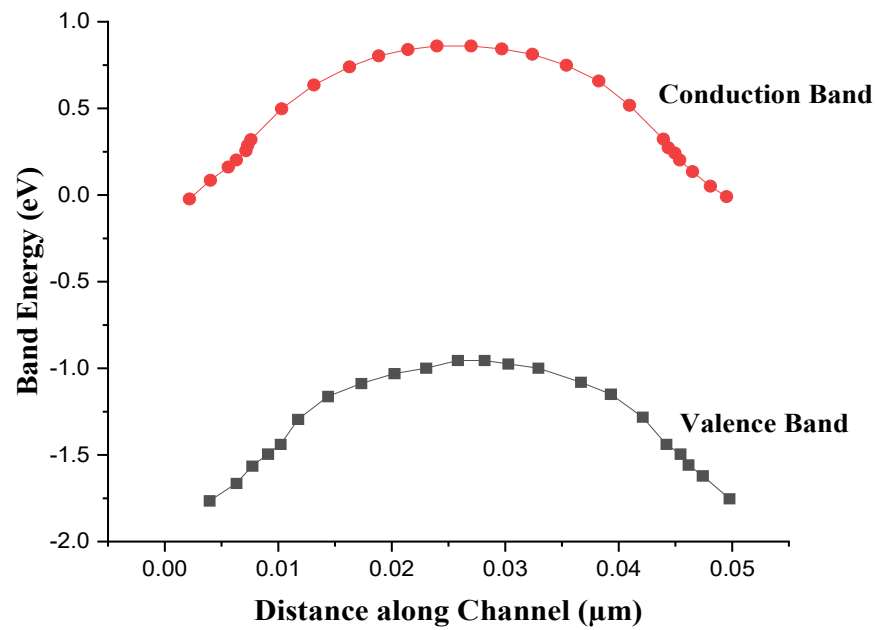


Figure 6. Energy band diagram of $\text{Al}_{0.30}\text{Ga}_{0.60}\text{As}$ Channel-based 40 nm JLFET.

Figure 7 shows the electric potential distribution of a 10 nm and a 40 nm $\text{Al}_{0.30}\text{Ga}_{0.60}\text{As}$ channel-based JLFET. Electric field distribution depends on various factors, including channel doping in the silicon substrate, gate oxide material, and gate-to-source voltage for 40 nm JLFET. There is a significant increase in electric potential energy from the source, and the drain ends with a deeper and broader dip near the gate electrode compared to 10 nm JLFET. The main reason for this is the formation of a more significant depletion layer, which results in a more significant reduction in electric potential in that region [43].

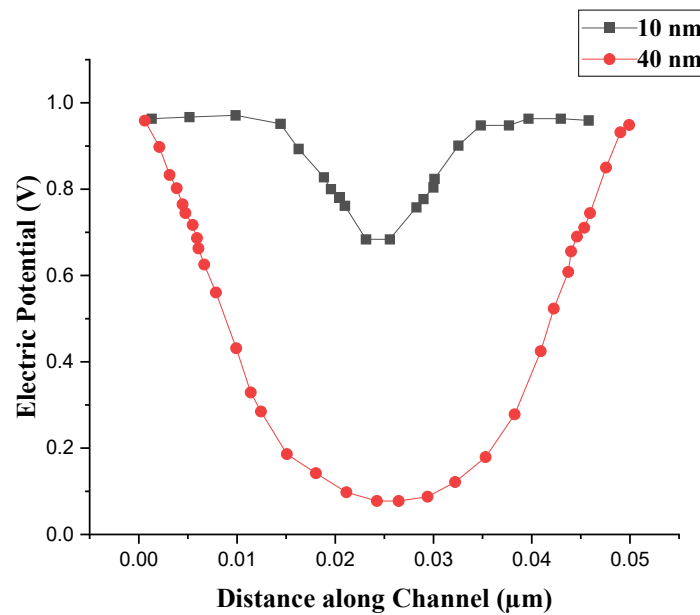


Figure 7. Electric potential distribution along the channel for $\text{Al}_{0.30}\text{Ga}_{0.60}\text{As}$ channel-based JLFET.

Figure 8 shows the 10 nm and 40 nm current flow lines of the $\text{Al}_{0.30}\text{Ga}_{0.60}\text{As}$ channel-based JLFET. In AlGaAs-based JLFET, the current is influenced by drift and diffusion phenomena similar to silicon, but AlGaAs has a direct energy band gap, and the current flow lines are more focused and less spread out than silicon [44]. Because of the shorter channel length that approaches the steeper electric field and higher current density, the current flow lines in the 10 nm device are more concentrated. Enclosing carriers can improve their carrying characteristics but can also cause more dispersion and possible failure. Due to the larger channel length of the 40 nm device, current flow lines are more dispersed, which produces a more even electrical distribution.

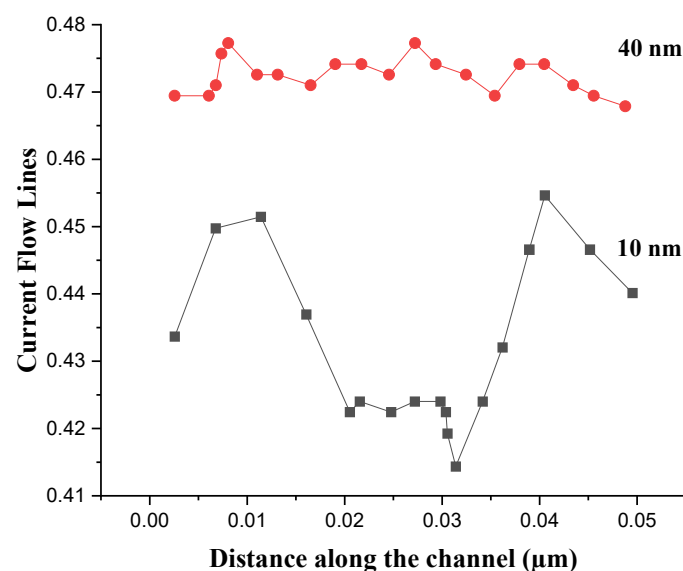


Figure 8. Current flow lines along the channel for $\text{Al}_{0.30}\text{Ga}_{0.60}\text{As}$ channel-based JLFET.

Figure 9 shows the electron concentration of 10 nm and 40 nm $\text{Al}_{0.30}\text{Ga}_{0.60}\text{As}$ channel-based JLFETs. The electron concentration or carrier density is crucial to understand the electrical performance of any device. It can also be influenced by doping, intrinsic properties, and temperature. The electron concentration in AlGaAs JLFET is deeper and higher

than silicon JLFET [45]. More significant doping levels and an improved electric field can typically lead to a larger electron concentration in a 10 nm device. It may result in higher leakage currents and make device control more difficult. However, the electron concentration is usually lower for 40 nm devices, but it is more evenly spread throughout the channel, resulting in stable operation. The longer channel makes better control over carrier concentration possible, lessening leakage currents' effect and enhancing device reliability.

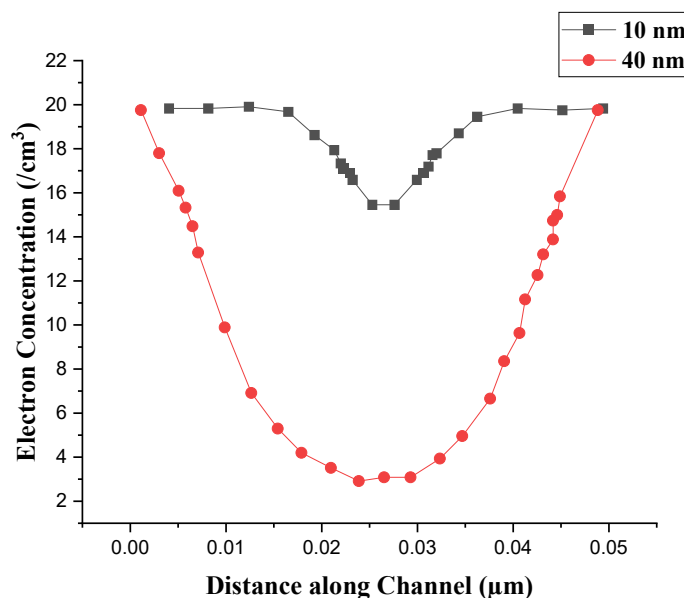


Figure 9. Electron concentration along the channel for $\text{Al}_{0.30}\text{Ga}_{0.60}\text{As}$ channel-based JLFET.

Figure 10 shows the electron mobility of 10 nm and 40 nm $\text{Al}_{0.30}\text{Ga}_{0.60}\text{As}$ channel-based JLFETs. Due to high mobility and wider bandgaps, AlGaAs enable faster electron transport, higher drive currents, and more enhanced electrostatic control than silicon devices [46,47]. Reduced scattering is usually associated with higher electron mobility because a shorter channel facilitates more effective carrier transport. Although the 40 nm device's mobility may be marginally less than that of the 10 nm device, it has advantages such as reduced scattering and more stable operating conditions.

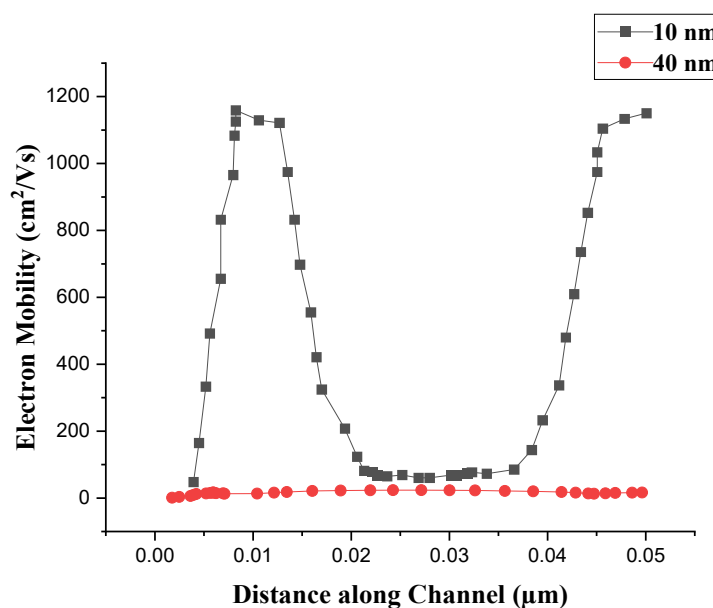


Figure 10. Electron mobility along the channel for $\text{Al}_{0.30}\text{Ga}_{0.60}\text{As}$ channel-based JLFET.

Figure 11 illustrates the I_D - V_{DS} characteristics of the cylindrical gate-all-around $\text{Al}_{0.30}\text{Ga}_{0.60}\text{As}$ channel-based JLFET at $V_{GS} = 1.2$ V, while V_{DS} ranges from 0 to 1 V. This device demonstrates a high ON-state current and a low OFF-state current, showcasing excellent electrostatic control, with a maximum drain current of $2.38548734 \times 10^{-5}$ A (at 10 nm), $1.31566809 \times 10^{-5}$ A (at 20 nm), $9.77385934 \times 10^{-6}$ A (at 30 nm), 8.5672922×10^{-6} A (at 40 nm), $8.33677822 \times 10^{-6}$ A (at 50 nm), and $8.16522822 \times 10^{-6}$ A (at 60 nm), and the saturation slope is about to 4.8060692×10^{-6} A (at 10 nm), 2.1114994×10^{-6} A (at 20 nm), 8.447915×10^{-7} A (at 30 nm), 4.629001×10^{-7} A (at 40 nm), 4.1971784×10^{-7} A (50 nm) and 3.1932996×10^{-7} A (60 nm). It can be understood here that the maximum drain current and saturation slope increase as channel length decreases. Compared to other inversion devices, SCEs are less common in JLFETs. Equation (1) explains how the space charge area connected to the junctions (designated as SCE in the equation) and the expansion of the drain space charge region with drain voltage (designated as DIBL in the equation) cause the threshold voltage to decrease in the junction or other CT devices.

$$V_{th} = V_{tho} - \text{SCE} - \text{DIBL}, \quad (1)$$

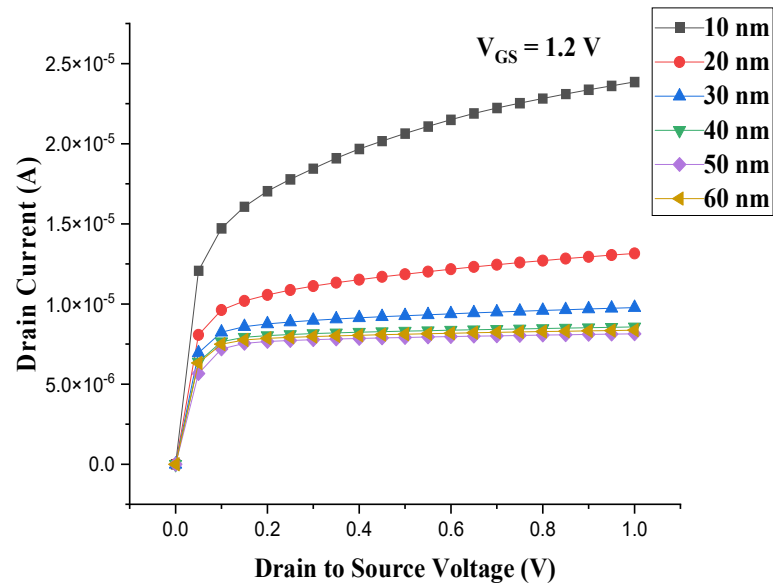


Figure 11. Output characteristics of $\text{Al}_{0.30}\text{Ga}_{0.60}\text{As}$ channel-based JLFET with different channel lengths.

In CTs, the total distance between the source and drain is known as physical gate length (L_{physical}), which is the fabricated gate length of the device and influences overall SCEs. The region within the physical gate length, which actively controls carrier transportation, charge flow, and other subthreshold characteristics, is known as effective gate length (L_{eff}). The region within the physical gate length where SCEs dominate due to threshold voltage roll-off, velocity saturation, DIBL, and other parameters is known as localized short channel effective length (L_{SCE}). In traditional transistors, $L_{\text{SCE}} < L_{\text{eff}} < L_{\text{physical}}$. In JLFET, L_{physical} is the fabricated gate length of the device, defining the scalability and influencing the channel resistance. As we know, in JLFET, there is no pn junction, so L_{eff} is the portion in the channel where depletion modulation provides gate control-dominated conduction, and L_{SCE} is the portion where SCEs significantly impact the conduction process. In concluding remarks, for CTs, $L_{\text{eff}} < L_{\text{physical}}$ due to fringing fields, and $L_{\text{SCE}} < L_{\text{eff}}$ because of the SCE-affected region. However, in JLFET, L_{eff} is mainly driven by the gate field, but L_{SCE} is influenced by depletion width modulation.

In CTs, in most cases, $L_{SCE} < L_{eff}$, where physical gate length is $L_{physical}$, effective gate length is L_{eff} when the device is in ON condition, and effective gate length is L_{SCE} when the device is in OFF condition. In the ON state for JLFET, conduction occurs because the channel remains partially depleted; however, many free carriers are available for carrier transport. In the OFF state for JLFET, the device is effectively turned off due to the depletion of the entire channel. L_{SCE} determines whether residual leakage current persists and becomes more critical for leakage and power dissipation. JLFETs are less subject to SCEs and have excellent SS and DIBL because doping concentration throughout the device length is constant. Mathematical expressions for SS and DIBL are explained in Equations (2) and (3), respectively:

$$\text{Subthreshold Slope} = \frac{dV_G}{d\log I_D} \quad (2)$$

$$\text{DIBL} = V_{th@V_{ds}=50\text{mV}} - V_{th@V_{ds}=1\text{V}} \quad (3)$$

The simulated results for DIBL and SS versus different channel lengths for $\text{Al}_{0.30}\text{Ga}_{0.60}\text{As}$ channel-based JLFET are plotted in Figure 12. The result shows that in JLFET, the high electric field region is placed in the drain, and the gate covers the outer side of this region. The impact of the drain electric field on the channel is much lower than that of CTs, which provide smaller DIBL. Under the threshold, the strongly doped JLFET depletion produces a large electric field perpendicular to the current flow; the field becomes zero above the threshold. A decrease in DIBL characterizes the OFF situation because the drain-source voltage drop does not occur in the channel region, and the blocking of the current is caused by squeezing the carriers out of the channel region [48].

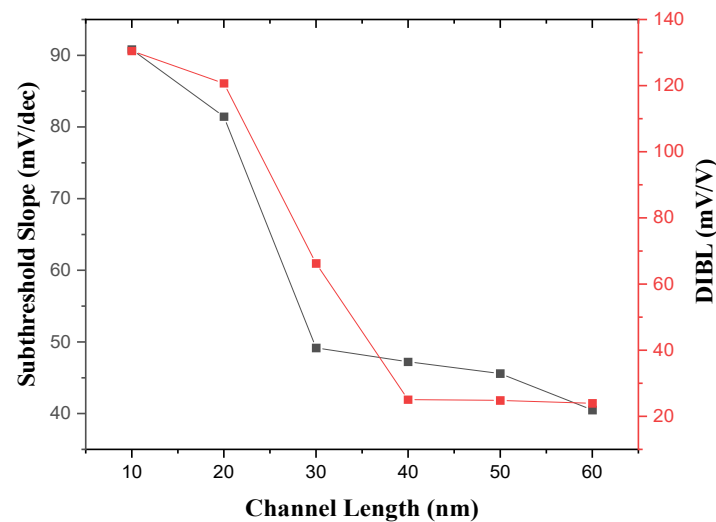


Figure 12. SS and DIBL variation for $\text{Al}_{0.30}\text{Ga}_{0.60}\text{As}$ channel-based JLFET with different channel lengths.

Furthermore, the conduction mechanism in gate-all-around, $\text{Al}_{0.30}\text{Ga}_{0.60}\text{As}$ channel-based JLFET, is compared with different channel lengths in Figure 13. Figure 13 depicts simulated results for I_{ON} and I_{OFF} versus different channel lengths. Moreover, results show that our design boasts some desirable features of JLFET, such as low leakage current and linear variation of drain current with control gate voltage. This device can be an ON & OFF switch in ultra-low power applications. In the ON condition of this device, the large current flows due to the heavily doped source and drain, but in the OFF state, the device cut off due to the work function difference between the gate material and silicon substrate [49].

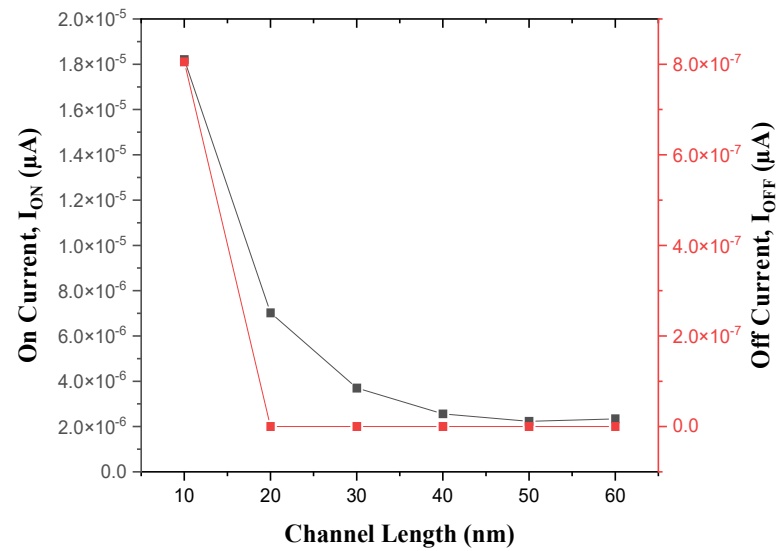


Figure 13. On current and Off current variation for $Al_{0.30}Ga_{0.60}As$ channel-based JLFET with different channel lengths.

Figure 14 illustrates the channel length dependency of the transconductance of cylindrical gate-all-around $Al_{0.30}Ga_{0.60}As$ channel-based JLFET for different channel lengths ranging from 10 nm to 60 nm. Having superior transconductance in JLFET architecture is attributed to its better charge transport properties than other CTs and NCTs. It can be observed here that the value of transconductance increases as channel length increases. Figure 14 illustrates the transconductance profile of $Al_{0.30}Ga_{0.60}As$ channel-based JLFET for different channel lengths and simulation results showing a peak transconductance (gm) value of 1.3×10^{-4} Siemens for 60 nm. The transconductance can be defined as the change in the drain current for change in the gate voltage and can be expressed as the ratio of the gate capacitance to the carrier transit time τ so that $G = 1/2\pi\tau\tau$. The current-to-voltage ratio is commonly referred to as gain. The transconductance versus gate voltage graph shows the relationship between the device's transconductance and gate voltage with constant drain to source voltage and represents any device's amplification capability [50,51].

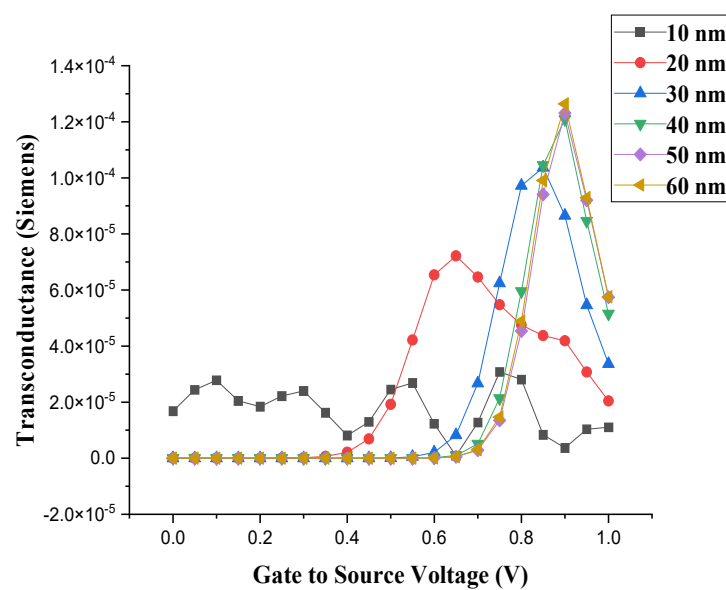


Figure 14. Transconductance variation of $Al_{0.30}Ga_{0.60}As$ channel-based JLFET with different channel lengths.

Transconductance and MOSFET threshold voltage (V_{th}) are closely correlated and depend on gate channel size. Figure 14 demonstrates that the transconductance curve begins at a comparatively low value of g_m for a channel length of 10 nm, indicating modest amplification. On the other hand, the g_m curve climbs steeply for longer channel lengths and increases amplification as the gate voltage increases. The gate voltage at which the derivative of low drain voltage transconductance, dg_m/dV_{GS} (g_{m2}), is highest is known as the threshold voltage. Moreover, JLFET with 60 nm channel length has the highest threshold voltage and transconductance.

Comparative Study of Subthreshold Analysis of JLFET with Different III-V Materials

This paper presents the DC analysis of cylindrical gate-all-around $Al_{0.30}Ga_{0.60}As$ channel-based JLFET investigations with different channel lengths. Table 6 compares the suggested architectures with gate lengths ranging from 10 nm to 60 nm concerning gate length, threshold voltage, maximum drain current, saturation slope, SS, DIBL, on current, and off current. The results indicate that the 10 nm device has the lowest threshold voltages, the highest maximum drain current, and a current and saturation slope. This work shows that the SS of JLFETs with 40, 50, and 60 nm channel lengths is approximately 47 mV/dec, 45 mV/dec, and 40 mV/dec. JLFETs have superior SS and DIBL and are less susceptible to SCEs due to constant doping concentration across the device length. Because the smaller SS demonstrated in this research lowers the OFF current of the transistor, it may be used in low-power applications. Our constructed JLFETs showed the lowest DIBL and SS values, indicating enhanced resilience against short-channel effects. The slope of the gate voltage to the drain current log is known as the SS. It is a crucial parameter for any device's subthreshold analysis. The findings demonstrate that the SS and DIBL values for the suggested task are in good agreement.

Table 6. Performance comparison of the proposed $Al_{0.30}Ga_{0.60}As$ channel-based JLFET with different channel lengths.

L_g (nm)	V_{th} (V)	Saturation Slope (A)	Max. Drain Current (A)	SS (mV/dec)	DIBL (mV/V)	I_{ON} (μA)	I_{OFF} (μA)	I_{ON}/I_{OFF}
10	0.71864309	4.8060692×10^{-6}	$2.38548734 \times 10^{-5}$	90.811026	130.478984	18.2114482	0.80515476	22.61858
20	0.92221857	2.1114994×10^{-6}	$1.31566809 \times 10^{-5}$	81.4501738	120.697472	7.02601295	3.0486378×10^{-8}	230464043
30	0.95883678	8.447915×10^{-7}	$9.77385934 \times 10^{-6}$	49.1701421	66.2491032	3.7020172	$1.85712014 \times 10^{-12}$	$1.99341826 \times 10^{12}$
40	0.9691365	4.629001×10^{-7}	8.5672922×10^{-6}	47.2267559	25.0701147	2.56180952	$3.69007316 \times 10^{-14}$	$6.94243558 \times 10^{13}$
50	0.97815102	4.1971784×10^{-7}	$8.33677822 \times 10^{-6}$	45.5820223	24.8246716	2.22791721	$1.77755482 \times 10^{-15}$	$1.25336062 \times 10^{15}$
60	0.98420158	3.1932996×10^{-7}	$8.16522822 \times 10^{-6}$	40.5020524	23.9363979	2.33849879	$4.15367459 \times 10^{-14}$	$5.62995184 \times 10^{13}$

In this work, the subthreshold analysis of 40 nm cylindrical gate-all-around JLFET with various III-V channel materials has been provided and compared. Table 7 is furnished with 40 nm gate length, threshold voltage, maximum drain current, saturation slope, SS, DIBL, on current, and off current of the proposed structures having silicon as channel material and various channel materials for comparison. The different channel materials such as Gallium Arsenide (GaAs), Indium Phosphide (InP), Gallium Nitride (GaN), Gallium Phosphide (GaP), Aluminium Gallium Arsenide Phosphide (AlGaAsP), Indium Gallium Arsenide Phosphide (InGaAsP), Aluminium Gallium Arsenide (AlGaAs) and their different compositions such as $Al_{0.20}Ga_{0.80}As$ and $Al_{0.30}Ga_{0.60}As$ have been utilized in this work. The result shows that GaAs, $Al_{0.20}Ga_{0.80}As$, and $Al_{0.30}Ga_{0.60}As$ devices have the highest I_{ON}/I_{OFF} of about 1.133861×10^{10} , 4.299456×10^{12} , and 6.942438×10^{13} and they also have the maximum drain current, and saturation slope with the lowest threshold voltages. Materials GaAs and AlGaAs have DIBL of about 30 mV/V and SS value of about 64 mV/dec. Other materials such as $Al_{0.20}Ga_{0.80}As$ and $Al_{0.30}Ga_{0.60}As$, GaP have DIBL about 28 mV/V,

25 mV/V, and 22 mV/V, respectively. GaAs and their compound materials have provided good agreement of the values of SS and DIBL for proposed work with an SS of about 64 mV/dec, which is very close to the ideal value of 60 mV/dec.

Table 7. Performance comparison of various III-V channel materials for 40 nm JLFET according to this work.

Si and III-V Material	V _{th} (V)	Saturation Slope (A)	Max. Drain Current (A)	SS (mV/dec)	DIBL (mV/V)	I _{ON} (μA)	I _{OFF} (μA)	I _{ON} /I _{OFF}
GaAs	0.819608	6.41239×10^{-7}	2.31345×10^{-5}	64.47608	30.5962	12.7614	1.125467×10^{-9}	1.133861×10^{10}
InP	0.656255	-3.1528×10^{-10}	5.02586×10^{-6}	66.8384	39.4156	4.28187	3.6750×10^{-5}	116513.47
AlGaAsP	0.799256	1.01434×10^{-7}	2.91153×10^{-6}	64.44775	40.81138	1.61177	1.717025×10^{-10}	9.386899×10^9
GaN	0.472639	3.99288×10^{-6}	7.14924×10^{-5}	68.34655	40.35768	4.91099	5.031638×10^{-3}	9760.222
InGaAsP	0.656257	-3.1528×10^{-10}	5.02585×10^{-6}	66.83845	39.41564	4.28188	3.675004×10^{-5}	116513.47
GaP	0.552483	8.468×10^{-11}	5.02435×10^{-6}	67.84844	22.50066	4.42848	3.620443×10^{-4}	12231.8586
AlGaAs	0.819837	6.4125×10^{-7}	2.31344×10^{-5}	64.47583	30.59605	12.7615	1.125457×10^{-9}	1.133872×10^{10}
Al _{0.30} Ga _{0.60} As	0.9691365	4.629001×10^{-7}	8.5672922×10^{-6}	47.2267559	25.0701147	2.56180952	$3.69007316 \times 10^{-14}$	$6.94243558 \times 10^{13}$
Al _{0.20} Ga _{0.80} As	0.908568	5.19404×10^{-7}	1.29049×10^{-5}	47.30019	28.52392	5.42004	1.260631×10^{-12}	4.299456×10^{12}

In Table 8, we have finally performed a performance comparison between our device and those available architectures in the literature. Materials, gate length, SS, DIBL, on current, off current, and the ratio of on current to off current are provided in Table 8. Due to their direct energy band gap, better mobility than silicon, and superior SS and DIBL, JLFETs made of III-V materials are less susceptible to SCEs. Additionally, III-V material can have high frequency and speed due to its smaller SS. Our constructed JLFETs showed the lowest DIBL and SS values, indicating enhanced resilience against SCEs. The findings demonstrate that the SS and DIBL values for the suggested task are in good agreement.

Table 8. Performance comparison of the proposed JLFET with other device architectures available in the literature.

Device Architectures	Authors	Materials	L _g (nm)	SS (mV/dec)	DIBL (mV/V)	I _{ON} (μA)	I _{OFF} (μA)	I _{ON} /I _{OFF}
Cylindrical Gate-all-around JLFET (This work)	P. Srivastava et al.	GaAs	40	64.47608	30.5962	12.7614	1.125467×10^{-9}	1.133861×10^{10}
Cylindrical Gate-all-around JLFET (This work)	P. Srivastava et al.	Al _{0.30} Ga _{0.60} As	40	47.22677	25.07014	2.56184	3.690073×10^{-14}	6.942438×10^{13}
Cylindrical Gate-all-around JLFET (This work)	P. Srivastava et al.	Al _{0.20} Ga _{0.80} As	40	47.30019	28.52392	5.42004	1.260631×10^{-18}	4.299456×10^{12}
Symmetric Double Gate JLFET	Talukdar et al. [52]	GaAs	30	65	-	-	-	-
SiGe Double Gate Junctionless MOSFET	Rout et al. [53]	GaSb	20	59.78	-	-	-	7.52×10^{13}
Compound JLFET	Cho et al. [54]	GaAs	40	90	-	-	-	About 10 ⁸

6. Conclusions

Our research included a thorough analysis and evaluation of JLFETs' performance concerning other CTs and NCTs with various channel lengths, especially concerning low-power applications. We developed several JLFET performance metrics, such as transconductance, I_{ON}/I_{OFF}, SS, and DIBL. Our investigation highlighted the outstanding outcomes of the SS of approximately 40 mV/dec and a minimum DIBL of approximately 23 mV/V for 60 nm architecture. Researchers have proposed the innovative idea of JLFET replacing CT. As the traditional MOSFET is not able to control SCEs, the birth of non-conventional JLFET architecture has arrived, and the results show that JLFETs are more highly immune to SCEs than CT and that III-V materials provide higher electron mobility, higher current drive capability and better control over threshold voltage than silicon so that they are especially

promising for high speed and high-frequency applications. Group III-V materials are a class of semiconductors that refer to materials comprising group III elements (such as aluminum, gallium, and indium) and group V elements (such as nitrogen, phosphorus, arsenic, and antimony) of the periodic table. This combination of materials provides distinctive electrical and optoelectronic properties and has a direct energy band gap. High-K dielectrics promise the continuous availability of tiny devices. Selecting a high-K material is essential since the gate dielectric is the fundamental component of a MOSFET. There is still a wide range of dielectrics accessible that have not yet been studied but may hold the key to unlocking the mysteries facing researchers. The results were enhanced by using non-silicon materials with multigate architecture.

Author Contributions: Conceptualization, P.S.; methodology, P.S.; software, P.S.; validation, P.S., A.U., and S.Y.; formal analysis, P.S.; investigation, C.M.S.N.; resources, P.S.; data curation, P.S.; writing—original draft preparation, P.S., A.U., S.Y., C.M.S.N. and A.K.S.; writing—review and editing, P.S., A.U., S.Y., C.M.S.N. and A.K.S.; visualization, C.M.S.N.; supervision, A.K.S. All authors have read and agreed to the published version of the manuscript.

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Abbreviations

The following abbreviations are used in this manuscript:

JLFET	Junctionless field effect transistor
SCEs	Short channel effects
DIBL	Drain-induced barrier lowering
SS	Subthreshold slope
CTs	Conventional Transistors
NCTs	Non-conventional Transistors
ITRS	International Technology Roadmap for Semiconductors
SOI	Silicon on Insulator
FDSOI	Fully depleted silicon on insulator
PDSOI	Partially depleted silicon on insulator.
NCEs	Narrow channel effects

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