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Characterization of the Power Distribution Network for Commercialized STM32s Using a Resonance Frequency Measurement Method †

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Abstract: Power integrity is a critical aspect of microcontroller (MCU) system design. The present tendency of increasing current density and operating frequency, along with decreasing operating voltage, significantly diminishes voltage margins. Given the cost efficiency required for MCU systems, this context places important constraints on the design of the power distribution network (PDN), which directly impacts power supply noise. Therefore, characterizing the PDN is necessary. This paper introduces a cost-effective measurement and modeling method to estimate the die-package resonance frequency of the PDN, a major threat to power integrity. The method, applied to two 32-bit MCUs from STMicroelectronics with varying PDN configurations, enables the identification of the die-package resonance frequency. The results lead to the refinement of the die capacitance model for both cases, with a maximum relative error of less than 7%. The final objective is to implement the measurement system in the die in order to adjust the PDN if necessary.

Keywords: microcontroller; power distribution network; resonance frequency; system modeling

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1. Introduction

Power supply noise has been a primary consideration in system on chip (SoC) designs for several decades. Nowadays, this issue continues to grow as increased current density and operating frequency, along with decreased operating voltage, reduce the supply noise margins. Voltage noise threatens SoC performance and reliability, potentially leading to failure. The power distribution network (PDN) has a significant impact on power supply noise, necessitating the extensive evaluation of power domains through simulations and measurements. Microcontroller (MCU) systems are not exempt from power integrity (PI) issues. Typically, these systems are designed with strong cost constraints to remain competitive, limiting the range of feasible solutions to improve the power supply. Additionally, the wide variety of applications makes analyzing the robustness of a MCU's power supply in various contexts a challenging task [1].

Several methods have been introduced to characterize the PDN through simulations and measurements [2–4]. In an industrial context, the goal is usually to reach a compromise between complexity, necessary resources, and accuracy. This article focuses on the evaluation of a key metric and significant threat of PDN quality: the die-package resonance. A novel method, fitting the cost efficiency required in an industrial context, was proposed in [5], and its application to model the die capacitance was discussed in [1]. Building on this previous work, this paper presents an extensive application of the method to two commercial STM32 MCUs with different consumption levels. Experimental and simulation

results are compared across various decoupling configurations within each case study. This comparison assesses the effectiveness of the proposed technique to characterize the die-package resonance frequency of different types of MCUs, ranging from high-performance to general-purpose applications, while relying on common instrumentation. This work represents the first step toward the larger goal of implementing on-chip a cost-effective PDN characterization solution, relying on the measurement method presented in this paper. This would allow customers to characterize the PDN characteristics of the MCU system running in its end application and adjust them if necessary.

Section 2 provides further details regarding the power integrity context of MCU systems. Section 3 introduces the resonance frequency measurement method. Section 4 details the method's validation and application on a high-power microprocessor unit (MPU), and Section 5 presents its application to a mid-range power MCU. Finally, Section 6 summarizes the main findings and future outlook.

2. Power Integrity Context

It is essential to consider power integrity (PI) in microcontroller design, as PI issues can compromise supply voltage requirements and reduce the system's cost efficiency. To ensure a robust system design and guarantee the correct chip operation, simulations and circuit characterization are required.

2.1. Power Distribution Network

In an MCU system, the PDN is responsible for delivering a stable supply voltage to the chip. Distributed across the entire system, it comprises a voltage regulator module (VRM), a PCB, a package, and an IC. Essentially, any element that generates or transmits power to the chip, from power to ground, is part of the PDN. Decoupling capacitors, usually located on the PCB, play a crucial role by compensating current surges during chip operation, supplying charge within certain frequency ranges. The PDN components exhibit resistive, capacitive, and inductive parasitic behavior, allowing a simplified lumped RLC network to represent the PDN, as depicted in Figure 1.

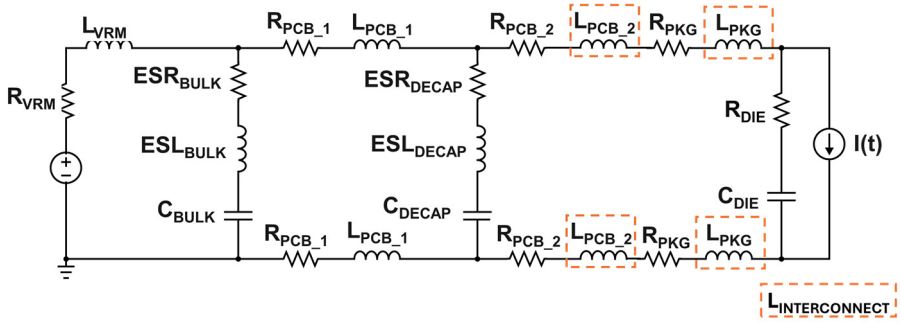

Figure 1. Lumped equivalent representation of a PDN.

In this figure, R_{VRM}, R_{PCB}, and R_{PKG} illustrate the resistive behavior of the VRM, PCB, and package, respectively. Similarly, L_{VRM}, L_{PCB}, and L_{PKG} account for the equivalent inductances of the VRM, PCB, and package, respectively. The die resistive and capacitive contributions are represented by R_{DIE} and C_{DIE}. The bulk and additional decoupling capacitors located on the PCB are represented by their capacitance value as well as their corresponding equivalent series inductance (ESL) and resistance (ESR).

2.2. Power Integrity Risks

A microcontroller system is sensitive to DC IR drop and AC noise at the chip's power rails. During the chip's operation, the current drawn encounters the PDN's parasitics, causing power supply variations. This noise is greatly influenced by the chip's activity and the PDN design. If the PDN is poorly designed, resulting in a high impedance, the noise can become critical and negatively affect chip operation. This is particularly critical

at parallel resonances, impedance peaks resulting from the interaction between a PDN's capacitive element and a parallel inductance. The resonance frequency is expressed by the following equation:

$$f_{res} = \frac{1}{2\pi\sqrt{LC}} \quad (1)$$

Figure 2 illustrates an example of an impedance profile.

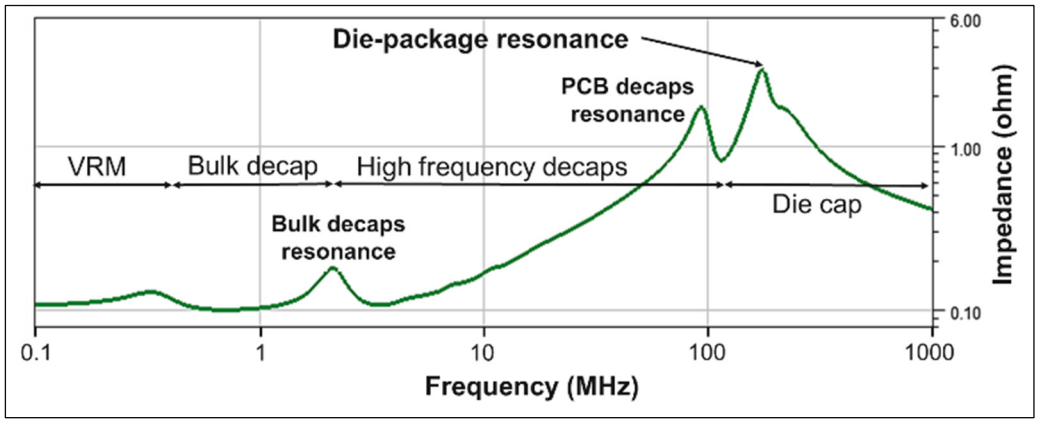

Figure 2. Impedance profile of a PDN.

The most critical resonance usually occurs between the die capacitance C_{DIE} and interconnect inductance $L_{INTERCONNECT}$, which is the loop inductance arising from the nearest decoupling capacitors on the PCB to the chip. Referring to Figure 1, this includes a portion of the total PCB inductance, specifically L_{PCB_2}, as well as the package inductance, L_{PKG}. This resonance is referred to as "main resonance" in the rest of this paper. When a fast current step is drawn, it leads to ringing at the resonance frequency in the power supply. When the overall activity is repetitive at the resonance frequency, this causes significant noise in the power supply over multiple clock cycles, which can reach critical levels and affect the chip's operation. This can induce reliability issues, as well as signal propagation delay variations or jitter on the clock signal, leading to timing margin violations and functional failures [6]. These threats to the chip's correct operation make it essential to estimate and measure supply noise, as well as characterize the PDN.

2.3. PDN Diagnosis

To evaluate the robustness of the MCU, simulations of the power domain are first performed during the design phase. This allows designers to foresee significant power delivery issues with the current design and make necessary adjustments before production. Simulations must be performed in both the frequency and time domains. In the frequency domain, the impedance profile provides valuable information on the PDN parasitics' impact over frequency. Simulations in the time domain are also essential to ensure the robustness of the PDN design. They allow designers to verify that time and voltage margins are respected in the different operating modes. For multi-purpose microcontrollers, with multiple end applications and thus PDN possibilities, it is impossible to simulate all end cases. Usually, the worst case leading to the most critical noise is evaluated [3,4,7]. The accuracy of the simulations depends on the quality of the models used for each element of the PDN. These simulations require a package and board design, along with an evaluation of the die's resistive and capacitive elements. These models must be validated against system measurements in real-life operating conditions, which is a challenging task.

There are several techniques to measure the supply noise or PDN impedance. Most measurements are performed by probing the conducted or radiated noise at the PCB or package level, or by evaluating the PDN impedance using a vector network analyzer (VNA). Such measurements are practical, but equipment parasitics and off-chip probing can alter the measurement precision. To characterize more precisely the PDN and supply noise,

fully embedded solutions were developed. These comprise dedicated on-chip circuits, enabling comprehensive noise measurement at the die level. Several on-chip oscilloscope circuits rely on equivalent time sampling (ETS) to measure high-bandwidth signals [8–11]. This subsampling method requires a periodic measured signal, and digitization is often performed via comparator-based techniques [9–12]. Noise levels are determined by comparing the measured noise to multiple voltage references [9]. Leveraging such circuits, complete on-chip PDN characterization techniques have been developed. They allow for the extraction of the impedance, resonance frequencies, and/or parasitic elements [13–15], using a PDN excitation circuit such as a synthetic current load.

These methods provide valuable insights into PDN parasitic elements and can help improve PDN models, but they may be difficult to implement in a large-scale industrial context. They result in a significant area overhead, often incompatible with the cost constraints of STM32 MCUs. Without such complex solutions, extracting PDN parasitics from the final system in its end application can be difficult. This work proposes a simple, cost-effective external measurement method for determining the main resonance frequency, which characterizes the die capacitance and interconnect inductance. Most techniques in the literature for extracting resonance frequencies involve a dedicated on-chip circuit to excite the PDN [14–19], which increases the cost of the chip. They may also require precise knowledge of the consumption current [15–17,20]. While this approach provides the benefit of determining the PDN impedance, extracting the current can be challenging. Conversely, the method proposed in this work relies exclusively on existing circuits common to all MCUs to excite the PDN and estimates the die-package resonance using only the voltage measurement. The final goal is to embed this solution directly on the chip while maintaining its cost efficiency. This would allow for the adjustment of the PDN or adaptation of the chip operation according to its final environment, namely, the application's PCB.

3. Resonance Frequency Measurement Method

As explained in Section 2, the main resonance frequency depends on the die capacitance and interconnect inductance. By measuring this frequency, we can gain insights into these critical PDN parasitics. The method proposed in this work was developed by leveraging the on-chip pre-existing circuits found in all MCUs and is based solely on noise measurements in order to be versatile and cost-efficient.

3.1. Principle

The switching activity of an MCU at its operating frequency is reflected in its power supply noise, affected by the parasitic elements of the PDN. Utilizing this principle, the method leveraged the phase- locked loop (PLL) that generates the MCU's clock to internally excite the power supply. By evaluating the supply noise while sweeping the PLL frequency across the main resonance frequency range (10–200 MHz), the main resonance frequency can be identified. The method is summarized by the following steps:

- Sweep the PLL frequency within the main resonance frequency range (10 MHz–200 MHz);
- Measure and average the power supply noise at each frequency;
- Apply a fast Fourier transform (FFT) to the averaged voltage;
- Identify the main resonance frequency using the measured noise and its spectrum.

During the measurement, the MCU executes a simple "while (1)" loop. The resulting supply noise is averaged to reduce random parasitic noise and emphasize the periodic pattern. This technique requires a periodic signal to average and a stable oscilloscope trigger for accurate averaging. Despite this, identifying the resonance frequency directly from the noise waveforms can be challenging. Instead, it is easier to analyze the amplitude of the fundamental peaks within each measured spectrum to identify the main resonance frequency. Figure 3 illustrates the measurement process, which is repeated for the entire PLL frequency sweep. Once the voltage noise waveforms are acquired for each PLL frequency swept, the amplitude of the fundamental peaks in each spectrum is measured. Plotting these amplitudes versus the PLL frequency reveals the highest peak, indicating

the resonance frequency. This is shown in Figure 4. To accelerate the measurement process, an initial sweep is conducted with an 8 MHz or 4 MHz step to broadly identify the main resonance frequency. Then, a finer sweep is performed around that frequency with a 1 MHz step to pinpoint the main resonance frequency more precisely.

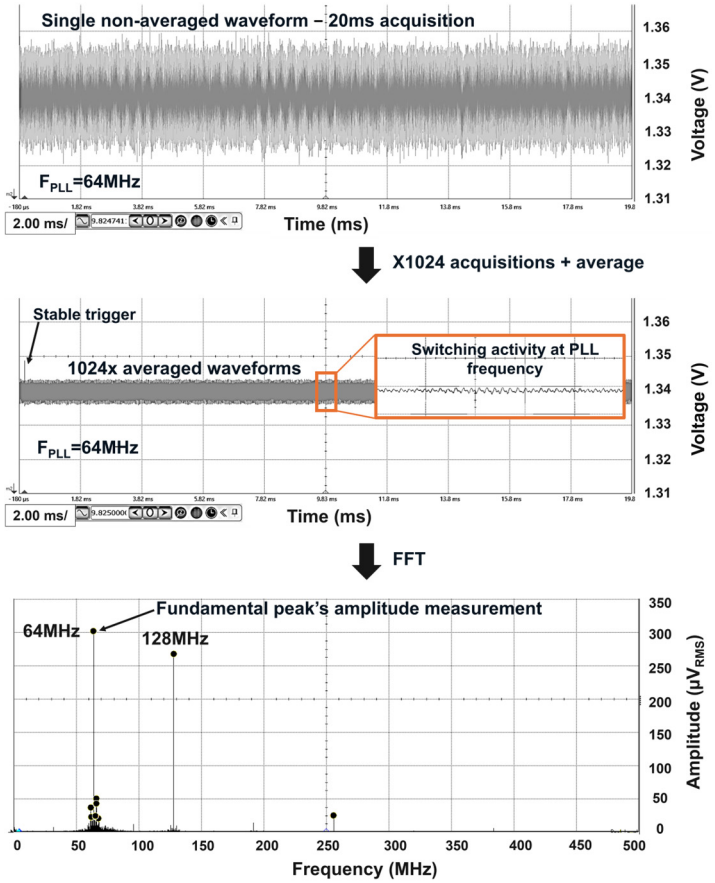

Figure 3. Main resonance frequency measurement process for an example of F_{PLL} = 64 MHz.

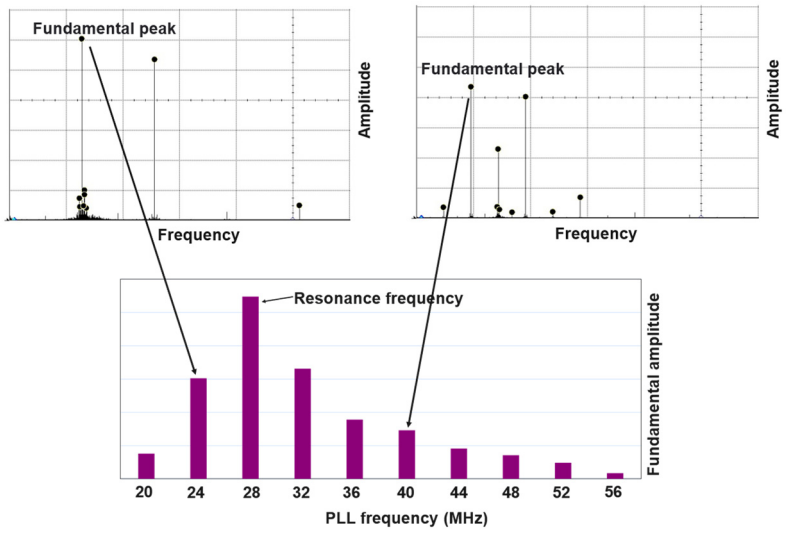

Figure 4. Resonance frequency identification process: comparison of the fundamental peak amplitudes from the spectrum according to the PLL frequency.

The obtained results can be confirmed by identifying the undamped oscillating noise shape when operating around the estimated resonance, if the clock-edge current is suffi-

ciently large. Finally, the main resonance frequency can be rapidly evaluated by considering the noise spectrum at a low PLL frequency. Clock harmonics close to the resonance are amplified by the PDN, which directly showcases the resonance frequency in the spectrum. However, the accuracy of this method depends on the PLL frequency value and noise amplitude. If the noise level is too low when operating at a low frequency, as might be the case for low-power MCUs, this identification method may not be operational.

3.2. Measurement Setup

In order to satisfy the cost constraint and favor ease of implementation and replicability, the measurement is performed using common instrumentation, such as a standard 10:1 passive probe with an oscilloscope. To reduce the parasitic loop inductance brought by the probe, a ground spring adaptor is used for the ground reference path. The noise is probed directly on the PCB, through the pad of a dedicated analog input/output (IO) internally connected to the power grid, if available, or through regular power supply test pads or vias. Each noise waveform is acquired for 20 ms, and 1024 waveforms are averaged for each frequency point swept in the first case study. To improve the time efficiency of the method, this number is adjusted to 256 waveforms for the second case study. The complete measurement setup is illustrated in Figure 5.

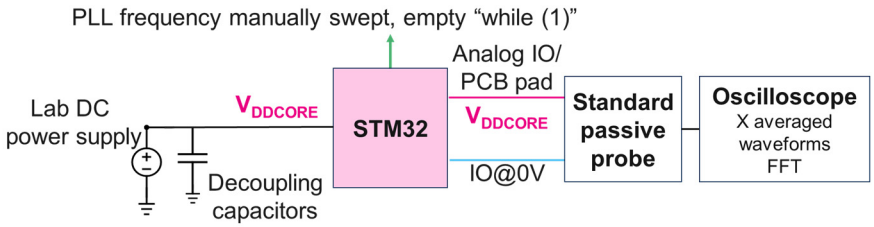

Figure 5. Proposed resonance frequency measurement setup.

3.3. Setup Validation

Since the proposed method uses common instrumentation, the setup must be validated to ensure it can properly capture the MCU activity reflected in the noise. This is achieved by measuring the dynamic current of a high-performance MPU using a CT6 probe. This current transformer translates the current to a voltage with a 5 mV/mA sensitivity and has a 2 GHz bandwidth. To accurately measure the AC current, all decoupling capacitors are removed except for a 22 µF bulk decoupling capacitor, retained to ensure supply voltage stability. The measured current waveform is then compared to the averaged noise acquired using this method’s setup for the same chip operation. Figure 6 shows the current measurement setup, and the results for a PLL frequency of 8 MHz and 64 MHz are displayed in Figures 7 and 8, respectively.

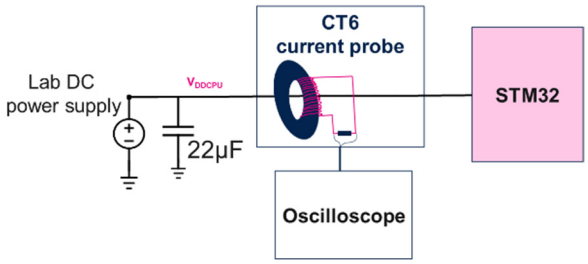

Figure 6. CPU current measurement setup for the measurement method validation.

Figures 7 and 8 show that the current pattern is similar to the measured average noise pattern for the two PLL frequencies evaluated. The switching activity is also identifiable in both measurements. This demonstrates the efficiency of the proposed measurement setup in capturing the MCU’s activity.

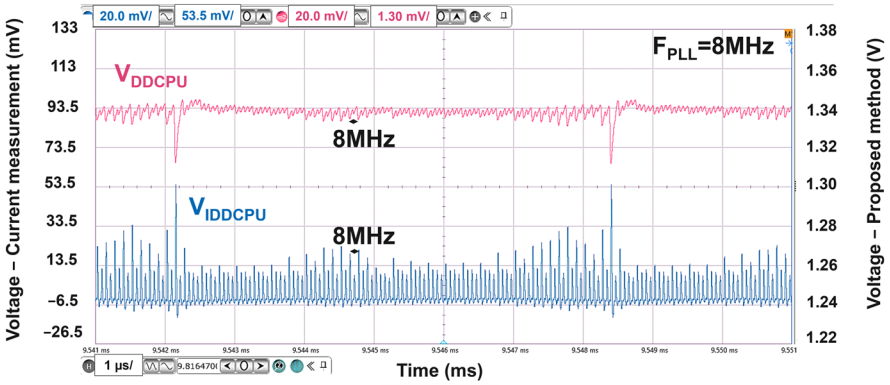

Figure 7. CPU current (blue) measured with a CT-6 probe and CPU supply voltage (red) measured with the proposed method's setup for F_{PLL} = 8 MHz.

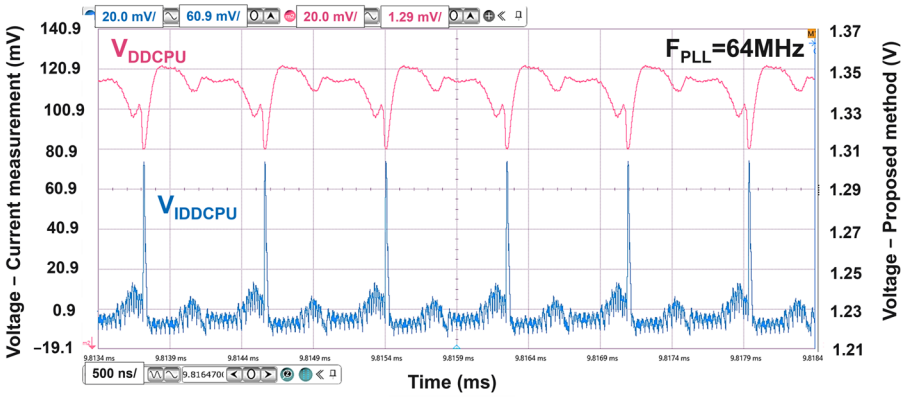

Figure 8. CPU current (blue) measured with a CT-6 probe and CPU supply voltage (red) measured with the proposed method's setup for F_{PLL} = 64 MHz.

4. Validation on a High-Power MPU

Now that the measurement setup is validated, the ability of the proposed technique to efficiently characterize the main resonance frequency must be confirmed. This is evaluated in two steps. First, the results of this work's method when applied to a high-power STM32 are compared to a former method, previously validated [21]. This comparison is performed for two PDNs within the same system, obtained by changing the decoupling configuration on the PCB. The dedicated CPU power domain is evaluated. The measurements are performed on a board originally designed to assess the electromagnetic compatibility of the STM32, which is packaged in a wire-bonded BGA. The second step consists of correlating the experimental results with the simulation results for four decoupling configurations. This will also help to ensure the proposed method enables the detection of a change in PDN parasitics through the measured resonance frequency. The four decoupling configurations evaluated are summarized in Table 1.

Table 1. Four decoupling configurations tested for the first case study.

Configuration 1	Configuration 2	Configuration 3	Configuration 4
7 × 1 µF (all decaps)	3 × 7 µF (3 decaps)	1 × 1 µF (1 decap)	No decap

4.1. Comparison with a Previously Validated Method [21]

The former method relies on an external signal generator, capacitively coupled to the power supply, to stress the PDN. The frequency of the sine wave varies across the common resonance frequency range, and the peak-to-peak noise is measured using an active probe.

The measurement setup is shown in Figure 9. The measured noise over the sweep is plotted versus the excitation signal frequency to reveal the resonance.

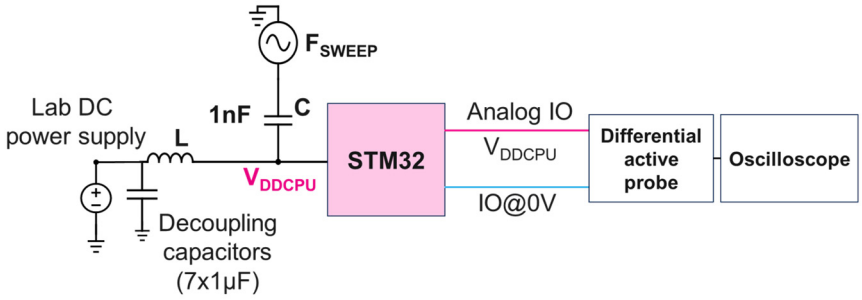

Figure 9. Setup of the former resonance frequency measurement method.

This measurement was performed for Configurations 1 and 2, and the probing location was the same as the one used when applying this work's method. The results are shown in Figure 10. The first peak of each measurement corresponds to the main resonance frequency, while the second peak area illustrates the PCB planes' resonance. The observation of the PCB resonance is related to the previously validated method when measuring the noise far from the chip on the PCB, and not on-chip or on package leads. The several small local peaks observed in those high-frequency areas can be attributed to a trigger level that is unadjusted for the frequencies. However, since these peaks are not the focus of the measurement, they do not compromise the validation of the proposed measurement method.

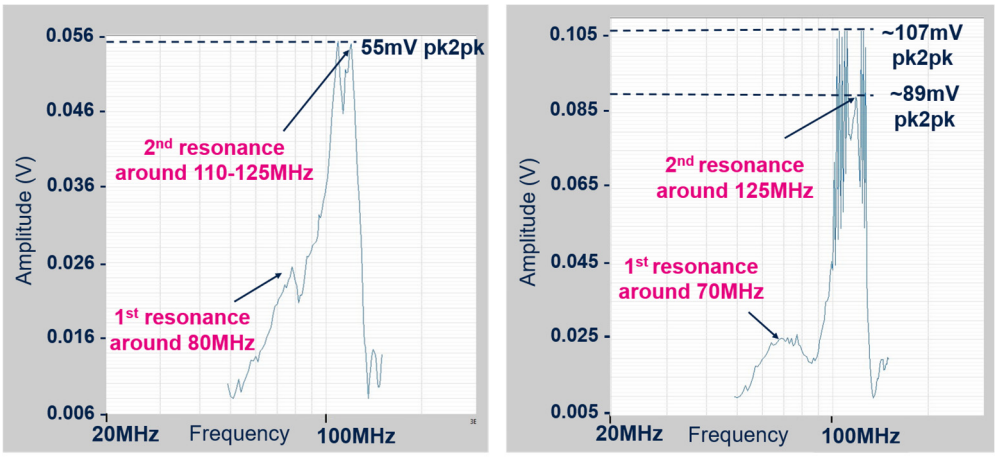

Figure 10. Measured CPU supply voltage using the former method [21] for Configuration 1 (**left**) and Configuration 2 (**right**).

The resonance frequency measured is compared to that acquired with the novel method, with the results summarized in Table 2.

Table 2. Estimated resonance frequency using the method in [21] and this work's method for Configurations 1 and 2.

Method Used	Main resonance in Configuration 1	Main Resonance in Configuration 2
Former method	~75–80 MHz	~70 MHz
This work	~80 MHz	~64 MHz

The two measurement techniques yield similar results for both decoupling configurations, confirming the proposed method's ability to evaluate the main resonance frequency

across various PDNs. Additionally, it offers the benefit of eliminating the PCB planes' resonance predominance in the measurement.

4.2. Modeling and Simulation

To finalize the evaluation of the measurement method, results are compared with the simulated main resonance frequency of different PDNs, obtained with the four decoupling configurations introduced earlier [1].

The VRM is modeled, as a first order, as its output bulk decoupling capacitor. This representation is not suited for comprehensive PI analysis, which includes low-frequency behavior and time-domain simulations. For such evaluations, a complete small-signal model is necessary. However, the focus of this work is on correlating the high-frequency main resonance, where the VRM's impact is less significant. Therefore, the selected simplified model may be adequate to achieve a good correlation at high frequencies [22] with the benefit of reducing the overall model and simulation complexity.

The PDN interconnect is modeled using an S-parameter, extracted after merging the final PCB and package layouts in an EDA tool. Decoupling capacitors are not integrated into the interconnect model. Instead, their S-parameters, provided by the manufacturer, are connected externally to it.

The die is represented by an RC lumped model, with values extracted from a chip power model (CPM). In this case, the CPM represents a Dhrystone activity in a fast–fast (FF) process corner with a maximum internal voltage and temperature. These were the only conditions available for simulating the die activity. Since this process voltage temperature (PVT) corner differs from the typical environment in which the measurement is performed, discrepancies between the measurement and simulation results may arise. The die's extracted RC values are R_{DIE} = 35 mΩ C_{DIE} = 10 nF.

The parasitic values from the measurement setup, as specified in the manufacturers' datasheets, are summarized in Table 3.

Table 3. Measurement setup parasitic elements for the model.

Setup Element	Parasitic Impedance	Parasitic Capacitance	Parasitic Inductance
Oscilloscope	1 MΩ	14 pF	-
Passive probe	9 MΩ	9.5 pF	20 nH
Supply wires	62 mΩ	-	46 nH

The simulated impedance profile for Configuration 1 is depicted in Figure 11, with the main resonance frequency observed at 48 MHz. The corresponding experimental results, obtained using the measurement method with an 8 MHz step, are presented in Figure 12. Here, a distinct resonance shape is observed, with the resonance frequency estimated to be around 72 MHz. The same conclusion can be drawn from observing the 8 MHz spectrum, depicted in Figure 13, which shows amplified harmonics around 80 MHz. This spectrum appears to be a superimposition of two spectra: one with even harmonics and the other with odd harmonics of the PLL frequency. It should be noted that the even harmonics are predominant.

Additionally, it is interesting to mention that the undamped oscillatory noise pattern, typical of a resonance, is more pronounced at a PLL frequency of 36 MHz rather than 72 MHz. This is illustrated in Figure 14. In this system, operating at half the resonance frequency proves to be more harmful than at the actual resonance frequency. This can be attributed to the switching activity occurring on both the rising and falling edge of the clock, resulting in a 72 MHz switching pattern when the operating frequency is 36 MHz.

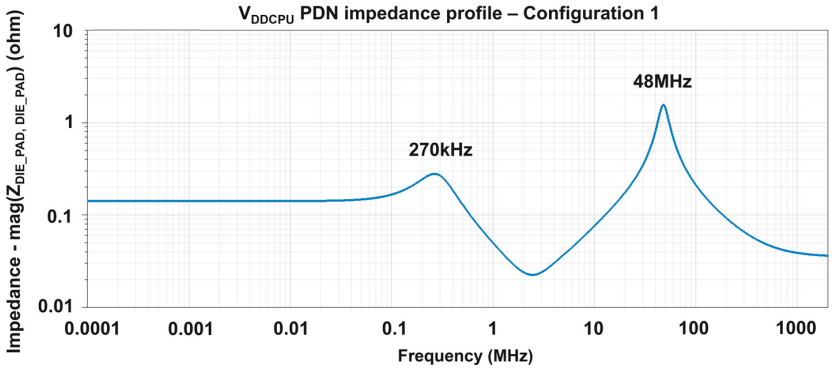

Figure 11. Simulated V_{DDCPU} PDN impedance profile for Configuration 1.

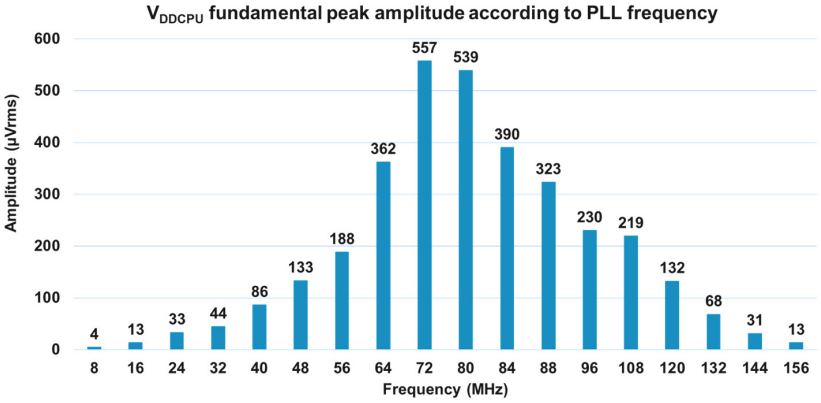

Figure 12. V_{DDCPU} fundamental peak amplitude over PLL frequency for Configuration 1.

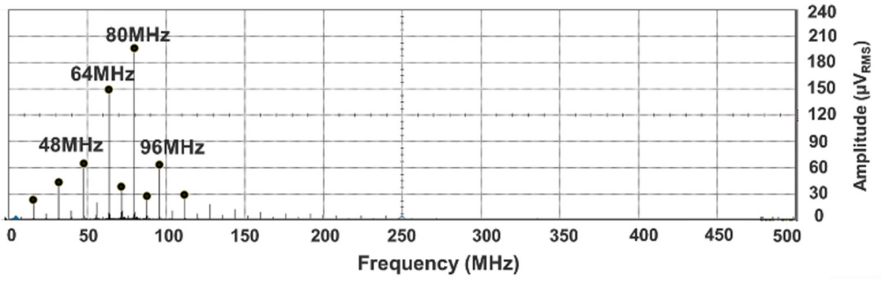

Figure 13. CPU averaged supply noise spectrum for F_{PLL} = 8 MHz.

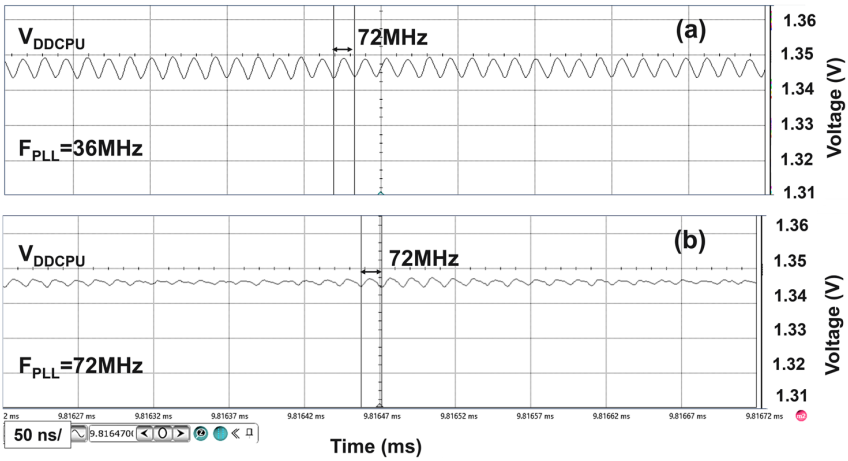

Figure 14. CPU averaged supply voltage for (**a**) F_{PLL} = 36 MHz and (**b**) F_{PLL} = 72 MHz.

The combination of all these observations strongly suggests a resonance frequency in the range of 72 MHz to 80 MHz. A more detailed analysis, using a finer step, identified the resonance frequency at 75 MHz. This significantly deviates from the simulated results, indicating a potential issue with either the measurement process or modeling approach. This difference likely stems from inaccuracies in the die capacitance model, as it was extracted for different conditions than those used during the measurement. The model extraction conditions were constrained by the limited availability of VCD files and cell library models during the design phase. Furthermore, the measurement method was previously validated using an established method, thus confirming its efficacy.

4.3. Model Refinement

The die capacitance model is refined by first determining the interconnect inductance that contributes to the main resonance frequency, and then calculating the die capacitance value that results in the measured resonance frequency. The interconnect inductance is deduced from the following equation, using the initially simulated resonance frequency:

$$L_{INTERCONNECT} = \frac{1}{C_{DIE} \times (2\pi f_{res})^2} \quad (2)$$

With an initial simulated resonance frequency of 48 MHz, we have $L_{INTERCONNECT}$ = 1.1 nH. The die capacitance required to obtain a 75 MHz resonance frequency, as measured, is then C_{DIE} = 4.1 nF. This value is rounded to 4 nF in the updated model, as the precise measurement is valid within $\pm$ 1 MHz. This adjustment resulted in a 76 MHz main resonance frequency in the simulation. The die resistance was not updated since this study primarily focuses on the resonance frequency, to which the die resistance does not contribute, and which is more challenging to estimate.

To validate the refined die model, the measurement is applied to the three additional decoupling configurations listed in Table 1. The measurement for Configuration 1 was detailed earlier. Configurations 2 to 4, achieved by removing decoupling capacitors on the PCB, are expected to exhibit a lower resonance frequency due to increased inductance. By comparing the experimental results of these four distinct PDNs with the new simulation results, the validity of the new model can be evaluated.

The impedance profile of Configuration 2, depicted in Figure 15, shows an expected resonance frequency of 66 MHz, which expectedly decreased compared to the first configuration.

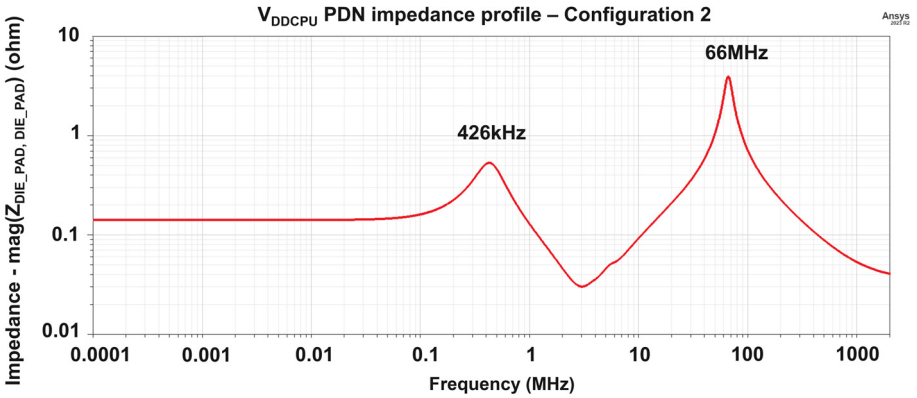

Figure 15. V_{DDCPU} PDN impedance profile with the updated die capacitance model for Configuration 2.

The corresponding measurement results are depicted in Figure 16. It reveals a resonance frequency around 64 MHz. A finer step narrowed this down to 66 MHz, indicating a strong correlation between the experimental and simulated results. This resonance frequency is also observable in the noise spectrum for a PLL frequency of 8 MHz, as depicted in Figure 17. Indeed, the 64 MHz peak, being the closest harmonic to 66 MHz, is signifi-

cantly amplified compared to the others. Additionally, these results confirm the validity of the refined die capacitance model of 4 nF.

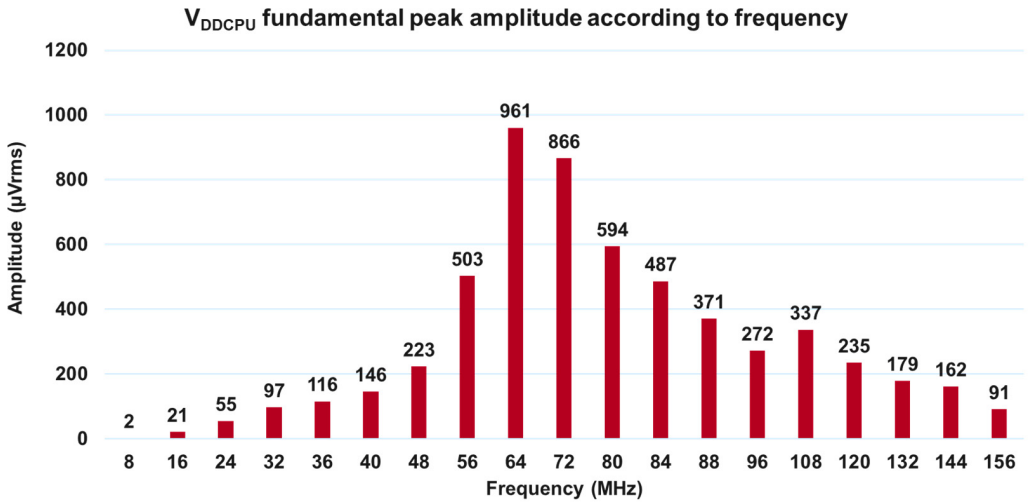

Figure 16. V_{DDCPU} fundamental peak amplitude over PLL frequency for Configuration 2.

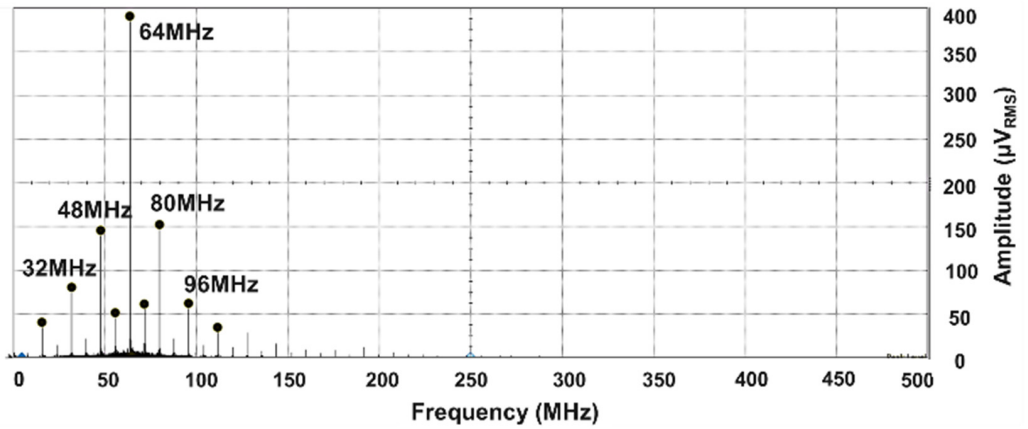

Figure 17. CPU averaged voltage spectrum for F_{PLL} = 8 MHz and Configuration 2.

Figures 18 and 19 present the measurements and simulations for Configuration 3 and 4, respectively. Once again, a good correlation is observed for these two configurations. Table 4 summarizes the measured and simulated resonance frequencies for the four PDNs, along with the relative errors. These results confirm the validity of the updated die capacitance model.

The resonance frequency of the last configuration is significantly lower than the others, explained by the removal of all decoupling capacitors, which considerably increases the inductance involved in the main resonance.

The proposed measurement method has been successfully validated for a high-power microprocessor system across four different PDN configurations, enabling the refinement of the die model. To test the method's applicability to a broader range of STM32s, its efficiency against a lower-consumption MCU is evaluated.

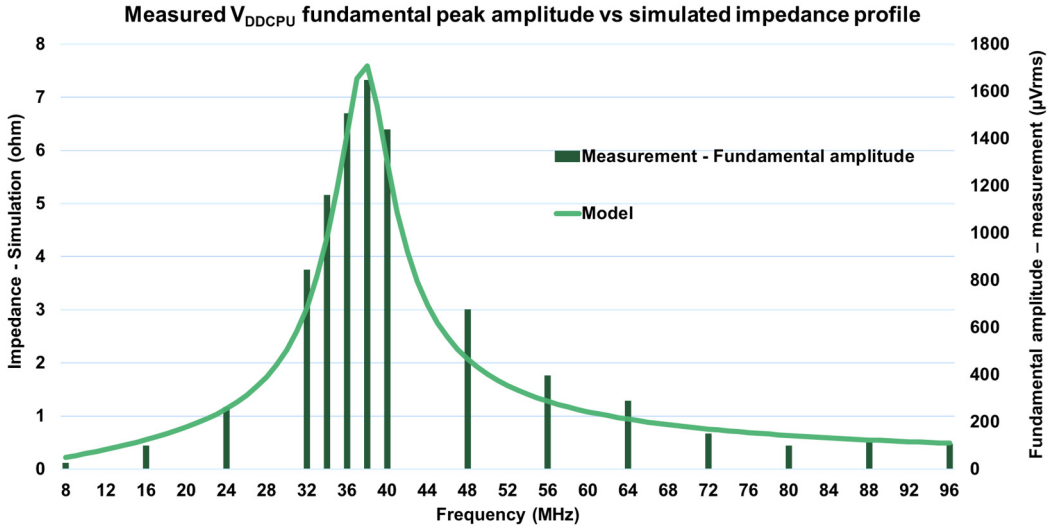

Figure 18. Measured (dark green) V_{DDCPU} fundamental peak amplitude vs. simulated (light green) impedance profile for Configuration 3.

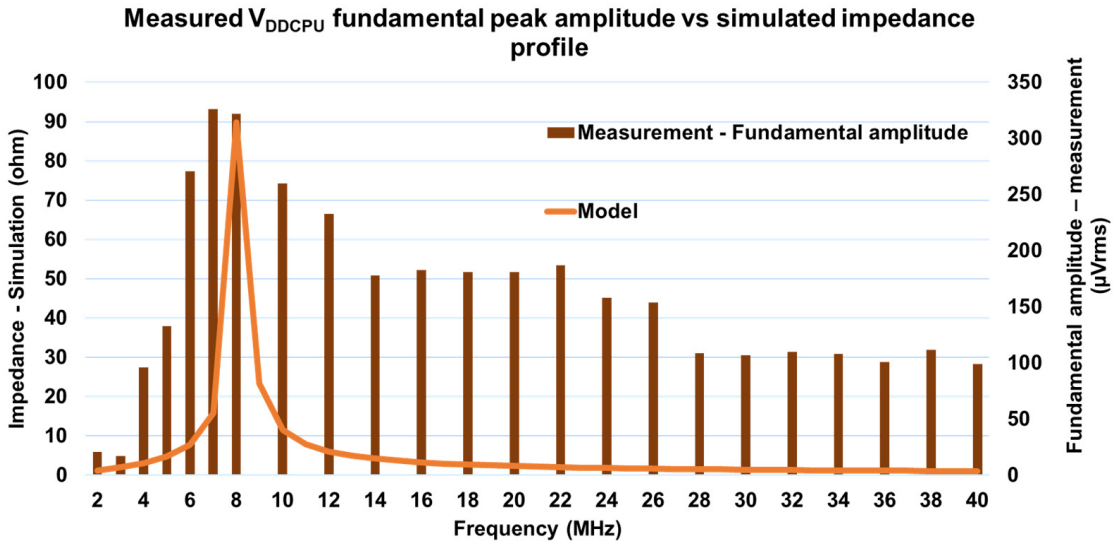

Figure 19. Measured (brown) V_{DDCPU} fundamental peak amplitude vs. simulated (orange) impedance profile for Configuration 4.

Table 4. Measured and simulated resonance frequency and relative error for each decoupling configuration.

Configuration	Measurement	Simulation	Relative Error
Configuration 1	75 MHz	76 MHz	1.3%
Configuration 2	66 MHz	66 MHz	0%
Configuration 3	38 MHz	38 MHz	0%
Configuration 4	7 MHz–8 MHz (7.5 MHz)	8 MHz	6.3%

5. Mid-Range-Power MCU Case Study

The second case study examines a mid-range-power microcontroller with a common power supply for the core and CPU circuits, supplied by an internal LDO. As in the previous case, the STM32 is housed in a wire-bonded BGA package, and measurements are conducted on the same type of PCB.

To assess the proposed method's efficiency for this system, two decoupling configurations, summarized in Table 5, are evaluated.

Table 5. Decoupling configurations tested for the second case study.

Configuration 1	Configuration 2
2 × 1 µF	1 × 1 µF

5.1. Modeling and Simulation

The modeling strategy is similar to the first case study. The die model was extracted from a CPM representing a Dhrystone operation at an FF process corner, with a maximum temperature and voltage. Under these conditions, which differ again from the measurement context, the die capacitance is 25 nF, and the die resistance is 84 mΩ. The impedance profile for Configuration 1, depicted in Figure 20, shows the main resonance evaluated at 9 MHz.

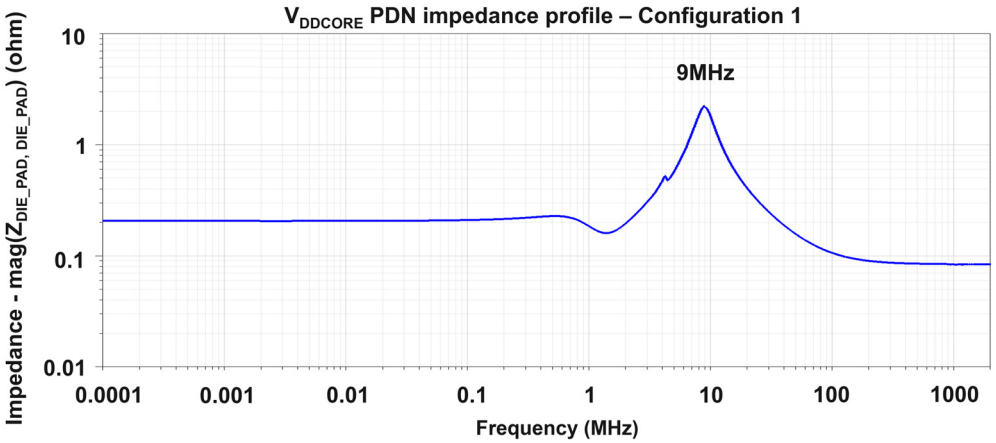

Figure 20. Simulated V_{DDCORE} PDN impedance profile for Configuration 1.

5.2. Experimental Results

The measurement method is applied to the STM32 system in Configuration 1. The trigger used for the average is a 10 kHz PWM signal, internally generated by a timer and output on a general-purpose IO (GPIO). Figure 21 shows the fundamental peak amplitudes. The resonance frequency is evaluated at 12 MHz, which significantly differs from the simulated value. Consequently, the die capacitance model will be adjusted using the method introduced in the previous case study. The second configuration will help validate the updated model.

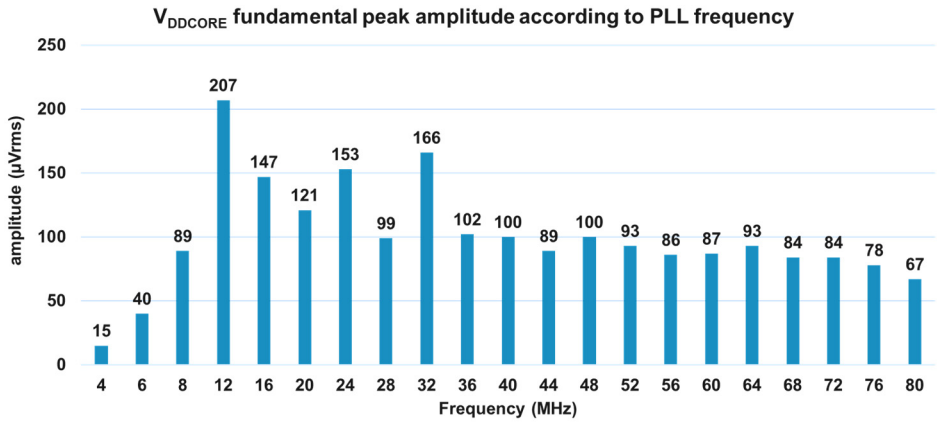

Figure 21. V_{DDCORE} fundamental peak amplitude over PLL frequency for Configuration 1.

Additionally, two other fundamental peaks at 24 MHz and 32 MHz are locally predominant. To verify if these are not local resonance frequencies, the noise spectrum for F_{PLL}=2 MHz is analyzed. As depicted in Figure 22, a clear resonance pattern appears from the 2 MHz harmonics, with the highest peak at 12 MHz. However, the peaks at 24 MHz and 32 MHz are not observed as local maxima, suggesting that the peaks observed in Figure 21 are not related to PDN parasitics. They may originate from the measurement setup or be harmonics of the resonance frequency. Further measurements with the second decoupling configuration will provide additional data to investigate their origin.

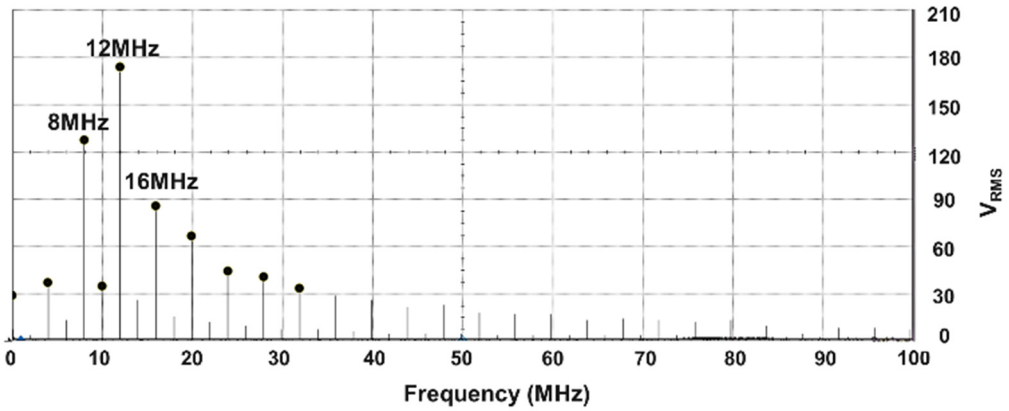

Figure 22. V_{DDCORE} supply noise spectrum for F_{PLL} = 2 MHz and Configuration 1.

5.3. Model Correction

Applying the same die capacitance refinement process as introduced earlier, we obtain $L_{INTERCONNECT}$ = 12.5 nH and C_{DIE} = 14 nF to simulate a 12 MHz resonance frequency. To check the validity of this model, the impedance profile for Configuration 2 is simulated, and the resonance frequency is measured. Both results are presented in Figure 23.

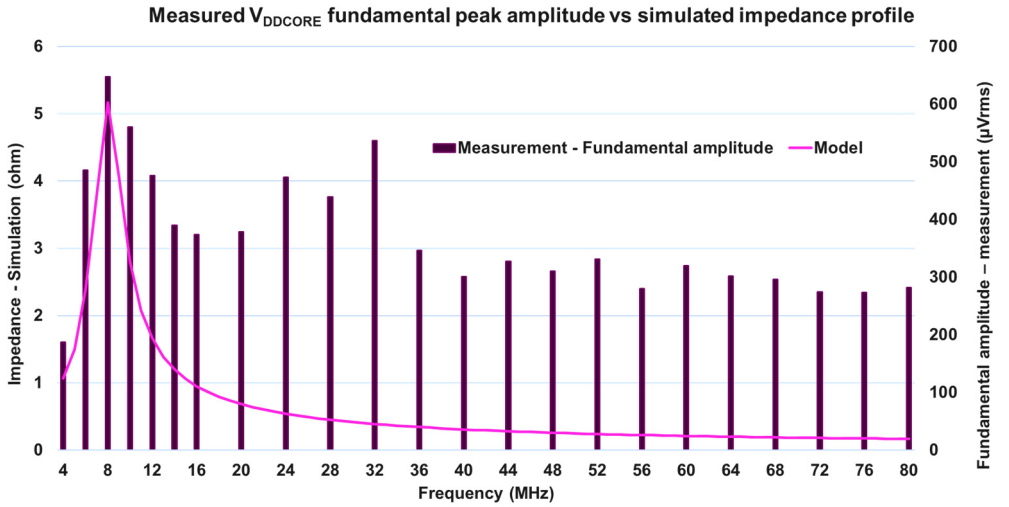

Figure 23. Measured (purple) V_{DDCORE} fundamental peak amplitude vs. simulated (pink) impedance profile for Configuration 2.

Both the experimental and simulated results indicate a resonance frequency of 8 MHz, thus validating the model refinement. The same phenomenon regarding the 24 MHz and 32 MHz peaks, as observed in Configuration 1, is noted. These peaks correspond to the third and fourth harmonics of the resonance frequency. However, given the consistent pattern between Configurations 1 and 2 and the absence of a local maximum at the 2nd harmonic of 16 MHz, these peaks are likely attributed to a different phenomenon. Further investigation into this matter is underway. Despite these local peaks, the main resonance

frequency was still identifiable. The main peak decreased as expected when the inductance was increased by removing the decoupling capacitors, transitioning from Configuration 1 to Configuration 2. Additionally, measurements using a completely different setup, consisting of a spectrum analyzer and dedicated probe in a different lab, confirmed the same main resonance frequency as previously evaluated for the two decoupling configurations. It should also be noted that this local predominance disappears when analyzing the noise spectrum for a 2 MHz operation, while the 8 MHz resonance is clearly identified. This is shown in Figure 24.

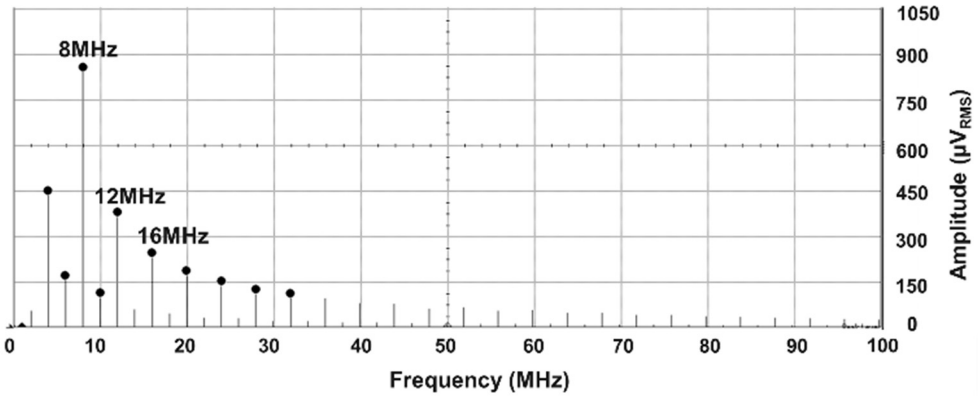

Figure 24. V_{DDCORE} supply noise spectrum for F_{PLL} = 2 MHz and Configuration 2.

Despite these observations, an excellent correlation between the measurement and simulations using the updated model is observed, as summarized in Table 6.

Table 6. Measured and simulated resonance frequency and relative error for each decoupling configuration.

Configuration	Measurement	Simulation	Relative Error
Configuration 1	12 MHz	12 MHz	0%
Configuration 2	8 MHz	8 MHz	0%

These results outline the efficiency of the proposed method when applied to a mid-range-power MCU.

6. Conclusions

The characterization of the PDN through simulation and measurement is a critical aspect of the design phase of an MCU system. Evaluating the die-package resonance is essential, as it may cause significant noise in the power supply. This article proposes a straightforward method for measuring that resonance frequency. While the impedance is not directly evaluated, the method is easy to implement, cost-efficient, and provides valuable insight into PDN parasitics. By identifying the main resonance frequency, operations can be adjusted to avoid triggering it if necessary. The measurement method was successfully applied to two types of STM32 for different PDN configurations. In each case study, the measurement method allowed for the refinement of the die capacitance model. The final results showed a good correlation for all evaluated PDNs, offering a uniform modeling method effective for both high-power and mid-range-power STM32 devices. However, the method's efficiency for low-power MCUs has yet to be evaluated. Moreover, the analysis of the high-power MPU highlights the potential risk of operating at half the resonance frequency rather than at the resonance frequency itself in some cases. Future steps include investigating the emergence of local maximum peaks in certain measurements to facilitate the identification of the main resonance frequency and exploring the on-chip integration of this measurement method while maintaining cost efficiency. Embedded on-chip, this

measurement method would allow customers to characterize an essential metric of the PDN in their final MCU application and make necessary design or operational adjustments.

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