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A 1.87 µW Capacitively Coupled Chopper Instrumentation Amplifier with a 0.36 mV Output Ripple and a 1.8 GΩ Input Impedance for Biomedical Recording †

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Abstract: Chopper and capacitively coupled techniques are employed in instrumentation amplifiers to create capacitively coupled chopper instrumentation amplifiers (CCIAs) that obtain a high noise power efficiency. However, the CCIA has some disadvantages due to the chopper technique, namely chopper ripple and a low input impedance. The amplifier can easily saturate due to the chopper ripple of the CCIA, especially in extremely low noise problems. Therefore, ripple attenuation is required when designing CCIAs. To record biomedical information, a CCIA with a low power consumption and a low noise, low output ripple, and high input impedance (Z_{in}) is presented in this paper. By introducing a ripple attenuation loop (RAL) including the chopping offset amplifier and a low pass filter, the chopping ripple can be reduced to 0.36 mV. To increase the Z_{in} of the CCIA up to 1.8 GΩ, an impedance boost loop (IBL) is added. By using 180 nm CMOS technology, the 0.123 mm^2 CCIA consumes 1.87 µW at a supply voltage of 1 V. According to the simulation results using Cadance, the proposed CCIA architecture achieves a noise floor of 136 nV/$\sqrt{Hz}$, an input-referred noise (IRN) of 2.16 μV_{rms}, a closed-loop gain of 40 dB, a power supply rejection ratio (PSRR) of 108.6 dB, and a common-mode rejection ratio (CMRR) of 118.7 dB. The proposed CCIA is a helpful method for monitoring neural potentials.

Keywords: low power; chopper amplifier; ripple attenuation; input impedance

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1. Introduction

Wireless biomedical sensors (WBSs) are increasingly used to track our daily activities in order to detect cardiovascular diseases at an early stage [1–4]. Monitoring human biopotential requires the use of low-power sensors deployed in wearable or implantable systems. Researchers are currently developing brain–computer interfaces for numerous applications such as long-term monitoring, sports, rehabilitation, mobile monitoring, and improving the quality of life of patients [5,6]. WBSs typically use an instrumentation amplifier (IA) with low power consumption and low noise to connect with many types of biological sensors. The electrocardiograms (ECGs) of the heart and the electroencephalograms (EEGs) of the brain are examples of these biopotential signals. Neuroscience research and therapy can benefit from the use of biomarkers such as action potentials (APs) and local field potentials (LFPs) [7–9]. Biopotential signals often have an extremely small amplitude. For example, the amplitude range of an EEG is from 10 to 100 µV and that of an ECG is about 1 mV. The frequency range of the biopotential signals is 0.5–150 Hz [7,8]. The amplitude of the AP and LFP signals is about 100 µV to 1 mV, with a frequency range of 0.2 to 10 kHz for APs, and 1 to 200 Hz for LFPs [9]. Consequently, before signal processing is applied, these

neural signals need to be amplified. A wearable biomedical sensor, constructed as shown in Figure 1, provides these neurological signals.

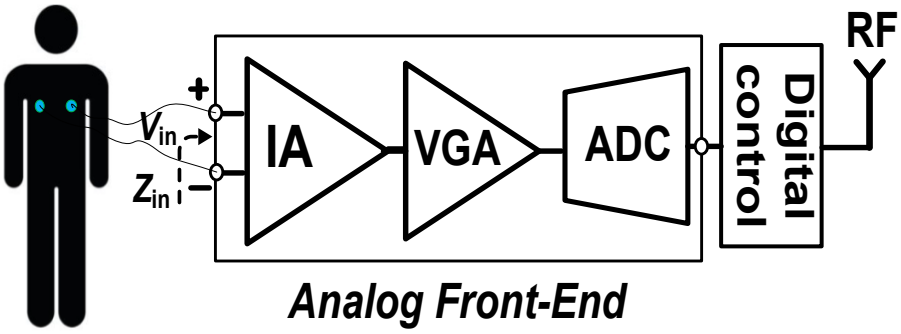


Figure 1. System architecture of a typical wireless sensor biomedical system.

The first stage measures the amplitude of the small bio signal with a dry or wet electrode. An analog front-end, consisting of an IA at the first stage, a variable gain amplifier (VGA) at the middle stage, and an analog-to-digital converter (ADC) at the last stage, processes the neural signal in the second stage before it is transmitted by RF. The preamplifier of the analog front-end must obtain a high input impedance (Z_{in}) to reduce the DC input current that could cause tissue damage [8]. The IA must likewise demonstrate a low power, low noise, high-power supply rejection ratio (PSRR), and common-mode rejection ratio (CMRR) to eliminate noise from the power line and environmental factor, which may be important in some cases.

The chopping technique is frequently used in IA [10–17] to create an IA with a high PSRR, CMRR, and noise efficiency. The input capacitance and the switches in the chopper block generate the switched capacitance resistor, which is inversely proportional to the chopper frequency. This leads to a limitation of the Z_{in} of the amplifier if there are no impedance boosting techniques [18]. The ripple appears as a triangular wave affecting the quality of the signal of interest caused by a modulated intrinsic offset [19–21]. Furthermore, for long-term battery life suitable for WBS applications, the power consumption of the IC must be as small as possible, and the noise must also be low so as not to affect the signal quality at the output of the IC. Although a number of biomedical amplifiers with low power consumption have been published, it has not yet been possible to improve the output ripple or Z_{in}. For example, in 2020, the chopper amplifier in [22] consumed 3.24 µW at a 1.8 voltage supply, the Z_{in} just reached 440 MΩ, while the ripple suppression technique used an AC coupling capacitor, which caused this design to be affected by the noise folding [19]. In 2021, the current-reuse instrumentation amplifier [23] dissipated 5.94 µW at a voltage supply of 1.8 V to achieve a Z_{in} of 2.6 GΩ without any ripple suppression approaches. In 2024, although the amplifier [24] consumed only 2.47 µW from a 1.5 V supply, the output ripple and Z_{in} were not improved.

This paper presents a CCIA for biomedical information recording that is characterized by low noise, high input impedance, low output ripple, and low power consumption. At 1 V, the 0.123 mm^2 CCIA, which was simulated using a 180 nm CMOS process, consumes 1.87 µW. According to simulation results, it is shown that the output ripple being reduced to 0.36 mV is achieved with an RAL being switched on, and the Z_{in} of the CCIA increases up to 1.8 GΩ when the impedance boost loop (IBL) is active. When both the RAL and IBL are activated, the proposed CCIA obtains a closed-loop gain of 40 dB, an input referred noise (IRN) of 1.81 μV_{rms}, a thermal noise of 136 nV/$\sqrt{Hz}$, a common mode rejection ratio (CMRR) of 118.7 dB, and a power supply rejection ratio (PSRR) of 108.6 dB. Achieving a noise efficiency factor (NEF) of 6.8 and 7.5 with both RAL and IBL turned off and on, respectively, demonstrates that the CCIA records biomedical information successfully.

2. Design

The proposed CCIA for biomedical monitoring applications with a low output ripple and a high Z_{in}, as shown in Figure 2, consists of the main channel and three auxiliary loops such as a negative feedback loop (FBL), a ripple attenuation loop (RAL), and an impedance boosting loop (IBL) in order to solve the main problems of biopotential amplifiers. The transconductance input stage (G_{m1}) of the main path is a dual-folded cascode amplifier (DFC) with a biased current of 1.2 µA. In order to attain a working stability and a high swing, the G_{m3} used a common source (CS) amplifier, combined with a Miller capacitor of 1.5 pF. A bias current of 1.8 µA is used for the channel and global common mode feedback (CMFB) from a V_{DD} of 1 V. The CCIA has a closed-loop gain of 40 dB, which is defined by the ratio of the input and negative feedback capacitors. In this design, the input capacitor $C_{in1,2}$ is set at 20 pF and the negative feedback capacitor $C_{fb1,2}$ is set at 0.2 pF. The PMOS pseudo-resistor $R_{b1,2}$ is used to bias DFC using the common mode voltage V_{CM} = 0.5 V. The capacitors ($C_{in1,2}$, $C_{fb1,2}$, $C_{m1,2}$, and $C_{LP1,2}$) are created using the MIM capacitor technique.

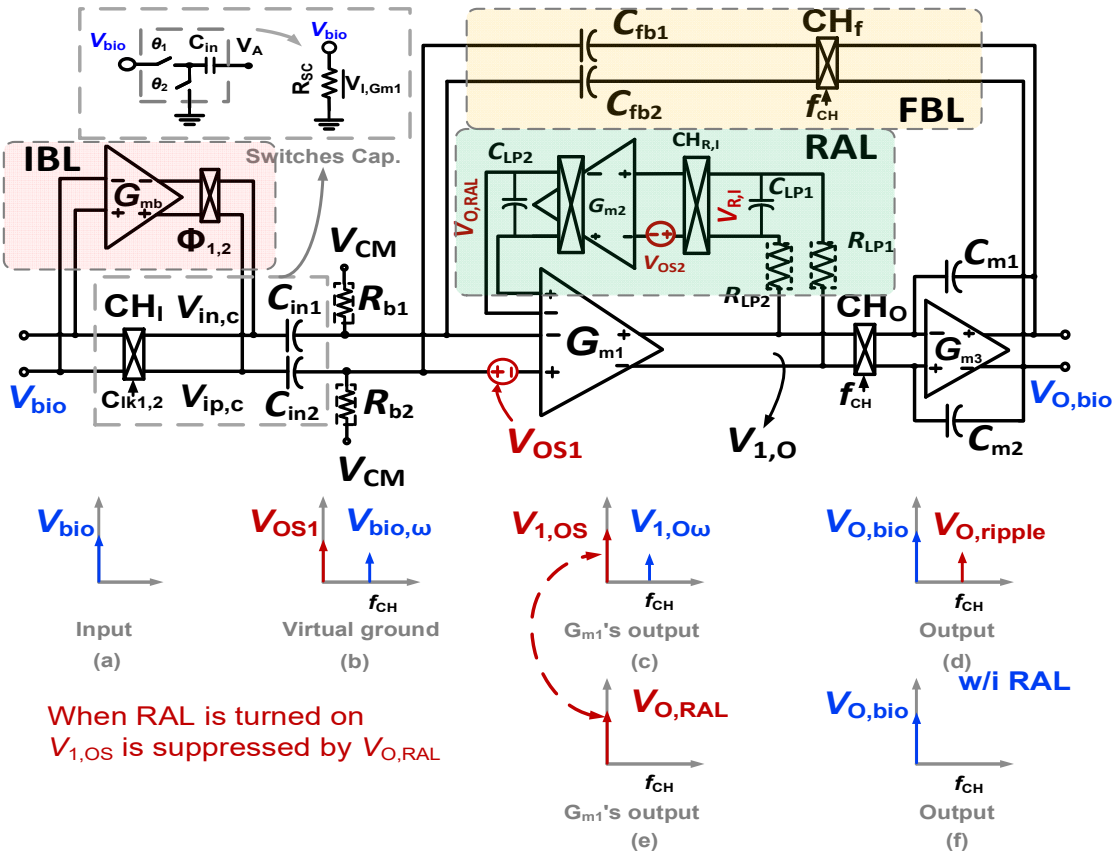


Figure 2. The schematic of the proposed CCIA with the spectrum of signal corresponding to each node.

As shown in Figure 2, the chopper CH_I is employed to modulate the bio signal input V_{bio} at low frequency (as shown in Figure 2a) up to a signal at f_{CH} = 10 kHz, before reducing it with a negative feedback loop at the virtual ground. When $V_{bio,\omega}$ is at virtual ground (as shown in Figure 2b), it can be written as $V_{bio,\omega} = V_{bio}/(1 + \beta A_V)$, where A_V is the open-loop gain voltage of the CCIA, and β is the factor of the negative feedback loop based on the ratio of C_{fb} to C_{in}. The chopper CH_O converts the $V_{bio,\omega}$ to the essential frequency band after G_{m1} has amplified it to produce $V_{1,O\omega}$. Finally, G_{m3} amplifies this signal to

generate a bio signal amplification $V_{O,bio}$ at the CCIA's output (as shown in Figure 2d). The transfer function of the proposed CCIA can be expressed as follows:

$$H(s) = -\left(g_{m1}C_{in1,2}\Big/(C_{in1,2}+C_{fb1,2})C_{m1,2}\right)\Big/\left(s+g_{m1}C_{fb1,2}\Big/(C_{in1,2}+C_{fb1,2})C_{m1,2}\right) \quad (1)$$

where g_{m1} is the transconductance of the first stage; and $C_{in1,2}$, $C_{fb1,2}$, and $C_{m1,2}$ are the input, negative, and Miller capacitors, respectively. Unfortunately, G_{m1} is attached to the offset voltage V_{OS1} resulting from the process variation (as shown in Figure 2b). After this is amplified by G_{m1} to create $V_{1,OS}$ at the output of DFC, the $V_{1,OS}$ is also chopped to the chopper frequency before being integrated by the Miller integrator. This results in a considerable ripple at the output (as shown in Figure 2d). The amplitude of the output ripple can be described as follows:

$$V_{O,Ripple} = \frac{V_{OS1}g_{m1}}{2f_{CH}C_{m1,2}} \quad (2)$$

where g_{m1} is the transconductance of the first stage; f_{CH} is the chopping frequency; and $C_{m1,2}$ are the phase margin compensation capacitors. For example, V_{OS1} = 10 mV, g_{m1} = 0.7 µS, f_{CH} = 10 kHz, $C_{m1,2}$ = 1.5 pF, and $V_{O,Ripple}$ = 233 mV.

The block diagram of an RAL is also shown in Figure 2. Instead of capturing the signal at the output, as in the usual approach, the RAL uses a low-pass filter (LPF) to obtain the signal at the output of the DFC ($V_{1,O} = V_{1,OS} + V_{1,O\omega}$) (as shown in Figure 2c) before the chopper output CH_O. This is because the $V_{1,OS}$ signal is continuously amplified, while the AC signal $V_{1,O\omega}$ is filtered out by the LPF in this case. To ensure that no AC signal is applied to G_{m1b}, which has the schematic shown in next section, the capacitor C_{LP2} is added to the output of the RAL, although the LPF has a small low-pass corner controlled by $R_{LP1,2}$ and C_{LP1}. After amplifying $V_{1,OS}$, the signal $V_{O,RAL}$ is connected to G_{m1b}, creating a negative feedback loop to compensate for $V_{1,OS}$ (as shown in Figure 2e). This means that the ripple caused by V_{OS1} is reduced at the output of the CCIA (as shown in Figure 2f). To increase the loop gain (L_G) of the RAL and achieve a high ripple attenuation factor (RAF), G_{m2} is implemented using a two-stage operational amplifier for low noise and low power consumption. We assume that V_{OS2}, another inherent offset caused by process variations, is similarly associated with G_{m2}. The modulated offset V_{OS2} also generates the ripple at the CCIA's output and has the same effects as V_{OS1}, so it needs to be reduced. The ripple at the output of the CCIA is mitigated by a DC loop gain's factor $L_G(0)$ of the feedback loop RAL. The equation to determine $L_G(s)$ in the technique proposed in this study is as follows:

$$L_G(s) \cong g_{m1b}R_{LP}A_{vGm2} = g_{m1b}R_{LP}\frac{A_{vGm2,DC}}{1+s/\omega_p} \quad (3)$$

$$L_G(0) \cong G_{m1}R_{LP}A_{vGm2,DC} \quad (4)$$

where G_{m1b} is the auxiliary transconductance of the first stage G_{m1}; and $A_{vGm2,DC}$ and f_p ($\omega_p = 2\pi f_p$) are the DC gain and cut-off frequency of the two-stage amplifier G_{m2}.

In the chopper biopotential amplifier, the input capacitor and the chopper are combined together, creating a switched capacitor resistor. At the completion of a cycle through the chopper clock f_{CH}, a charge of $Q = 2C_{in}V_{in}$ is delivered [7]. Therefore, Z_{in} can be determined as $Z_{in} = 1/(2C_{in}f_{CH})$. For example, Z_{in} is 2.5 MΩ for biomedical recording applications when the input capacitor C_{in} = 20 pF and f_{CH} = 10 kHz. An impedance boost loop (IBL) with a time diagram, as shown in Figure 3, is used to pre-charge Q to the C_{in}, as the Z_{in} must be improved by minimizing the charge Q from the input signal V_{in}. When the IBL is connected to C_{in}, the connection flowing from the input is interrupted and the V_{in} is copied by the buffer in IBL and is pre-charged to C_{in}. Assuming that the pre-charge current from the buffer is high enough, C_{in} will be fully charged from IBL; thus, when C_{in} is connected to the input after pre-charging, C_{in} does not require a charge from the

input signal V_{in}. This results in the fact that the Z_{in} can be set indefinitely. The Z_{in} can be represented following the analysis in [7], as follows:

$$Z_{in} = Z_0/(\alpha + \exp(-T/\tau)) \quad (5)$$

where Z_{in} is the input impedance, Z_0 is the input impedance without any boosting technique, α is the buffer gain error, T is the pre-charge time, and τ is the actual time constant.

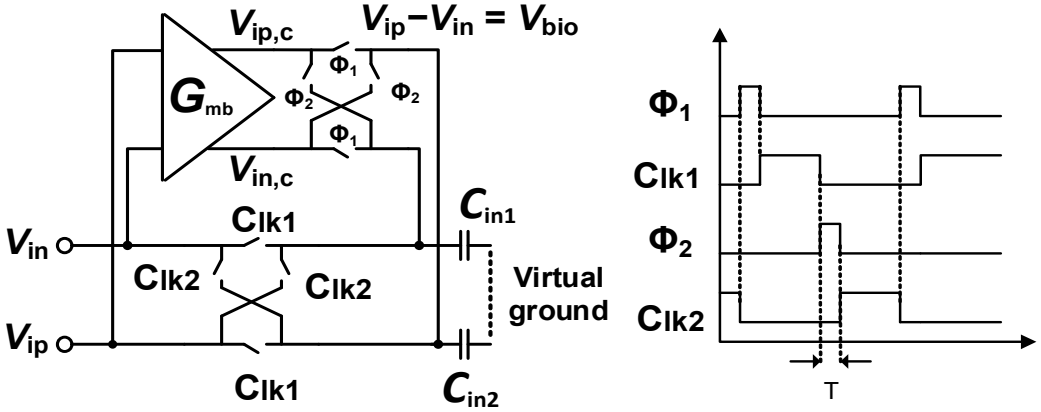
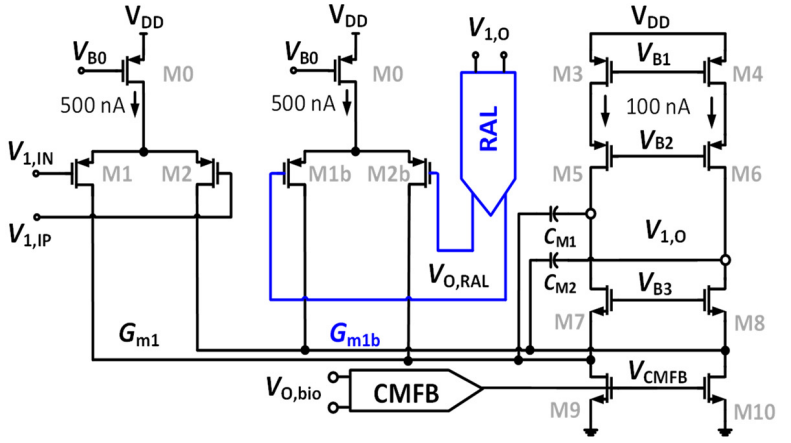


Figure 3. Schematics of the IBL and time diagram of the CCIA.

3. Circuit Implementation

Figure 4 shows the dual cascode amplifier (G_{m1}) combining with the RAL block. A feedback loop is set up comprising G_{m1b}, a two-stage chopper amplifier, and the RC-LPF in order to mitigate the output ripple. Figure 4 shows that the input stage consumes a power of 1.2 µW from a supply voltage of 1 V. The global common mode feedback circuit (CMFB) [25], which is used and consumed a biased current of 200 nA from 1 V, is employed to control the DC voltage at the output node of the CCIA. The gates of the transistors M_9 and M_{10} are adjusted using the CMFB circuit (V_{CMFB}) to control the output DC voltage followed to $V_{CM} = V_{DD}/2$. The power consumption of 1.4 µW of G_{m1} including CMFB is used.



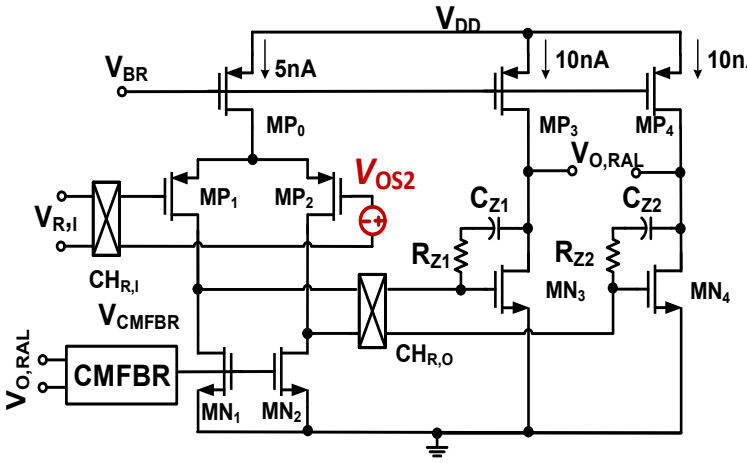
The table sizing of the CMOS transistors

M0	75µm/0.7µm
M1,2	30µm/0.7µm
M1b,2b	30µm/0.7µm
M3,4	15µm/0.7µm
M5,6	15µm/0.7µm
M7,8	6µm/0.7µm
M9,10	16µm/6µm
$C_{M1,2}$	0.3 pF

Figure 4. Schematic of the two-folded cascode opamp G_{m1} with table sizing of CMOS transistors.

Figure 5 shows the architecture of the chopper two-stage amplifier integrating with a common mode feedback circuit (CMFBR) [25] for G_{m2}. As already mentioned, the inherent offset V_{OS2} of G_{m2} has the same effect as V_{OS1}; the offset that is also upmodulated creates the ripple at the output of the CCIA. Consequently, it must be eliminated. In RAL, the chopper $CH_{R,I}$ is located at the output of the LPF, while the chopper $CH_{R,O}$ is put between the first and second stage of G_{m2}. This causes V_{OS2} to be modulated up to a high frequency

and then modulated down by the chopper CH_O, resulting in an offset voltage in the front of G_{m3}. Therefore, V_{OS2} is considered as an offset at the input of G_{m3}. Due to the high gain level of G_{m1} (about 80 dB), this offset is insignificant compared to the input. Therefore, its influence can be neglected. By using a 1 V supply, the first stage of G_{m2} consumes 5 nA, while the second stage of G_{m2} is biased to 20 nA for a better swing. The voltage V_{CMFBR} is generated by the CMFB circuit, which uses a bias current of 5 nA. Therefore, the total power of the RAL is only 30 nW.



The table sizing of the CMOS transistors

MP_0	30µm/0.7µm
$MP_{1,2}$	30µm/0.7µm
$MP_{3,4}$	60µm/0.7µm
$MN_{1,2}$	5µm/20µm
$MN_{3,4}$	0.7µm/0.7µm
$C_{Z1,2}$	3 pF
$R_{Z1,2}$	1.5 MΩ

Figure 5. Schematic of the chopper two-stage amplifier with table sizing of CMOS transistors.

The DC gain and the cut-off frequency of G_{m2} are decisive factors for determining the ripple attenuation factor and the bandwidth of the loop gain. The Monte Carlo simulation (MCS) method is used to study the fluctuation of these parameters across the chip and the mismatch of the device, including global variation and local mismatch. Figure 6a and Figure 6b show the value of the DC gain and cut-off frequency of G_{m2}, respectively. These distributions were derived from 300 samples of the MCS. The results show a mean value (MV) of the DC gain of G_{m2} of 90.9 dB, with a standard deviation (Std) of 0.167 dB. Furthermore, the MV of the cut-off frequency is 0.042 Hz with a Std of 0.0044 Hz.

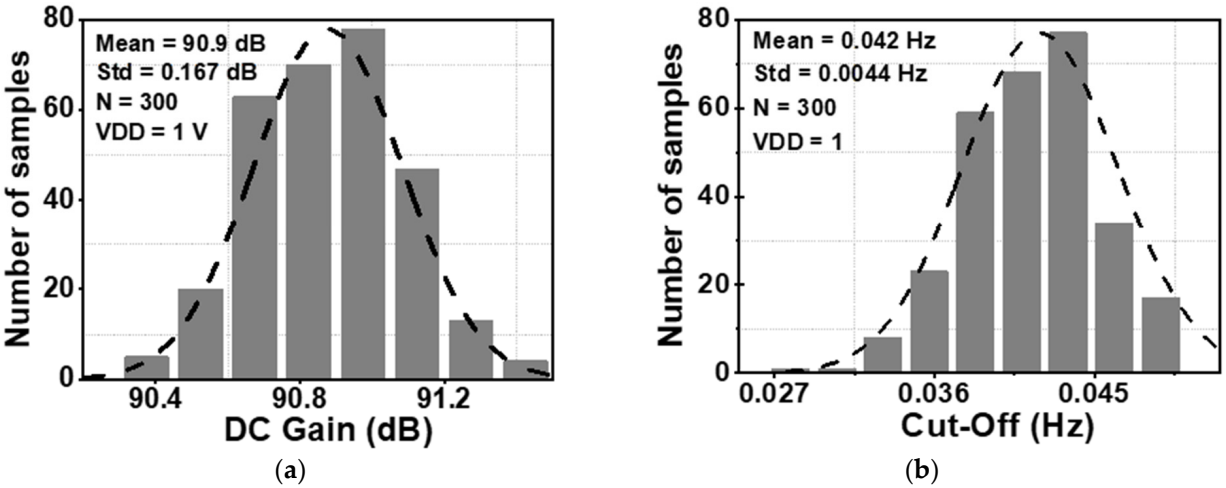
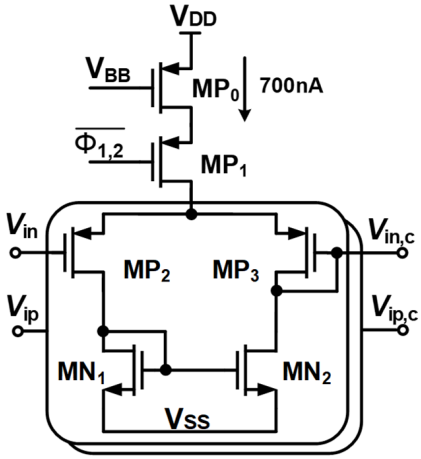


Figure 6. Monte Carlo simulation results for (**a**) DC gain, and (**b**) cut-off frequency of G_{m2}.

Figure 7 shows the schematic of the G_{mb} in the IBL. The MP0 and MP1 in G_{mb} are employed to bias and regulate the buffer with the purpose of reducing the impact of process variation on mismatch devices. The boosted input impedance in IBL can be affected by the pre-charge time T, the switches sizing of $\Phi_{1,2}$, and the buffer design. Figure 8 shows the clock generator for controlling the IBL. The pre-charge time T and $C_{lk1,2}$ are generated by

dividing the clock signal f_{CH}, which can be converted into a delayed signal by the use of several MOS capacitors and inverters. Although using a bias current of 700 nA, IBL is only enabled in 6 µs in each cycle of 100 µs (f_{CH} = 10 kHz); thus, IBL (G_{mb}) consumes only the current of 700 nA × 6/100 = 42 nA. The size and number of the MOS capacitor are shown in Figure 8. The sizing W/L of the switches $SW_{1,2}$ is set at about 0.5 µm/0.25 µm in order to minimize the inherent resistance. Furthermore, the pre-charge time T can be altered by using a two-switch $SW_{1,2}$ in order to mitigate the effect of process variability. This research examines the effect of the pre-charge time T and the size of the switches $\Phi_{1,2}$. Lengthening the pre-charge time T enhances the Z_{in} of the device, while simultaneously amplifying the noise of the device. The size of switches $\Phi_{1,2}$ in Figure 3 is another factor that affects the boost in Z_{in}. A small W/L size can result in a substantial voltage loss between these switches. Figure 9a and Figure 9b show the relationship between the Z_{in}, the input referred noise, the pre-charge time, and the switch sizing, respectively. As can be seen in Figure 9a, the Z_{in} improves from 2.5 MΩ to 0.7–1.8 GΩ when IBL is enabled with the pre-charge time T and is increased from 3 to 6 µs; however, the IRN increases sharply from 1.7 to 2.2 μV_{rms}. As shown in Figure 9b, when the switches sizing (Width-W) of $\Phi_{1,2}$ increases, the parasitic capacitors of these switches are also increased. When clock control for the pre-charge phase is applied to the gate of the CMOS transistor switches, the charge injection noise and clock feed-through increases [26,27], leading to an increase in the IRN. In this work, when the width of the switches sizing of $\Phi_{1,2}$ is changed from 1 to 5 µm, the IRN is increased from 1.8 to 2.1 μV_{rms}, while the noise increases from 2.5 to 3.2 μV_{rms} when W of $\Phi_{1,2}$ changes from 6 to 10 µm. According to the simulated results, as shown in Figure 9, in order to optimize Z_{in} and IRN, the pre-charge time T and the switches sizing $\Phi_{1,2}$ in this design are therefore set to 6 µs and W/L is set to 5 µm/0.5 µm.



The table sizing of the CMOS transistors

MP_0	75µm/0.7µm
MP_1	30µm/0.7µm
$MP_{2,3}$	30µm/0.7µm
$MN_{1,2}$	5µm/10µm

Figure 7. The schematic of the circuit in IBL with table sizing of the CMOS transistors.

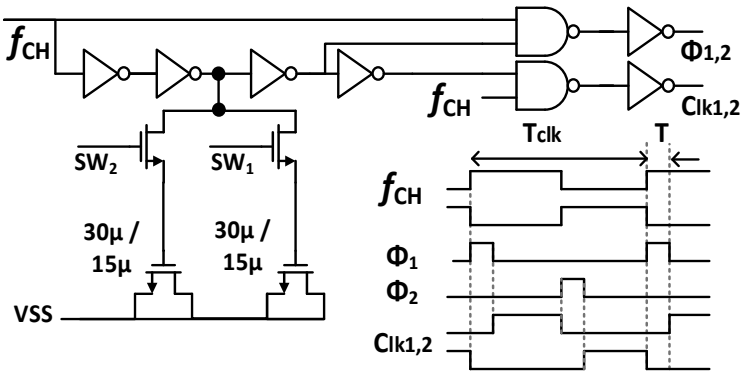


Figure 8. Schematic of a signal control generator for IBL.

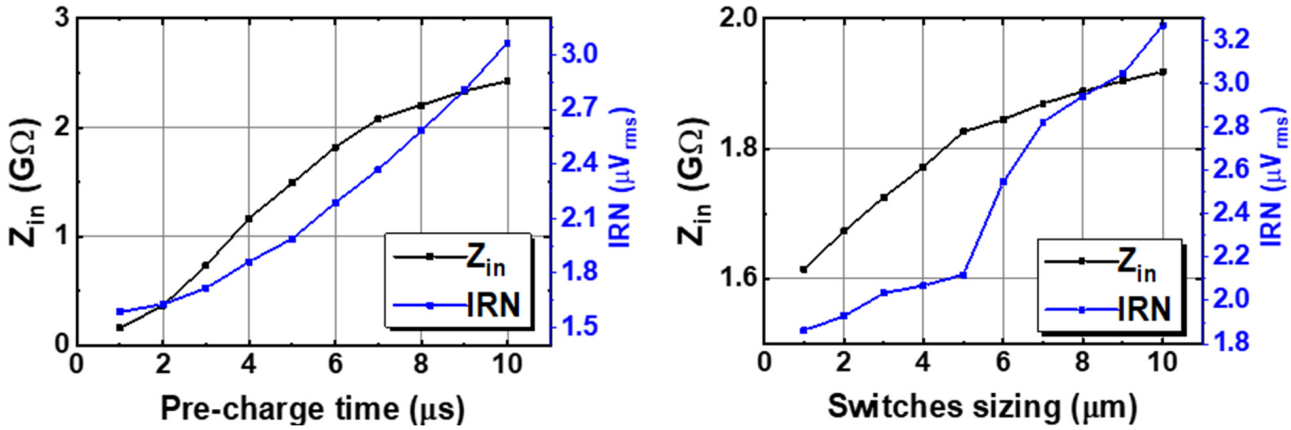


Figure 9. The relation between input impedance and noise to (**a**) the pre-charge time, and (**b**) the switches sizing.

4. Simulation Results

Figure 10 shows the layout of the proposed CCIA in the 180 nm CMOS process. The chip area of the CCIA configuration is 0.123 mm^2. Table 1 shows the power dissipation of each block in the CCIA. The total power consumption of the proposed CCIA is 1.87 μW from a V_{DD} of 1 V. G_{m1}, G_{m2}, G_{m3}, and G_{mb} consume 1400, 30, 400, and 40 nW, corresponding to 74.8%, 1.6%, 21.36%, and 2.24% of the total power consumption, respectively. According to the post-simulation results, it is shown that Figure 11 shows the simulated results of the CCIA's transfer function—(a) transient; (b) MCs. The CCIA's Av is 40 dB. The MCS results present that the MV of the closed-loop CCIA gain at 300 samples is 38.9 dB, with a Std of 0.28 dB. Figure 12 shows the MCS results for PSRR and CMRR after running 300 samples. At the 1 V supply, the MV of PSRR and CMRR are 108.6 and 118.7 dB with Stds of 23.7 and 24.4 dB, respectively.

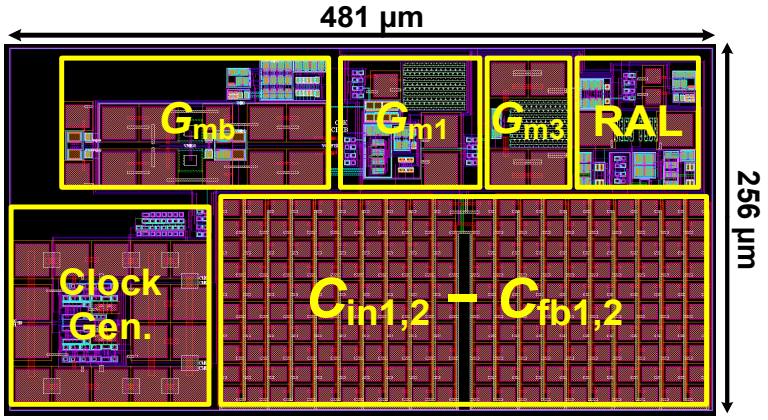


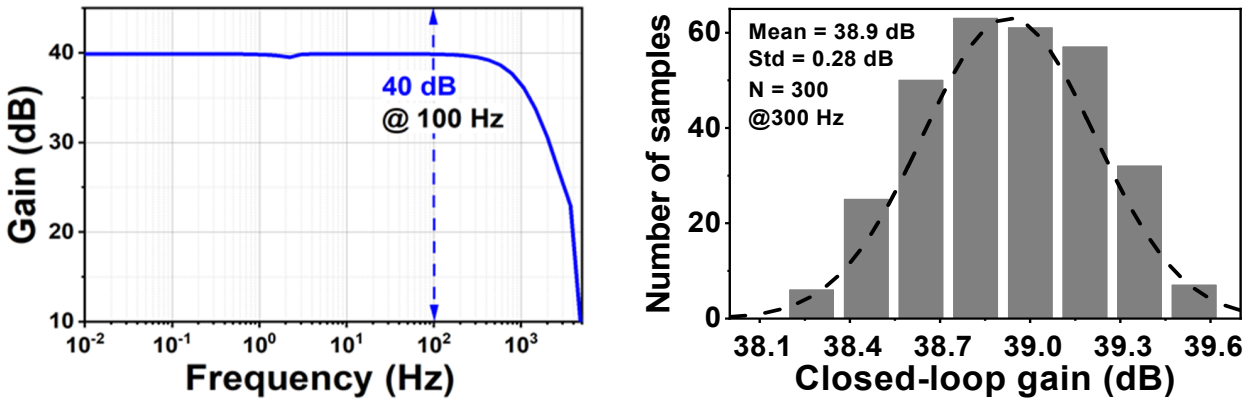
Figure 10. The layout of the proposed CCIA.

During the simulation, the input of the CCIA is configured so that it is short-circuited in order to test the output spectrum. Both V_{OS1} and V_{OS2} were set to a voltage of 5 mV. Figure 13 shows the simulated results of the voltage spectrum and the MCS of the output ripple. When the RAL is disabled, the amplitude of the output spectrum at the chopping frequency is about 82.2 mV, as shown in Figure 13a. The amplitude of the output ripple of the CCIA decreases to 0.36 mV when the RAL is enabled, as shown in Figure 13b. The output ripple is verified using an MCS that includes 300 samples and accounts for both local and global process variations. When the RAL level is changed from off to on, the MV of the output ripple decreases from 82.9 mV to 0.36 mV with a Std of 42.6 mV or 93 μV, as

shown in Figure 13c,d. The simulation results shown in Figure 14 therefore give an MV of 45.9 for the ripple attenuation, with a Std of 3.68 dB. The proposed feedback network effectively compensates for the offset voltage (V_{OS1}, V_{OS2}) caused by mismatches due to process, voltage, and temperature variations, resulting in a significant reduction in the output ripple voltage.

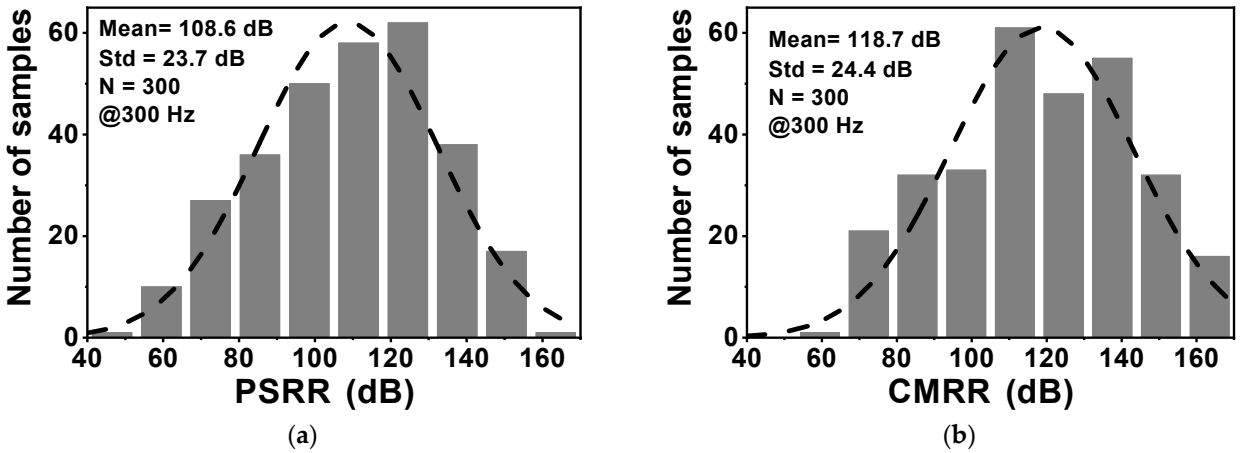
Table 1. The power dissipation of each block of the proposed CCIA.

Block	Circuit	Components	Power Dissipation (nW)
Dual_FC (G_{m1})	OPA-Dual FC	Differential Pair	500
		Differential Pair	500
		Cascode Branches	200
	CMFB		200
CS (G_{m3})	OPA-CS	Common source	400
RAL (G_{m2})	Stage-1	Differential Pair	5
	Stage-2	Common source	20
	CMFB2		5
IBL (G_{mb})	Buffer		42
	Total		1872



(**a**) (**b**)

Figure 11. (**a**) The transient of the proposed CCIA's transfer function; (**b**) MCS result of the proposed CCIA's transfer function.



(**a**) (**b**)

Figure 12. The MCS results of (**a**) PSRR; (**b**) CMRR.

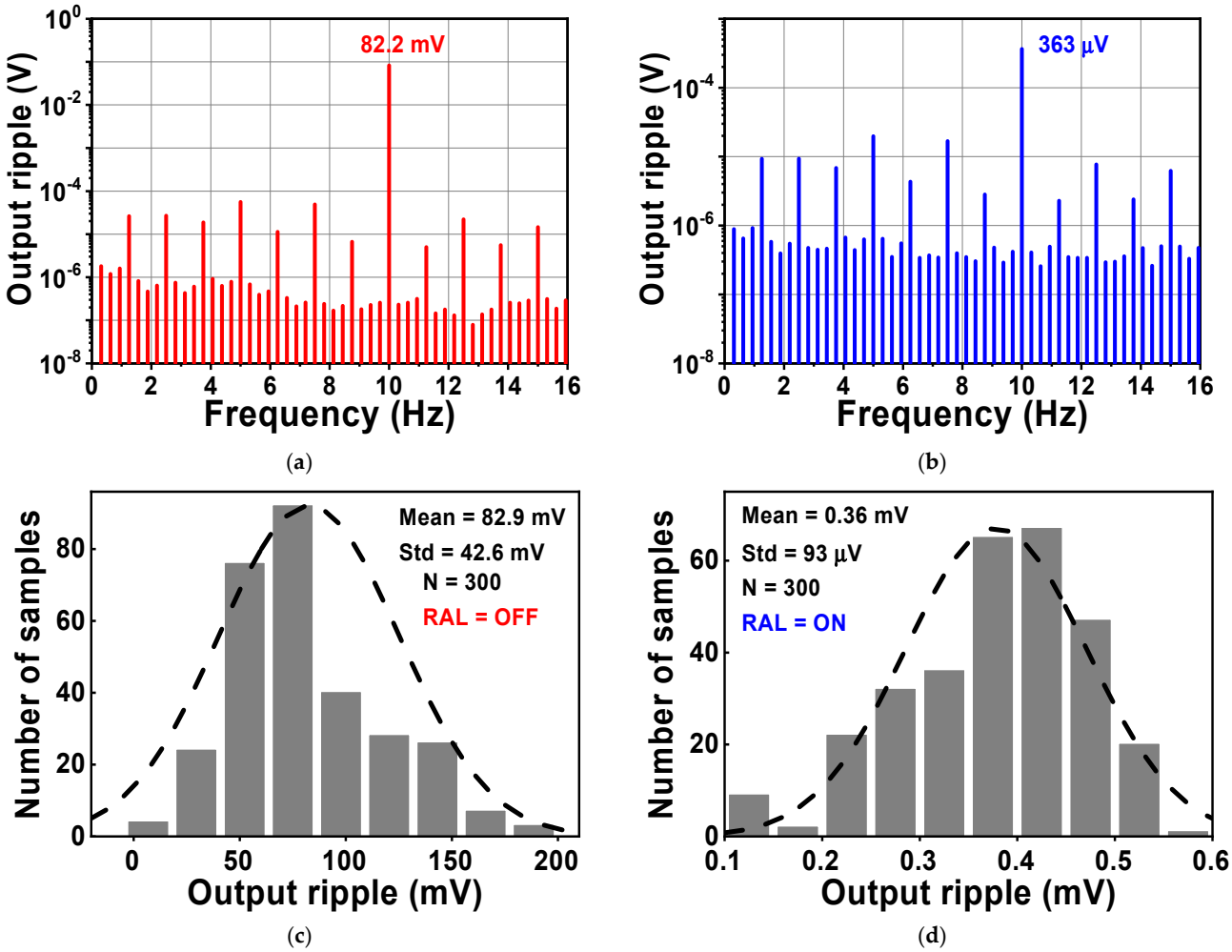


Figure 13. The simulated results of the voltage spectrum and MCS of the output ripple when RAL (**a**,**c**) is disabled, or (**b**,**d**) enabled.

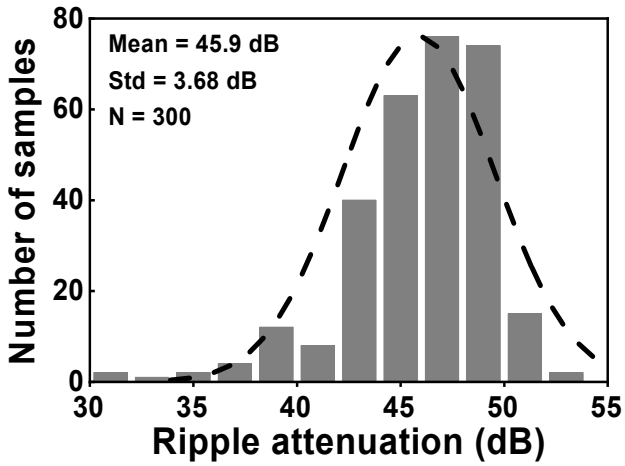


Figure 14. The MCS of the ripple attenuation result.

Figure 15 shows the effects of activating the impedance boost loop on the Z_{in} and the input-related noise. By setting the $SW_{1,2}$ parameter, it is possible to achieve different results for the input impedance. When $SW_{1,2}$ is set to 01 and 11, corresponding to a pre charge time of 3 and 6 µs, the Z_{in} in the low frequency range increases to about 0.7 and 1.8 GΩ, respectively, as shown in Figure 15a. Without the presence of IBL, the noise floor is about

119 nV/$\sqrt{}$Hz, while the $1/f$ corner frequency is 10 Hz. When IBL is enabled, the noise floor increases to 136 nV/$\sqrt{}$Hz, resulting in an IRN over a bandwidth of 1 to 200 Hz of 2.16 μV_{rms}. This increase is observed for different values of $SW_{1,2}$, which determines the pulse width of the pre-charge time. Figure 16a shows the variation of IRN for the proposed amplifier across several process corners, ranging from 1.9 to 2.6 μV_{rms}. On the other hand, Figure 16b shows the MV of IRN, which is 2.16 μV_{rms}, with a Std of 97.9 nV_{rms}, verified using an MCS with 300 samples, considering both local and global process variations.

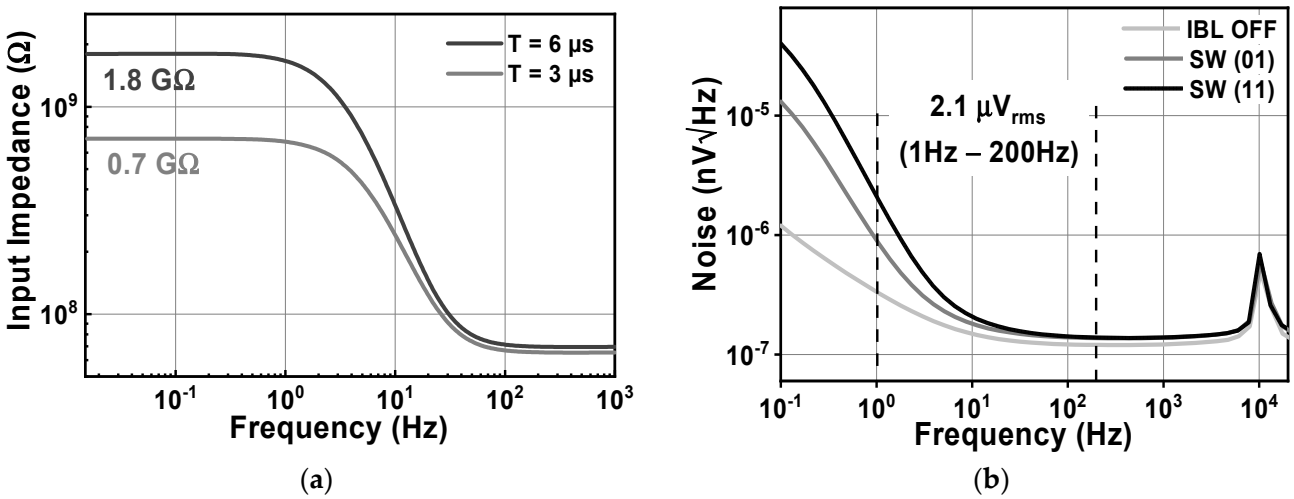


Figure 15. The simulated results of (**a**) the CCIA's input impedance; (**b**) the CCIA's noise.

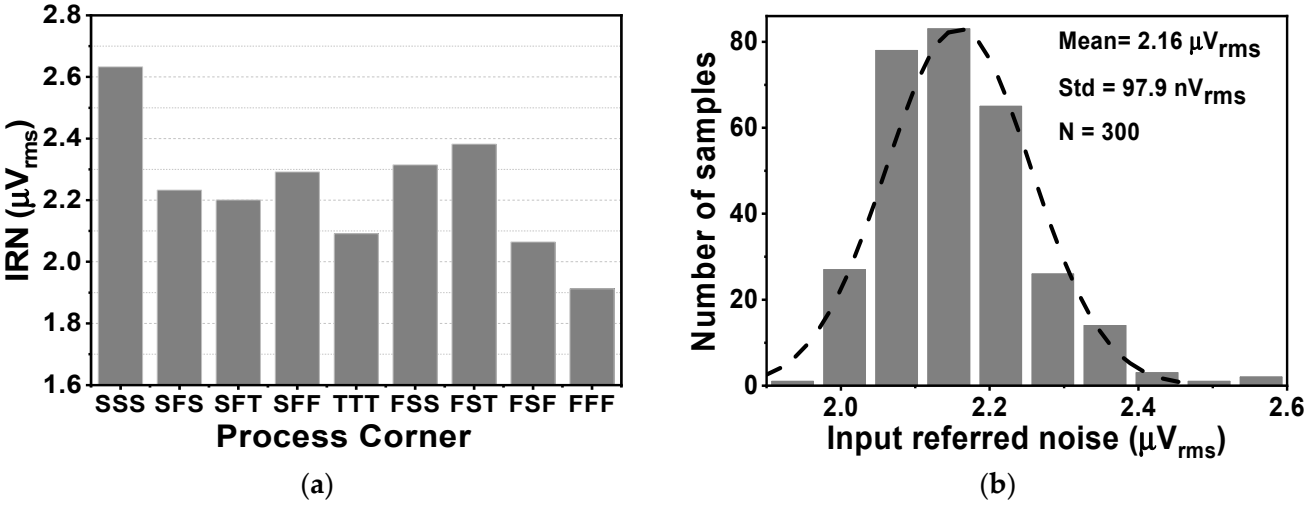


Figure 16. The simulated result of (**a**) the CCIA's noise across several the process corners and (**b**) the CCIA's noise.

Table 2 shows a brief summary of the primary design specifications, encompassing power consumption, output ripple's amplitude, Z_{in}, CMRR, PSRR, and NEF (noise efficient factor). There are several references that show simulation results, such as [24,28,29], in order to guarantee an equitable comparison. Table 2 is employed to evaluate the performance of the proposed design in comparison with the current state-of-the-art studies. The proposed CCIA obtains an NEF of about 7.5 by integrating RAL and IBL. Additionally, it exhibits a minimal output ripple of 363 µV and a significant Z_{in} of 1.8 GΩ. The CCIA's dissipation is 1.87 µW from a 1 V supply.

Table 2. Performance comparison.

Ref.	[18]	[23]	[24]	[28]	[29]	[30]	[31]	This Work
Year	2017	2021	2024	2022	2020	2021	2019	2024
Power (μW)	2	5.94	1.5	1.21	19.8	0.672	1.2	1.87
Supply (V)	1.2	1.8	2.47	1	1.8	2	5	1
Output ripple (mV)	0.012	NA	NA	0.061	NA	NA	NA	0.36
Ripple Attennuation (dB)	NA	NA	NA	>41	NA	NA	NA	45.9
Z_{in} (GΩ)	0.3	2.6	NA	NA	2.1	0.0575	400	1.8
Gain (dB)	25.7	40	59.7	40	46	40.6	20	40
PSRR (dB)	NA	85	>70	87	NA	84.2	N/A	108.6
CMRR (dB)	NA	93	>87	108	96	83.24	>70	118.7
IRN (μV_{rms})	9	1.4	1.18	1.8	1.9	2.01	3.7	2.16
NEF	7	NA	2.13	5.4	NA	2.63	NA	7.5
Tech. (nm)	40	180	130	180	180	350	180	180
Meas./Sim.	Meas.	Meas.	Sim.	Sim.	Sim.	Meas.	Meas.	Sim.

5. Conclusions

The paper presents a 1.87 μW capacitively coupled chopper instrumentation amplifier for biomedical recording. The output ripple is measured at 0.36 mV, and the input impedance is 1.8 GΩ. The CCIA chip occupies a chip area of only 0.123 mm^2 when implemented in a 0.18 μm CMOS technology. The ripple attenuation loop effectively decreases the output ripple of the proposed CCIA down to 0.36 mV. The CCIA is able to achieve a high input impedance of approximately 1.8 GΩ due to the impedance boosting loop. The low-power chopper amplifier has a power dissipation of 1.87 μW at a V_{DD} of 1 V. It also obtains a closed-loop gain of 40 dB, a PSRR of 108.6 dB, and a CMRR of 118.7 dB. The noise floor of the CCIA has a magnitude of 136 $nV/\sqrt{Hz}$, which leads to an IRN of 2.16 μV_{rms} across a bandwidth of 200 Hz. Thus, an NEF value of 7.5 is attained. This illustrates our ability to evaluate the performance of the proposed CCIA by comparing it to the most recent studies.

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