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An Extended Range Divider Technique for Multi-Band PLL

Rizwan Shaik Peerla [1], Ashudeb Dutta [1] and Bibhu Datta Sahoo [2,*]

[1] Department of Electrical Engineering, Indian Institute of Technology, Hyderabad 502205, India
[2] Department of Electronics and Electrical Communication Engineering, Indian Institute of Technology, Kharagpur 721302, India
* Correspondence: bsahoo@ieee.org

Abstract: This paper presents a multiplexer-based extended range multi-modulus divider (ER-MMD) technique for multi-band phase locked loop (PLL). The architecture maintains a modular structure by using conventional 2/3 divider cells and a multiplexer without adding any extra logic circuitry. The area and power overhead is minimal. The 2/3 divider cells are designed using true single phase clock (TSPC) logic for ER-MMD to operate in the sub-10 GHz range. A division range of 2 to 511 is achieved using this logic. The ER-MMD operates at a maximum frequency of 6 GHz with a worst-case current of 625 µA when powered with a 1 V supply. A dual voltage controlled oscillator (VCO), *L*5/*S* band PLL for Indian Regional Navigation Satellite System (IRNSS) application is designed, which incorporates an ER-MMD based on the proposed approach as a proof of concept. This technique achieves the best power efficiency of 12 GHz/mW, among the state-of-the-art ER-MMD designs.

Keywords: extended range multi modulus divider; multiplexer based divider; true single phase clock; multi-band phase locked loop

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1. Introduction

Modern system-on-chips (SoCs) frequently include a variety of modules that operate in various dedicated clock domains. For instance, multicore processors dynamically modify each core's clock frequency to enhance operational speed, power efficiency, and heat dissipation [1,2]. To satisfy a variety of applications [3,4], fractional-N phase-locked loops (PLLs) and frequency synthesizers are frequently utilized as clock generators. One of the key components in frequency synthesizers and PLLs is the programmable frequency divider [5–7]. High speed, low power, wide modulus range, low phase noise (PN), and high drive capability are desirable qualities in a programmable frequency divider. A PLL can provide clock signals with a broader frequency range due to a broad modulus range, which also increases reusability and speeds up time-to-market schedules.

One such application where a PLL divider plays a crucial role is location-based services (LBS), particularly for space applications or rescue and search operations [8]. To attain the necessary location accuracy, the LBS needs either a single global navigation satellite system (GNSS) frequency or several GNSS frequencies [9]. Numerous regional navigational systems exist, including GLONASS (Russia), Galileo (EU), and BeiDou (China). A system specifically designed for the Indian subcontinent is the Indian Regional Navigation Satellite System (IRNSS). This system uses navigation signal carrier frequencies of 1.176 GHz (*L*5-band with 24 MHz bandwidth) and 2.5 GHz (*S*-band with 16.5 MHz bandwidth) to provide extremely accurate LBS. In such instances, a conventional divider fails to operate at both the frequency bands, making extended range division obligatory.

The two prominent approaches for frequency division are programmable counter based divider [10] and multi modulus divider (MMD) [11]. While the earlier structure suffers from high loading and excess power, the later structure suffers from a limited division range ($2^{(N-1)}$ to $2^N - 1$, for N = 1, 2, and so on). Extra control logic should be added to MMD to widen the division range. For IRNSS applications, this requirement

becomes mandatory. According to [12], adding an OR-gate in the last stage of MMD will extend the division range, but this structure falls short when the PLL is operating in Fractional-N mode. To overcome this, a structure in [13] was proposed that adds extra control logic to MMD, which makes it work in Fractional-N mode. Even though these upgrades help in achieving extended range division, the main essence of the MMD is lost, i.e., the modular nature of the structure.

The proposed approach accomplishes three targets:

- An extended range division is achieved using conventional blocks;
- The modular nature of the proposed approach makes the layout compact, thereby minimizing the area overhead;
- The digital divider design of the MMD up to sub-10 GHz reduces the power overhead.

The only limitation of the proposed work is excess loading on the input of the divider, which limits the maximum operating frequency. This work presents an extended-range MMD approach built using conventional MMD blocks. Section 2 presents the conventional feedback divider techniques. A brief overview of extended-range MMDs are presented in Section 3. The proposed ER-MMD structure and operation are discussed in Section 4. As a proof of concept, a design example of $L5/S$ band PLL using the proposed ER-MMD is studied in Section 5, where dual band PLL is briefly discussed. The measurement results and performance comparison validates the proposed ER-MMD operation in Section 6, followed by the conclusion.

2. Feedback Divider in PLL: An Overview

The majority of prior programmable frequency divider structures are based on programmable counters and 2/3-dividers [10,14]. These two well-known programmable frequency divider architectures are covered in this part, along with some cutting-edge methods for enhancing speed, phase noise, and modulus range.

2.1. Programmable Counter Based Divider

Figure 1a illustrates the design and working of the programmable counter-based divider. It is made up of a programmable counter (PC), a programmable swallow counter (SC), and a dual-modulus prescaler (DMP). When the modulus control signal (MC), which is produced by the programmable swallow counter, is 0 and 1, the DMP_{OUT} is configured to be N and $(N-1)$, respectively. The timing diagram of the pulse-swallow counter is shown in Figure 1b. A prominent MMD structure is shown in Figure 1c. The operation of a pulse-swallow counter is as follows.

- The value of PC (P) is always greater than SC (S);
- Initially, MC is high and both PC and SC start counting in $(N-1)$ mode;
- As $P > S$, first SC reaches *end-of-count* (EOC) and changes MC from high to low;
- The remaining $(P-S)$ cycles are counted in N mode.

The frequency division ratio N_{DIV} is thus determined by (1).

$$N_{DIV} = S \cdot (N-1) + (P-S) \cdot N = S + N \cdot P \tag{1}$$

The flowchart depicting the operation of the programmable counter-based divider is given in Figure 2. It should be noted that three variables define the division ratio, N. As a result, the modulus range of the programmable swallow-counter-based dividers is quite broad. However, the DMP directly drives two counters, which increases the output load capacitance for the DMP and impairs high-speed functioning. On the other hand, the two counters continue to operate, increasing power usage. In order to conserve energy, a programmable divider based on a single programmable counter acting as both an SC and a PC was published in [15]. A sub-integer-based clocked divider is presented in [16]. By implementing a modified EOC generation mechanism that relaxes the timing requirement, the speed of the programmable counter has been increased [17].

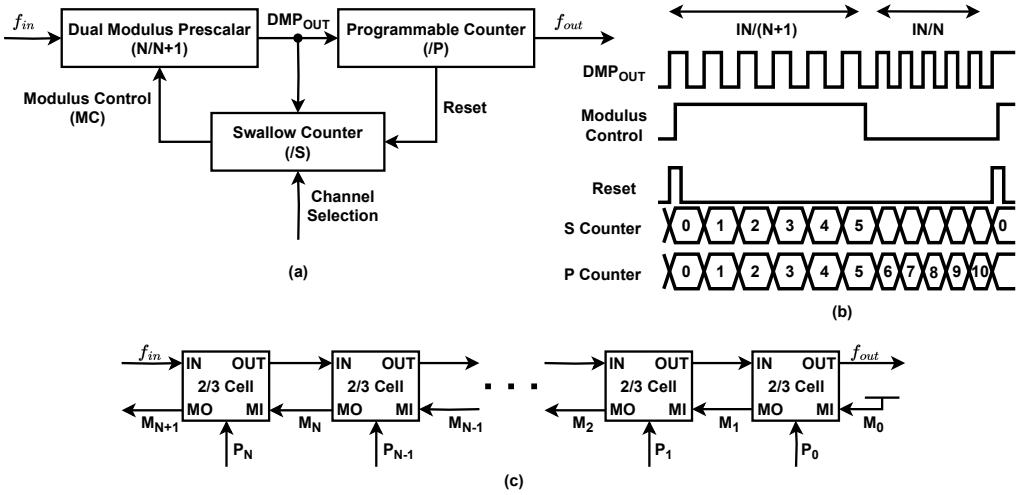


Figure 1. (**a**) Block diagram of conventional pulse-swallow-based feedback divider, (**b**) timing diagram showing the operation of a pulse-swallow counter, and (**c**) block diagram of conventional 2/3 cell-based MMD structure.

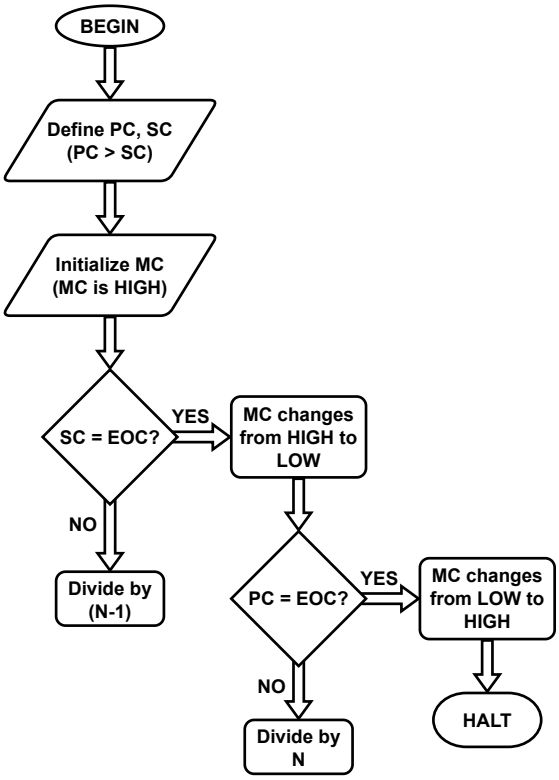


Figure 2. Flowchart showing the working principle of the pulse-swallow feedback divider.

2.2. Multi Modulus Divider Topologies

A standard MMD is depicted in Figure 1c and features an input (IN) and an output (OUT). The division ratio is controlled by modulus control (MI) and programming pin (P_i, where i = 0 to N). Depending upon the choice of MI and P_i, an appropriate modulus out (MO) is generated, which acts as MI to the next stage. For logic high values of MI and P_i, a divide-by-3 output is generated. Independent of what P_i is, the 2/3 cell operates in a divide-by-2 mode when MI is logic low. Table 1 summarizes the operation of a standalone 2/3 MMD cell. By adding multiple 2/3 cells, the division ratio can be increased. In such a scenario, the MI of the final 2/3 stage is connected to the supply (V_{DD}).

Table 1. Working of standalone 2/3 MMD cell.

Input	P_i	*MI*	Output
f_{in}	X	0	$f_{in}/2$
f_{in}	0	1	$f_{in}/2$
f_{in}	1	1	$f_{in}/3$

When the required division ratio of a PLL band falls outside the MMD range, this structure does not work. The MMD division range is expressed as in (2),

$$N = 2^0 P_0 + 2^1 P_1 + 2^2 P_2 + \cdots + 2^n P_n \tag{2}$$

where n is the total number of 2/3 divider cells (n = 0, 1, 2, so on) and P_i, where i = 0 to n, is the 2/3 cell digital control. Hence, the conventional MMD division range is limited to 2^n to $2^{n+1} - 1$. For instance, the division range for a 5-stage MMD is between 32 and 63.

3. Extended Range Divider Topologies

In order to extend the division range, a programmable chain of 2/1 frequency dividers was proposed in [18]. This achieves a full division range of 1 to 256 using an 8-stage divider. The 2/3 cell is built using conventional logic gates and D-flip–flops [12,19,20]. The power and delay are further optimized when the 2/3 cell is designed by low-leakage true single-phase clock (TSPC) flip–flops [21].

A straightforward dual-modulus divider was initially used to replace the $P - S$ counter, as shown in Figure 3a. Each cell's division is set to either 2 or 3, and many such 2/3 divider cells are placed to meet the required division range. When the control signal $P = 0$, the cell divides by 2, and when the control signal $P = 1$ then the cell divides by 3. To overcome this limitation, the structure in Figure 3b was proposed (discussed in Section 2.2). According to [12], an OR-gate was used to deactivate the final stage of an MMD, further extending the division range, as shown in Figure 3c. However, this structure does not work when the divider division is varying dynamically, as in the fractional-N PLL. The fractional operation might not succeed due to the inactive stage. This issue was addressed in [13], where the seamless division was accomplished by incorporating additional control logic into the traditional MMD (Figure 3d). The output of the intermediate stages is passed through to a multiplexer (MUX) to increase the divider modulus range, which distorts the MMD's modular design. The frequency range is enlarged in [22] by adding the logic of [12] to each 2/3 cell, which optimizes the first 2/3-cell, which works at the maximum frequency. Each of the aforementioned structures modifies the modular design of MMD and complicates the structure.

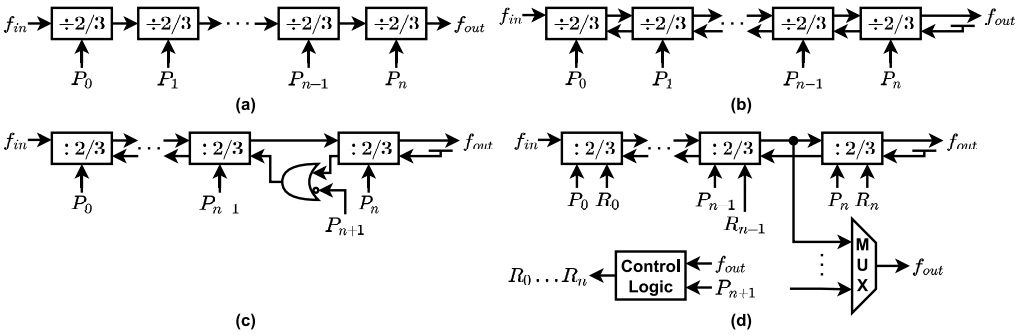


Figure 3. Block diagram depicting structures of (**a**) dual modulus divider, (**b**) prominently used MMD, (**c**) extended range MMD implemented in [12], and (**d**) the extended range MMD proposed in [13].

4. Proposed Extended Range MMD Structure

In Figure 4, the block diagram of the proposed extended range MMD is displayed. There are N sets of MMDs, each one generating a unique division range. The first set has only one 2/3 cell. The second set has two 2/3 cells providing a frequency division from 4 to 7. The number of sets can be increased depending on the logic in which the 2/3 cell is implemented. All MMD set outputs are fed to a MUX, and the required output is then delivered as a feedback signal to the phase frequency detector (PFD). The working of the proposed ER-MMD is as follows: The PLL output is given as input to all sets of the MMD. The output of each set is given to an input of an MUX. The output of the MUX can provide an extended range division ranging from 2 to $2^N - 1$, where N is the number of 2/3 cells in the last MMD set. The D-flip–flop of the 2/3 cell can be implemented using different logic. Each type of logic has its own set of requirements and provides certain pros and cons.

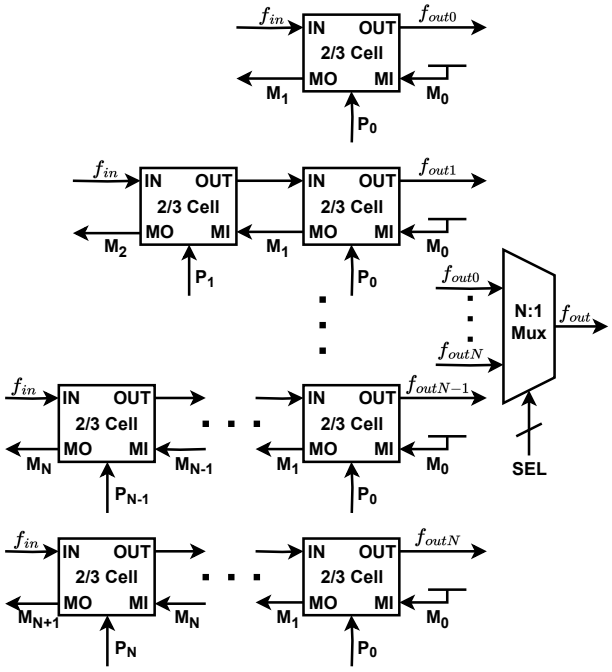


Figure 4. Block diagram of the proposed multiplexer-based ER-MMD.

4.1. D-flip–flop Structures for Divider

High-frequency division is accomplished with an analog frequency divider, which consumes more power but does not require rail-to-rail input signal swing. Figure 5a depicts the divide-by-2 cell and D-latches implemented using current mode logic (CML). Each D-latch is made up of a cross-coupled pair that is connected in a positive feedback arrangement to create negative transconductance and maximize operating frequency. One clock is utilized to drive each D-latch with complimentary clock phases, one of which is used for the flipping circuit and the other for the latching circuit. When CLK is high, M_5 switches ON. The differential pair ($M_{1,2}$) compares the input amplitudes at the gate terminals and transfers the result to the output nodes. When CLK is low, M_6 switches ON, and the output is held by the regenerative pair transistors ($M_{3,4}$). Because $M_{1,2}$ controls how quickly input amplitudes are sensed and transported to the output nodes, they determine the maximum operating frequency.

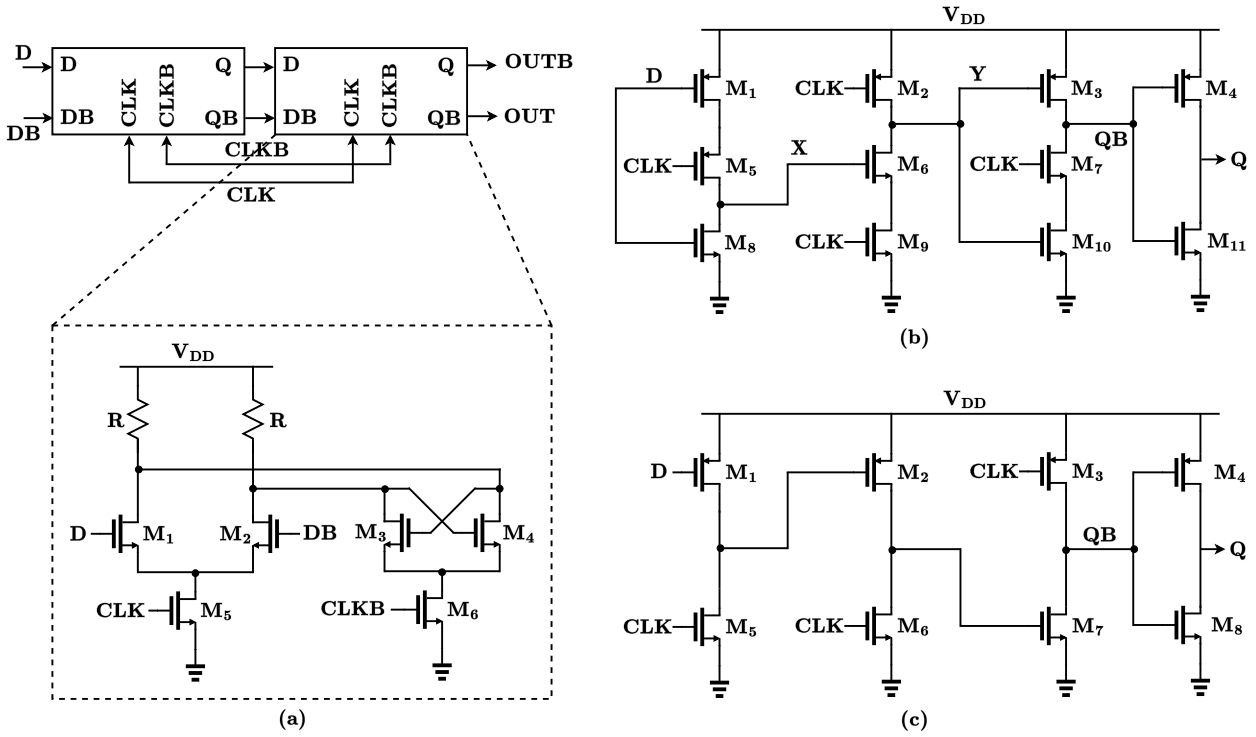


Figure 5. Block diagram of (**a**) CML divide-by-2 and basic circuit implementation of D-flip–flop, (**b**) simple TSPC logic-based D-flip–flop circuit, and (**c**) extended TSPC (E-TSPC)-based D-flip flop circuit.

In a digital frequency divider, the input clock must have a nearly rail-to-rail voltage swing in order to achieve proper frequency division. The divider based on a true single-phase clock (TSPC) D-type flip–flop shown in Figure 5b is based on dynamic logic. It has nine transistors and only uses a single clock. There are two modes in TSPC flip–flop operation: hold mode and evaluation mode. During hold mode, CLK is low, making node X pre-charge to a value based on the input D and node Y to pre-charge to VDD. The output QB is floating as transistors M_3 and M_7 are OFF. In the evaluation mode, CLK is high. If node X is pre-charged to VDD during hold mode, node Y is discharged, causing QB to be pulled up by transistor M_3. If node X is pre-charged to 0 during the hold mode then node Y is not discharged and QB is pulled down by transistors M_7 and M_{10}. The operation frequency can be higher than the static logic divider due to the low transistor count and short input-to-output delay. The MMD can operate until sub-10 GHz, depending upon the technology.

Another structure that uses dynamic logic is the extended true single phase clocking (E-TSPC)-based D-flip–flop. This is realized by using 6 transistors, as shown in Figure 5c, thereby reducing the critical path, which in turn enhances the operating frequency. The operation of an E-TSPC flip–flop is discussed in detail in [23]. The propagation delay and power consumption analysis are presented in [24]. Because of the static current and noise immunity issues, the E-TSPC circuit needs special care during its design. They are suitable for low-supply voltage and low-power applications. The frequency of operation is better than the TSPC-based D-flip–flop. The overall performance comparison of all three structures is tabulated in Table 2. Depending upon the target frequency, power requirement, and output phases, one can choose the suitable D-flip–flop logic.

Table 2. Performance comparison between CML, TSPC, and E-TSPC D-flip–flop.

	CML	TSPC	E-TSPC
Speed	High	Moderate	High
Input Swing	Low	Rail-to-Rail	Rail-to-Rail
Output Swing	Low	Rail-to-Rail	Rail-to-Rail
Output Phases	Diff.	Diff./Single	Diff./Single
Input Clock	Diff.	Single	Single
Power	High	Low	Moderate

4.2. Circuit Implementation

In this work, the 2/3 cells are implemented using TSPC logic. The combinational logic, except for an inverter, is incorporated inside the flop to lessen propagation delay and current consumption [25]. The TSPC flop structure is shown in Figure 6. The flop is built as a single circuit that includes the conventional D-flip–flop, *AND* gate, and *OR* gate. The main advantage of this structure is that it requires only single input and produces peak-to-peak output, because of which the intermediate buffer stages are not required. The ER-MMD design is simulated in UMC 65-nm CMOS. The TSPC-based MMD works up to 6-GHz across process, voltage, and temperature (PVT). This means a maximum of eight 2/3 MMD sets can be incorporated, proving a division range from 2 to 511.

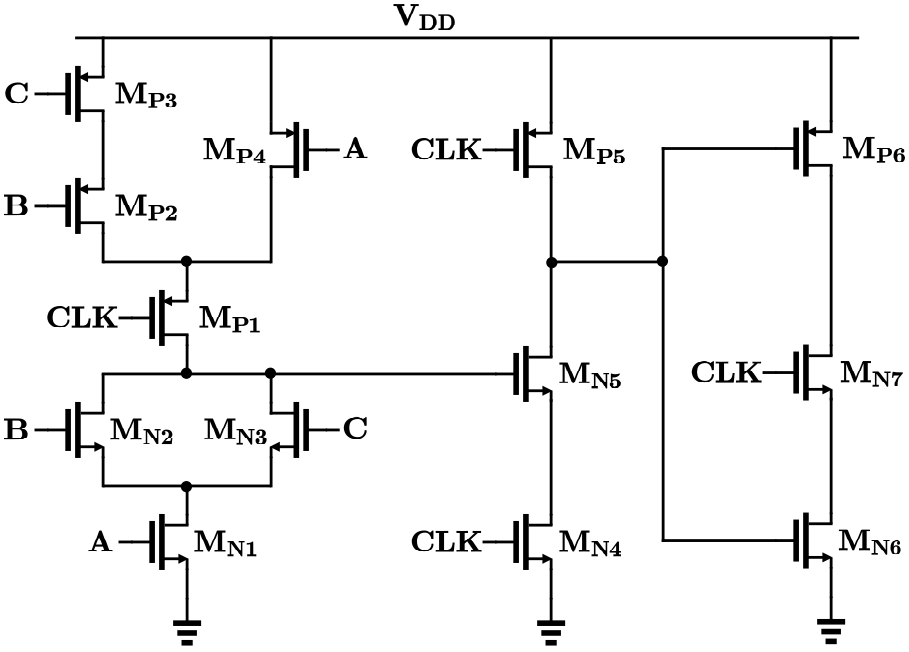


Figure 6. Circuit implementation of TSPC flop [25].

The current consumption, rise time, and fall time of the ER-MMD are summarized for three process corners, *viz.*, *slow–slow* (SS), *fast–fast* (FF), and *typical–typical* (TT). For each of the three process corners the current consumption, rise time, and fall time of the MMD output was simulated for three temperatures, *viz.*, -40°, 27°, and 85°, and three voltages, *viz.*, 0.9 V, 1 V, and 1.1 V, which is actually $\pm 10\%$ supply voltage variation.

The first 2/3 cell is the most power-consuming block. Figure 7 shows the current consumption of the proposed ER-MMD, which ranges from 370 µA to 610 µA across

PVT. The rise time and fall time (10% to 90% of supply) of the proposed ER-MMD output at 6-GHz input across PVT is shown in Figures 8 and 9, respectively. Even though the maximum variation in the rise and fall time across PVT is 1.5 ps and 1 ps, respectively, the proposed ER-MMD produces the desired output. This approach can extend the maximum division ratio from 511 to 1023 using E-TSPC logic in the first few stages and further using CML logic. Even though the ER-MMD designed using CML logic comes at a cost of very high power and stringent layout complexities, the CML logic is preferred for a PLL designed to work at *mm* -wave frequencies.

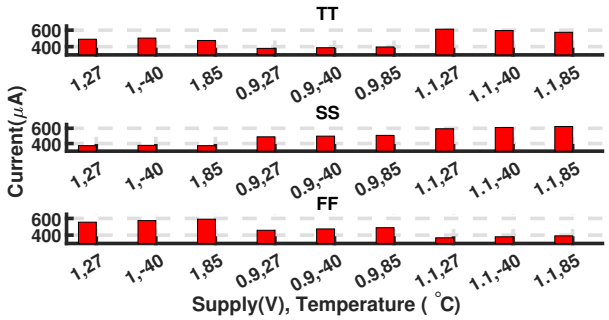


Figure 7. Current consumption of the proposed ER-MMD across PVT.

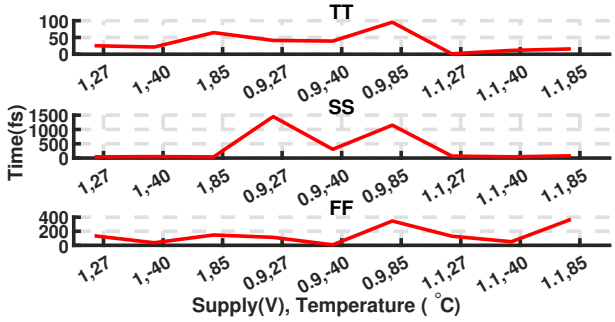


Figure 8. Extracted simulation of rise time of ER-MMD output with 6 GHz input across PVT.

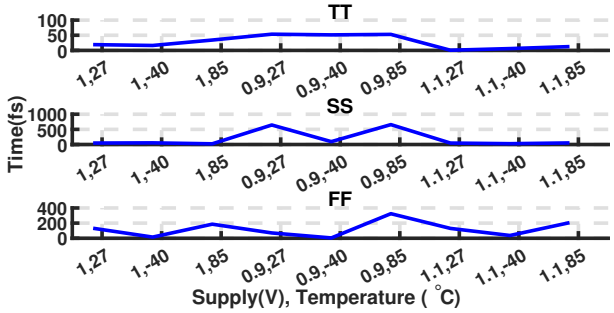


Figure 9. Extracted simulation of fall time of ER-MMD output with 6 GHz input across PVT.

The limitation of this structure is the extra loading on the input. At high frequencies, this constraint is very critical. The parasitic capacitance (C_{par}) at the input of the first 2/3 cell when supply is *ON* and *OFF* are tabulated in Table 3.

Table 3. Parasitic capacitance impact of first 2/3 cell and complete ER-MMD in *ON* and *OFF* state.

	Single 2/3 Cell		**Complete ER-MMD**	
	ON State	**OFF State**	**All Sets ON**	**Single Set ON**
C_{par}	15 fF	12 fF	120 fF	96 fF

A 20% reduction in C_{par} is observed when the 2/3 cell is OFF. From this observation, one way to reduce the extra loading is to power ON only one 2/3 set at a time. The total C_{par} when all sets are ON and only one set is ON is tabulated in Table 3. Thus, the extra C_{par} added in the proposed ER-MMD compared to a conventional MMD is reduced from 8 times to 6.4 times. This is the reason for ER-MMD to operate only up to 6 GHz using TSPC logic. There is no work in the literature that analyzes the effect of loading on the frequency of operation. The extension of this work would be to build an extended range MMD with minimal loading while maintaining the modular structure of the 2/3 cell.

5. Design of L5/S Band Dual VCO PLL

The work published in [26] is briefly discussed as proof of concept. Figure 10 shows a comprehensive block diagram of PLL. A pre-divider of 5 divides the crystal frequency of 26 MHz to 5.2 MHz (f_{REF}), which is enough to accomplish both $L5$ and S bands while the PLL is in integer mode. The PLL loop dynamics are chosen to ensure acceptable loop bandwidth and stability. The typical PFD, charge pump (CP), and a second-order loop filter are employed. The lower PLL loop bandwidth is supported by a nominal settling time for improved far-out PN.

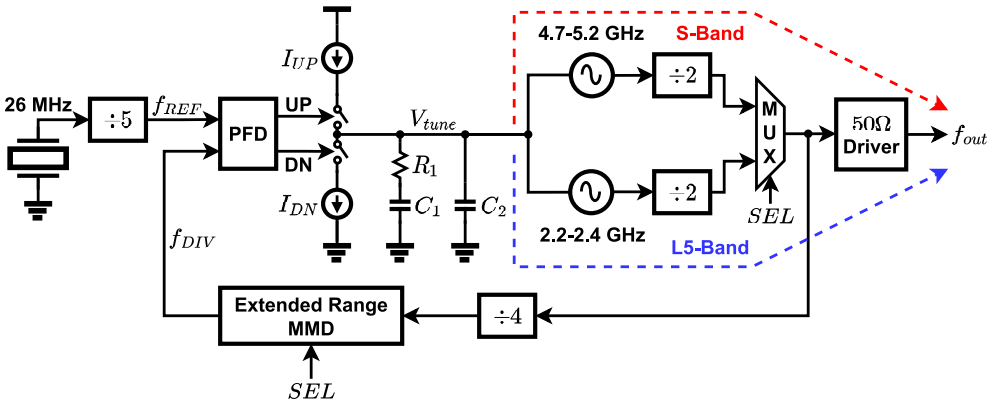


Figure 10. Dual VCO-based $L5/S$-band PLL block diagram designed in [26].

The PLL loop bandwidth is chosen to be less than $f_{REF}/20$. To lessen the current mismatch, an off-chip low drop-out regulator (LDO) supplies the CP current (I_{CP}). For PLL stability, a phase margin of 49°and above is maintained over the complete frequency range. Using the loop parameters (f_{REF}, feedback division ratio, I_{CP}, and VCO gain), passive loop filter (second order) values are chosen. A C_1 of 150 pF, C_2 of 15 pF, and R_1 of 50 KΩ, (see Figure 10) accomplishes phase margin of 54°and 49°, maintaining a loop bandwidth of 97 KHz and 140 KHz for S-band and $L5$-band, respectively.

In Figure 11, the block diagram of the ER-MMD is depicted, which is a sub-set of the ER-MMD shown in Figure 4. There are two sets of MMDs used, one with 5-stage TSPC 2/3 cells and the other with 6-stage cells. Both sets receive the divide-by-4 output of the VCO as input. Both MMD set outputs are fed into a simple MUX, and the desired output is then delivered as a feedback signal to the PFD. Table 4 illustrates how the proposed ER-MMD functions. MMD with six stages is operational when SEL is high. When the input control bits P[5:0] is used, an output in the range of $f_{in}/64$ to $f_{in}/127$ is produced. MMD with five stages is operational when SEL is low. An output between $f_{in}/32$ to $f_{in}/63$ is produced when control bits P[4:0] are prfovided as inputs.

The proposed ER-MMD has minimal additional die area. The ER-MMD has a negligible power overhead because it operates at a sub-GHz frequency. For both sets of MMDs, the control signals P_0 to P_4 are utilized. As a result, the goal of adopting a conventional design and creating an ER-MMD functioning from 32 to 127 is realized with low area and power overhead.

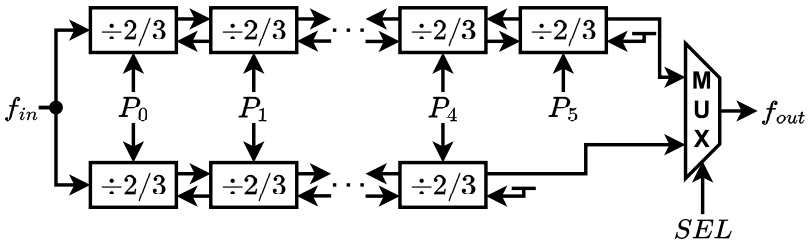


Figure 11. Block diagram of the proposed extended range MMD designed in [26].

Table 4. Fuctioning of proposed ER-MMD.

	***L5* Band**	***S* Band**	**Division Range**
MMD control bits	P[4:0]	P[5:0]	
SEL = 0	Yes	No	32 to 63
SEL = 1	No	Yes	64 to 127

5.1. VCO, CML Divider, and MUX

A differential LC-VCO that runs at double the intended local oscillator (LO) frequencies is employed. The I/Q LO signals are produced using a divide-by-2 CML device. The desired band is chosen at the output using the CML MUX. The operating frequencies of the VCO for the *L*5-band are 2.2–2.4 GHz, and for the *S*-bands are 4.7–5.2 GHz. Table 5 provides an overview of both VCOs frequency and PN. The divide-by-4 receives the output of the MUX as input before sending it to the MMD.

Table 5. Frequency planning, current consumption, and targeted PN for VCOs.

	***S*-Band**	***L5*-Band**
VCO Frequency (MHz)	4700–5200	2200–2400
LO Frequency (MHz)	2350–2600	1100–1200
Center Frequency (MHz)	2495.02	1178.45
Current (mA)	3.5	5
PN @ 1 MHz (dBc/Hz)	−120	−120
PN @ 100 KHz (dBc/Hz)	−90	−90

A complementary cross-coupled LC-VCO is used in this PLL. For discrete tuning, a binary weighted, 4-bit switched capacitor array (SCA) is incorporated. Two varactors biased at different bias voltages are designed for fine-tuning with good linearity [27]. The quality factor (Q) for both VCO across the frequency range is maintained above 10 by sizing them appropriately. The CML MUX output is routed to I/O pads via a 50 Ω driver.

5.2. PFD, CP, and Loop Filter

The PLL PN, especially the in-band PN, rest on the non-linearity of PFD and CP. In this work, PFD based on conventional D-flip–flop is used. An appropriate delay is added in the reset path to overcome the *dead-zone* issue [28]. The CP implementation is based on the switch-to-drain architecture [28]. The CP current is fixed at 0.35 mA and avoids programmability. Thus, the current is provided using an off-chip LDO in order to minimize the ripple on V_{tune}. The loop parameters are chosen carefully due to the lack of CP programmability. A single loop filter is utilized for both LC-VCOs.

6. Measurement Results

A narrow-band dual-VCO PLL was fabricated using the UMC 65-nm CMOS process. When powered using a 1 V supply, the PLL consumes 7.9 mW in the *L*5-band and 6.4 mW in the *S*-band. The PLL core size is 1.4 mm^2 (ref. Figure 12). The area of the proposed ER-MMD is 300 µm × 20 µm, as shown in Figure 12, which is negligible compared to the overall chip area. Due to two on-chip passive inductors, the large chip area is understandable. Even with ER-MMD of Figure 4, the chip overhead is minimal. The two inductors are positioned as far apart as feasible and are adequately insulated to prevent any coupling between them. The test board is mounted with a 68-pin QFN package die. An LDO installed on the test board supplies the 1.0 V supply. An Agilent EXA N9010A signal-analyzer is used for PN measurement.

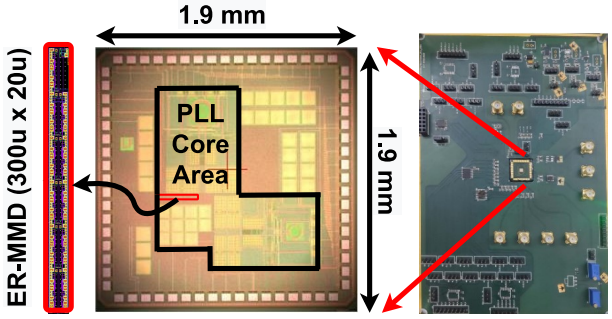


Figure 12. PCB mounted die micrograph of the dual VCO *L*5/*S* band PLL highlighting the proposed ER-MMD.

For the *L*5-band, an MMD set with 5 stage TSPC 2/3 cells is active. A division ratio of 57 is selected, which produces 5.2 MHz divider output. The PN of LO measured at the *L*5-band is shown in Figure 13. The PLL attains the PN of −49.44 dBc/Hz, −95.63 dBc/Hz, and −121.25 dBc/Hz at 10 KHz, 100 KHz , and 1 MHz offset, respectively. For *S*-band, MMD set with 6 stage TSPC 2/3 cells is active. A division ratio of 120 is selected which produces 5.2 MHz divider output. The PN of LO measured at the *S*-band is shown in Figure 14. The PLL attains the PN of −57.42 dBc/Hz, −94.56 dBc/Hz, and −120.12 dBc/Hz at 10 KHz, 100 KHz, and 1 MHz offset, respectively. The phase noise results prove the dual VCO *L*5/*S* band PLL, and thereby the proposed ER-MMD structure is working.

Table 6 compares the proposed ER-MMD with recent techniques. The work in [29] provides a 1 to 256 division ratio and also produces 50% duty cycle, but consumes higher power. The maximum operating frequency of the work in [5] is half of the proposed structure. Although the maximum frequency in [6] is a little high, the division ratio provided is limited.

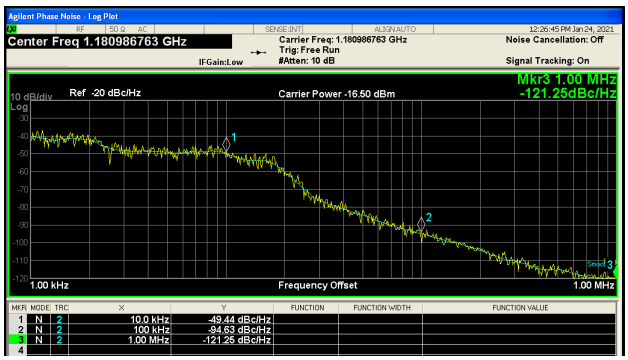


Figure 13. Measured LO PN at *L*5-band when ER-MMD division ratio is set to 57.

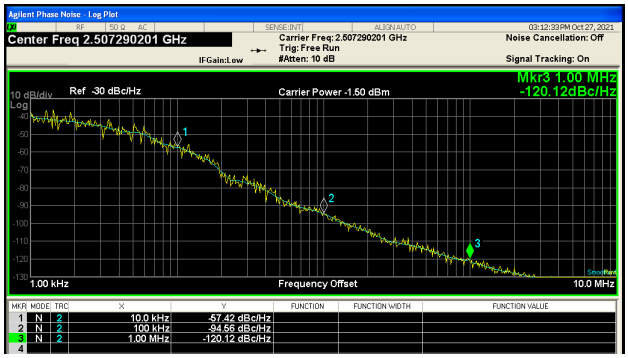


Figure 14. Measured LO PN at S-band when ER-MMD division ratio is set to 120.

Table 6. Performance comparison of ER-MMD with recent structures.

	This Work †	[29]	[5] ‡	[6]
Technology (nm)	65	180	130	65
Division Ratio	2–511	1–256	128–192	24–80
Supply (V)	1	1.8	1.2	1
Max. Frequency (GHz)	6	2.3	3	6.5
PN at 1 MHz offset (dBc/Hz)	−155	−140	NA	−141
Div. Power (mW)	0.5	3.4	NA	1
Power Efficiency (GHz/mW)	12	0.68	NA	6.25
50% Output Duty Cycle	No	Yes	No	No

† R + C + CC Extracted simulation. ‡ Extracted simulation.

7. Conclusions

A multiplexer-based ER-MMD approach is presented for multi-band PLLs. Conventional feedback divider techniques are discussed. Previous extended-range MMD architectures are examined. The design details of the proposed ER-MMD are given. The 2/3 cell is implemented in TSPC logic. Another logic implementation such as CML and E-TSPC is also examined, summarizing the pros and cons of each logic. As a proof of concept, a dual VCO *L*5/*S* band integer-N PLL is designed in UMC 65-nm CMOS, incorporating the proposed ER-MMD with 32 to 127 division ratio. The performance comparison shows that the proposed ER-MMD has better supply efficiency, maintaining the modular structure and minimal area overhead.

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