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A 0.6 V Bulk-Driven Class-AB Two-Stage OTA with Non-Tailed Differential Pair

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Abstract: This work presents a two-stage operational transconductance amplifier suitable for sub-1 V operation. This characteristic is achieved thanks to the adoption of a bulk-driven non-tailed differential pair. Local positive feedback is exploited to boost the equivalent transconductance of the first stage and the quasi-floating gate approach enables the class AB operation of the second stage. Implemented in a standard 180 nm CMOS technology and supplied at 0.6 V, the amplifier exhibits a 350 kHz gain bandwidth product and a phase margin of 69° while driving a 150 pF load. Compared to other solutions in the literature, the proposed one exhibits a considerable performance improvement, especially for large signal operation.

Keywords: body-driven amplifier; low-power; low-voltage; positive feedback

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1. Introduction

In applications that require low power consumption, such as implantable biomedical devices, sensor nodes for the Internet of Things, and energy-harvesting battery-less devices, the design of analog circuits has become a challenging task. Indeed, while in these applications the digital part benefits from the technological scaling in terms of energy consumption reduction and performance enhancement, the performance of analog circuits decreases when technology is scaled down due to the reduced intrinsic gains of transistors and of the signal-to-noise ratios [1,2]. These disadvantages are exacerbated when the supply voltage is reduced below 1V, in which the design of the operational transconductance amplifier (OTA), representing the universal and fundamental building block of any analog front-end, is particularly difficult.

Below the 1V supply, the most widely used design approach is the sub-threshold bias (also known as the weak reverse bias) [3–10]. Inverter-based OTAs represent another viable alternative [11–13]. However, the main disadvantage of operating the digital inverter as an amplifier is the high variation of the dc gain and gain bandwidth (GBW), with temperature and process corners. Moreover, only pseudo-differential operation is achievable.

When input rail-to-rail capability is required, the bulk driving (body driving) technique is an effective solution, even in combination with sub-threshold operation [14–28]. However, when compared to conventional gate-driven circuits, body-driven counterparts exhibit a lower voltage gain due to the reduced value of the bulk transconductance, which accounts for only 10–20% of the gate transconductance [1]. Moreover, if the bulk of NMOS transistors must also be driven, the body-driven approach mandates for a triple-well process. However, since most of the modern CMOS technologies provide such feature, this point is not a real limitation.

To overcome the low gain of bulk-driven OTAs, we exploit in this work local positive feedback to improve first-stage transconductance [26,29–31]. The class AB operation of the second stage is enabled by exploiting the quasi-floating gate approach [32]. Moreover, the

tail bias current of the input gain stage is avoided while maintaining differential operation.

This paper is structured as follows. Section II discusses the circuit operation principle and analytical design equations are carried out. Section III describes the design and simulation of the OTA, while in Section IV the experimental measurements and a comparison with other amplifiers in the literature are reported. Finally, concluding remarks are drawn in Section V.

2. The Proposed Circuit

Figure 1 shows the schematic diagram of the designed amplifier. Where not represented, the transistor bulk terminal is considered to be connected to the corresponding source. The first OTA stage is a bulk-driven non-tailed differential pair M_1-M_2 loaded by the current mirror M_3-M_4 and M_5-M_6. Differential to single-ended conversion is implemented by the additional current mirror M_9-M_{10}. The diode-connected transistor M_{B1} generates the voltage V_{B1} to be applied to the gates of M_1-M_2, thus setting their bias current. It is worth noting that the bulk terminal of M_{B1} is biased through the voltage divider R_1-R_2, which sets the analog ground [26].

Due to the lack of the tail current generator, the couple M_1-M_2 works as a pseudo-differential pair; however, as detailed in [26], the overall OTA input stage exhibits a quasi-differential behavior due to the action of M_7 and M_8 that make voltages at node 1 and 2, as seen in in Figure 1, dependent on the difference of the inverting and noninverting input voltages.

Thanks to the action of the local positive feedback implemented by transistors M_7 and M_8, the equivalent differential transconductance of the first stage is expressed by [26]:

$$G_m = \frac{\beta}{1-\alpha} g_{mb1,2} \tag{1}$$

where

$$\alpha = \frac{(W/L)_7}{(W/L)_3} = \frac{(W/L)_8}{(W/L)_5} \tag{2}$$

$$\beta = \frac{(W/L)_4}{(W/L)_3} = \frac{(W/L)_6}{(W/L)_5}, \tag{3}$$

and $g_{mb1,2}$ is the bulk transconductance of M_1 and M_2 and it is assumed that $(W/L)_9 = (W/L)_{10}$.

From (1), it is apparent that the first-stage transconductance can be boosted by appropriately choosing the aspect ratios α and β from (2) and (3), respectively. In particular, to avoid the magnitude of the positive feedback being higher than one (and, consequently, the amplifier becoming a latch), parameter α must be lower than 1. As a general rule of thumb, it is desirable to set α less than 0.9 to guarantee an adequate margin against process mismatches [31].

The second stage is made up of the common source stage M_{11} and M_{12}. Class AB operation is enabled by adding resistor R_{BATT}, connected between the gate of the load transistor M_{12} and the diode-connected transistor M_{B3}, and capacitor C_{BATT} which adds a path for the signal during dynamic operation [32]. Under quiescent conditions and considering that no DC current flows through R_{BATT}, the voltage at the gate of M_{12} is the same as at the gate of M_{B3}. Consequently, the quiescent current in M_{12} can be precisely set like in a conventional current mirror. During dynamic operation, the voltage at the output of the first stage is subject to a large variation. Capacitor C_{BATT}, which cannot discharge/charge rapidly through R_{BATT}, acts as a floating battery and transfers the voltage changes to the gate of M_{12}, thus providing class AB operation to the second stage.

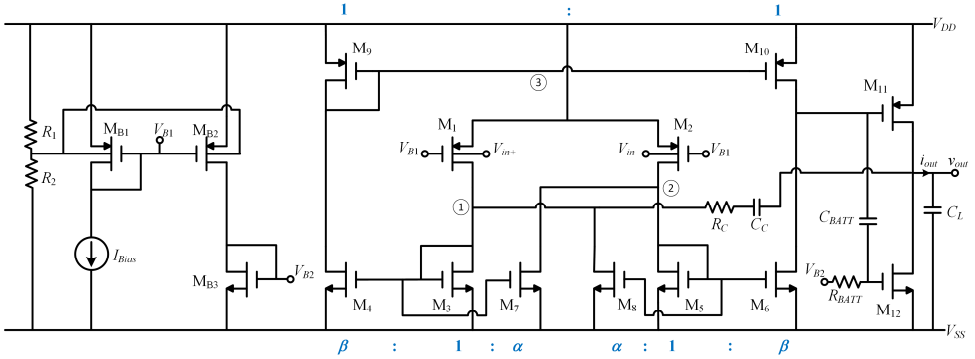

Figure 1. OTA schematic.

The frequency compensation branch is implemented by the conventional Miller capacitor C_C in series with the resistor R_C connected across node 1 and the output node.

Neglecting the parasitic capacitance contribution at nodes 1, 2, and 3 in Figure 1, the open-loop transfer function of the OTA can be approximated as

$$A(s) \approx A_0 \frac{1+\frac{s}{z}}{\left(1+\frac{s}{p_D}\right)\left(1+\frac{s}{p_2}\right)} \tag{4}$$

being $A_0 = G_{mb}\left(g_{m11}+g_{m12}\right)r_{o1}r_{o2}$ the DC gain, with $r_{o1} = r_{d10}//r_{d6}$ and $r_{o2} = r_{d11}//r_{d12}$, and the zero and poles expressed by

$$z = \frac{\alpha+2}{C_C\left(\frac{1}{g_{m3,5}}+2R_C\right)} \tag{5}$$

$$p_D = \frac{1-\alpha^2}{r_{o2}\left(C_L+(1+\alpha)\beta\left(g_{m11}+g_{m12}\right)r_{o1}C_C\right)} \approx \frac{(1-\alpha)}{\beta\left(g_{m11}+g_{m12}\right)r_{o1}r_{o2}C_C} \tag{6}$$

$$p_2 = \frac{C_L+(1+\alpha)\beta\left(g_{m11}+g_{m12}\right)r_{o1}C_C}{C_CC_L\left(\frac{1}{g_{m3,5}}+R_C\right)} \approx \frac{(1+\alpha)\beta\left(g_{m11}+g_{m12}\right)r_{o1}}{C_L\left(\frac{1}{g_{m3,5}}+R_C\right)} \tag{7}$$

where the rightmost approximation in (6) and (7) holds if the following relation is satisfied:

$$C_L \ll (1+\alpha)\beta\left(g_{m11}+g_{m12}\right)r_{o1}C_C \tag{8}$$

It is worth noting that, thanks to the adopted compensation strategy which exploits the embedded current buffer M3-M4-M9-M10, the non-dominant pole p_2 is moved at high frequency by a factor equal to $(1 + \alpha)\beta$◎as compared to a conventional two-stage Miller OTA.

The evaluation of the phase margin (*PM*) yields

$$PM \approx 90° - \tan^{-1}\left(\frac{GBW}{p_2}\right) + \tan^{-1}\left(\frac{GBW}{z}\right) \tag{9}$$

where *GBW* is the gain bandwidth product equal to $g_{mb1,2}/C_C$.

The slew rate (*SR*) of an amplifier is determined by the maximum available charging/discharging currents of capacitors in the circuit. By inspection of Figure 1 and neglecting the effect of parasitic capacitors, the overall *SR* can be expressed as

$$SR \approx \min\left(\frac{I_1}{C_C}, \frac{I_{out}}{C_L}\right) \approx \frac{I_{out}}{C_L} \quad (10)$$

where I_1 is the maximum current provided by M_1 and I_{out} is the charging/discharging current of the class AB output stage. Being $C_C \ll C_L$, the rightmost approximation in (10) holds.

3. Design and Simulation Results

Using a standard 180 nm CMOS process supplied by STMicroelectronics, the amplifier shown in Figure 1 was designed using the transistor dimensions, bias conditions, passive components values, and small-signal parameters reported in Tables 1–3 and assuming a nominal supply voltage equal to 0.6 V. The resistors were implemented using high-resistance polysilicon resistors with a square resistance of 3 kΩ.

Considering the transistor dimensions reported in Table 1, parameters α and β are equal to 0.83 and 15, respectively. Therefore, the bulk transconductance of M_1 and M_2, equal to 3.98 μA/V, is boosted by about 88 times.

Corner simulations and Monte Carlo analysis are executed to assess the robustness of the amplifier over process, temperature, and mismatch variations. The results are reported in Tables 4–6 for three different temperatures (i.e., −10 °C, 27 °C, and 85 °C) for all transistor corners. The results show that the amplifier is stable in all conditions. Furthermore, Monte Carlo simulation results over 1000 runs show a relative standard deviation lower than 25% for all parameters.

Table 1. Transistor dimensions.

Device	Value (μm/μm)
M_{B1}, M_{B2}, M_1, M_2	3/0.26 (×2)
M_{B1}, M_3, M_5	6/0.26
M_4, M_6, M_{12}	6/0.26 (×15)
M_7, M_8	5/0.26
M_9, M_{10}	6/0.26 (×4)
M11	6/0.26 (×8)

Table 2. Component values.

Device	Value
R_1, R_2	300 kΩ
R_{BATT}	1 MΩ
R_C	100 kΩ
C_{BATT}	800 fF
C_C	500 fF
C_L	150 pF
I_{Bias}	180 nA

Table 3. Small-signal parameters.

Param.	Value	Parameter	Value
$g_{m1,2}$	3.98 μA/V	$g_{m9,10}$	31.38 μA/V
$g_{mb1,2}$	1.197 μA/V	g_{m11}	55.97 μA/V
$g_{m3,5}$	2.71 μA/V	g_{m12}	62.89 μA/V
$g_{m4,6}$	36.04 μA/V	r_{o1}	1.03 MΩ
$g_{m7,8}$	1.848 μA/V	r_{o2}	764 kΩ

Table 4. Corner and Monte Carlo (1000 iterations) analysis results for T = −10 °C.

Param.	TT	SS	SF	FS	FF	MC	
						μ	σ
Power (μW)	3.29	3.11	3.19	3.31	3.44	3.27	0.24
DC Gain (dB)	64.8	59.6	67	56.7	67.1	67.4	0.8
GBW (kHz)	357	313.7	349.6	302.3	370.1	481.8	34.6
Phase Margin (deg)	67.6	67.5	67	69.6	68.8	67.6	2.1
Pos. Slew Rate (V/μs)	0.17	0.09	0.34	0.08	0.3	0.17	0.04
Neg. Slew Rate (V/μs)	6.61	5.98	5.47	6.7	6.62	6.58	0.57
V_{OS} (μV)	18.6	–7	56.6	–108.5	30.3	–78.1	$13.5 \cdot 10^{-3}$

Table 5. Corner and Monte Carlo (1000 iterations) analysis results for T = 27 °C.

Param.	TT	SS	SF	FS	FF	MC	
						μ	Σ
Power (μW)	3.71	3.56	3.64	3.36	3.86	3.69	0.28
DC Gain (dB)	67.4	65.7	68.5	64.2	68.1	67.2	0.5
GBW (kHz)	341.6	333.1	332.9	337.2	343.6	471.9	24.2
Phase Margin (deg)	66.6	65.4	66.3	67.1	68	66.5	1.8
Pos. Slew Rate (V/μs)	0.31	0.18	0.54	0.15	0.49	0.32	0.06
Neg. Slew Rate (V/μs)	4.6	4.72	3.92	4.99	4.35	4.58	0.37
V_{OS} (μV)	53.8	50.6	67.8	37.2	58.8	–30.5	$13.4 \cdot 10^{-3}$

Table 6. Corner and Monte Carlo (1000 iterations) analysis results for T = 85 °C.

Param.	TT	SS	SF	FS	FF	MC	
						μ	Σ
Power (μW)	4.22	4.17	4.22	4.24	4.23	3.91	0.21
DC Gain (dB)	68.1	68	68.4	67.2	68	66.4	0.4
GBW (kHz)	304.3	304.6	295.9	310.3	303	423.7	18.1
Phase Margin (deg)	65.4	64	65.3	65.7	66.8	65.4	1.5
Pos. Slew Rate (V/μs)	0.57	0.39	0.88	0.35	0.84	0.58	0.08
Neg. Slew Rate (V/μs)	2.15	2.42	1.55	2.71	1.86	2.15	0.22
V_{OS} (μV)	95.2	89	107.7	86	105	16.9	$13.4 \cdot 10^{-3}$

Figure 2 shows the simulated input referred noise versus frequency. The white noise level is equal to 1.3 μV/√Hz.

Figure 3 shows the magnitude of the power supply rejection ratio (PSRR) and the common mode rejection ratio (CMRR) versus frequency.

Figure 4 depicts the DC transfer characteristic of the amplifier in unity-gain configuration, showing a rail-to-rail input common mode range (*ICMR*). In the same figure, it can be also noted that the input current is lower than 13 nA.

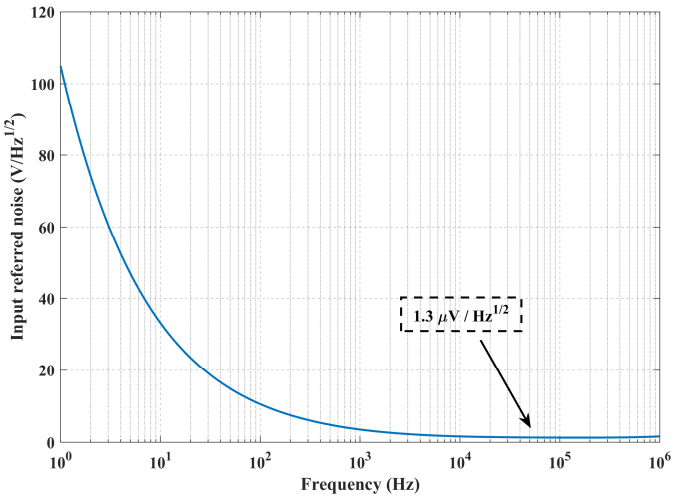

Figure 2. Input referred noise versus frequency.

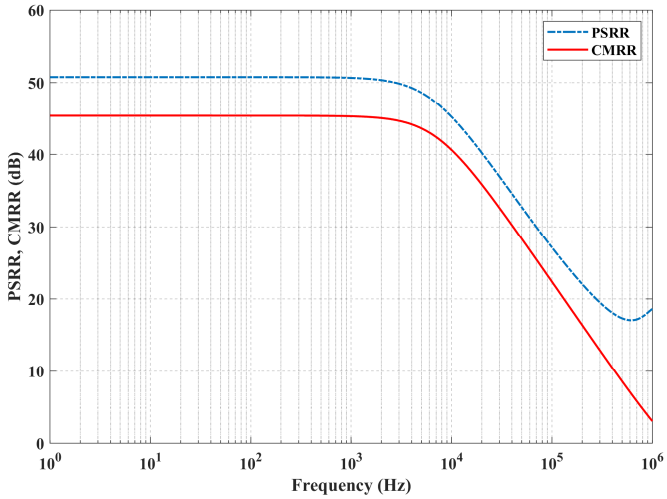

Figure 3. Magnitude of PSRR and CMRR versus frequency.

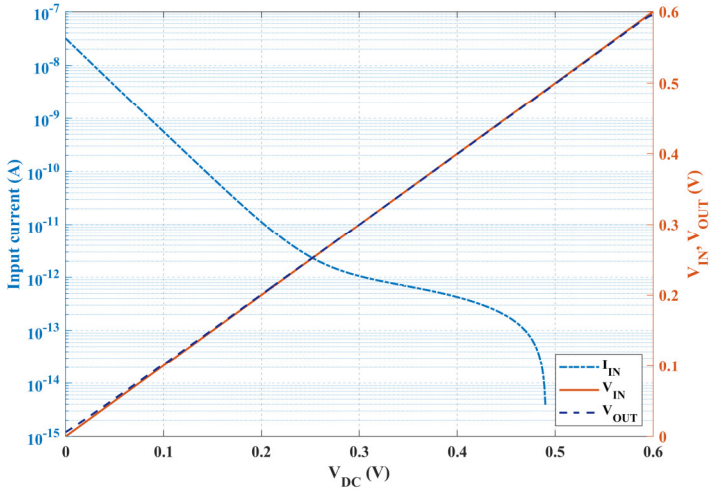

Figure 4. DC transfer characteristics in unity-gain configuration.

4. Measurement Results and Comparison

The OTA in Figure 1 has been fabricated and experimentally tested. The layout and the chip microphotograph of the circuit are shown in Figure 5. The occupied area is 1329 m^2.

The circuit has been characterized at a 0.6 V supply and a 150 pF capacitive load. Figure 6 reports the measured Bode plot in open-loop configuration, showing a *GBW* equal to 350 kHz and a *PM* equal to 69°. The transient response to a 100 mV_{pp} input step, with the OTA in unity gain, is shown in Figure 7.

Table 6 summarizes the OTA main performance parameters and a comparison with other sub-1 V amplifiers taken form the literature. To evaluate the performance trade-off between bandwidth, load capacitance, slew rate (*SR*), and total bias quiescent, I_T, we use in Table 6, the following conventional figures of merit:

$$IFOM_S = \frac{GBW}{I_T} C_L \tag{11a}$$

$$IFOM_L = \frac{SR}{I_T} C_L \cdot \tag{11b}$$

Among the considered solutions, only the single-stage in [26] exhibits a higher value of $IFOM_S$ but with a DC gain equal to 38 dB only. As compared to the remaining solutions, the increase in (11a) is equal to about 3.45. The proposed topology shows an increase in $IFOM_L$ equal to 4.36× against all the other solutions.

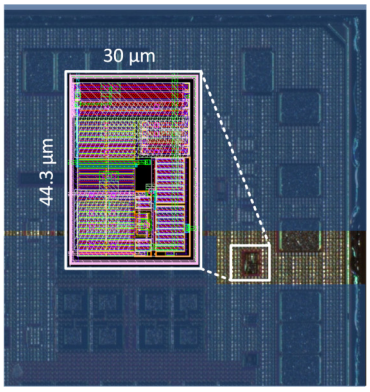

Figure 5. Chip microphotograph and layout of the amplifier.

Figure 6. Measured open-loop Bode plot.

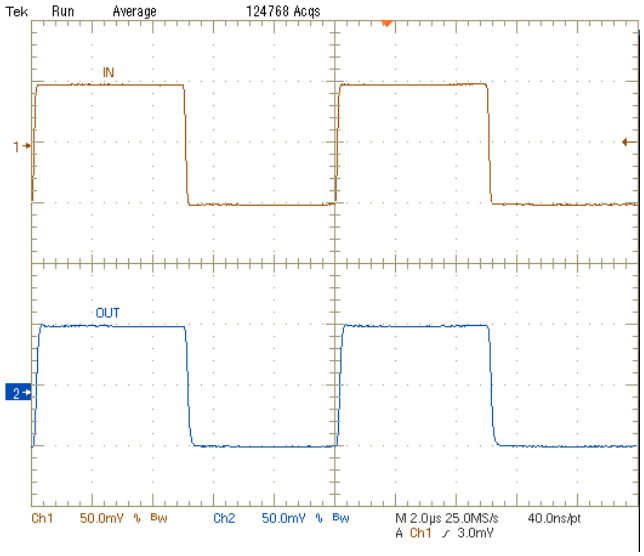

Figure 7. Measured unity-gain step response.

Two other traditional figures of merit, which take into account the silicon area, are included in Table 7:

$$IFOM_{AS} = \frac{\omega_{GBW}}{Area \cdot I_T} C_L \tag{12a}$$

$$IFOM_{AL} = \frac{SR}{Area \cdot I_T} C_L . \tag{12b}$$

Additionally, in this case the proposed solution outperforms the other amplifiers, except for the $IFOM_{AS}$ of [26]. It is worth noting, however, that the tail-less structure does not offer a CMRR and PSRR as high as tailed ones, but the values are still acceptable and comparable with other solutions.

Table 7. Comparison with others Sub-1 V experimentally tested OTAs.

Ref.	**[5]**	**[16]**	**[15]**	**[6]**	**[18]**	**[7]**	**[19]**	**[9]**	**[20]**	**[21]**	**[22]**	**[23]**	**[24]**	**[26]**	**[28]**	**[27]**	**This Work**
Year	2005	2007	2007	2012	2013	2014	2015	2016	2016	2018	2020	2020	2020	2022	2022	2023	2023
Technology (μm)	0.18	0.35	0.35	0.18	0.35	0.18	0.065	0.18	0.18	0.18	0.18	0.18	0.065	0.18	0.18	0.13	0.18
Area (mm^2)	17	0.06	0.0532	0.057	0.1575	0.057	0.00495	0.036	0.0198	0.0082	0.0085	0.0098	0.002	$8.66 \cdot 10^{-4}$	$7.9 \cdot 10^{-3}$	$2.34 \cdot 10^{-3}$	$1.33 \cdot 10^{-3}$
Supply (V)	0.5	0.6	1	0.8	1	0.5	0.5	0.5	0.7	0.3	0.3	0.3	0.25	0.4	0.4	0.3	0.6
C_L (pF)	20	15	17	8	15	30	3	40	20	20	30	30	15	150	30	35	150
DC gain (dB)	62	69	76.2	51	88	70	46	77	57	63	65	98.1	70	38	60	87	67
I_{bias} (μA)	150	0.9	358	1.5	197	0.15	366	0.14	36	0.056	0.042	0.04333	0.10400	0.08135	0.0096	0.01019	6.17
Power (μW)	75	0.54	358	1.2	197	0.075	183	0.07	25.2	0.0168	0.0126	0.013	0.026	0.03254	0.024	0.03373	3.70
GBW (MHz)	10	0.011	8.1	0.057	11.67	0.018	38	0.004	3	0.0028	0.00296	0.0031	0.0095	0.00556	0.007	0.0103	0.3503
PM (°)	60	65		60	66	55	57	56	60	61	52	54	88	79	60	58	69
SR (V/μs) [a]	2	0.015	3.88	0.14	1.95	0.003	43	0.002	2.8	0.0071	0.00415	0.0091	0.002	0.0074	0.079	0.00374	2.45
CMRR (dB)	65	74.5	70.5	65	40	--	35	55	19	72	110	60	62.5	36	85	58	45.4
PSRR (dB)	43	--	45	--	40	--	37	52	52	62	56	61	38	30	76	47	50.8
Op. mode [b]	GD	BD	BD	GD	BD	GD	BD	GD	BD	BD	BD	BD	BD	BD	BD	BD	BD
Stage #	2	2	1	1	2	2	3	2	3	2	2	3	3	1	2	3	2
$IFOM_S$ (MHz·pF/μA)	1.33	0.18	0.38	0.30	0.89	3.60	0.31	1.14	1.67	1.00	2.11	2.15	1.37	10.25	3.50	3.21	7.42
$IFOM_L$ ((V/μs)·pF/μA)	0.27	0.25	0.18	0.75	0.15	0.60	0.35	0.57	1.56	2.54	2.96	6.30	0.29	13.64	39.50	1.16	59.56
$IFOM_{AS}$ (MHz·pF/μA·mm^2)	78.43	3.06	7.23	5.33	5.64	63.16	62.92	31.75	84.18	121.95	248.74	219.00	685.10	11838.33	443.04	1372.89	5584.80
$IFOM_{AL}$ ((V/μs)·pF/μA·mm^2)	15.69	4.17	3.46	13.10	0.94	10.53	71.20	15.87	78.56	309.23	348.74	642.86	144.23	15745.41	5000.00	497.54	44817.46

[a] average value; [b] GD: gate drive, BD: bulk driven.

5. Conclusions

In this paper, a two-stage OTA exploiting local positive feedback, a non-tailed differential pair, and a class AB second stage are discussed, analyzed, and experimentally tested. A comparison with the state-of-the-art reveals that the proposed solution is suitable for area-constrained low-voltage low-power applications such as battery-less IoT nodes.

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