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FPGA-Based Decision Support System for ECG Analysis

Agostino Giorgio, Cataldo Guaragnella and Maria Rizzi *

Dipartimento di Ingegneria Elettrica e dell'Informazione, Politecnico di Bari, via E. Orabona 4, 70125 Bari, Italy
* Correspondence: maria.rizzi@poliba.it

Abstract: The high mortality rate associated with cardiac abnormalities highlights the need of accurately detecting heart disorders in the early stage so to avoid severe health consequence for patients. Health trackers have become popular in the form of wearable devices. They are aimed to perform cardiac monitoring outside of medical clinics during peoples' daily lives. Our paper proposes a new diagnostic algorithm and its implementation adopting a FPGA-based design. The conceived system automatically detects the most common arrhythmias and is also able to evaluate QT-segment lengthening and pulmonary embolism risk often caused by myocarditis. Debug and simulations have been carried out firstly in Matlab environment and then in Quartus IDE by Intel. The hardware implementation of the embedded system and the test for the functional accuracy verification have been performed adopting the DE1_SoC development board by Terasic, which is equipped with the Cyclone V 5CSEMA5F31C6 FPGA by Intel. Properly modified real ECG signals corrupted by a mixture of muscle noise, electrode movement artifacts, and baseline wander are used as a test bench. A value of 99.20% accuracy is achieved by taking into account 0.02 mV for the root mean square value of noise voltage. The implemented low-power circuit is suitable as a wearable decision support device.

Keywords: FPGA; embedded systems; digital signal processing; Matlab; decision support systems (DSS); ECG; arrhythmia; pulmonary embolism risk; QT-segment lengthening; computer-aided detection (CAD)

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1. Introduction

The most recent practice in the design of miniaturized circuits and systems for digital signal processing purposes is strongly oriented towards the use of programmable logic devices (PLD) and embedded systems designed using field-programmable gate arrays (FPGAs). FPGA circuits are preferred because of their specific purpose circuits, low-cost, reconfigurable characteristics, architectural flexibility, and fast time of development when new functionalities are added. Compared with a standard microcontroller, FPGAs have the capability of parallel and/or pipelined execution of multiple tasks and thus they minimize power consumption by using a slower system clock [1].

A great deal of FPGA-based wearable devices for the capture and analysis of bio-signals are available on the market according to recent trends in health-monitoring devices [2,3]. The study of bio-signals allows us to control and assess the functionality of the organ that generated it. For instance, the shape of the electrocardiogram signal (ECG) is considered by cardiologists to be representative of cardiac physiology. Diagnosis of heart conditions by means of ECG is the basic procedure to prevent and control cardiovascular pathologies, which are the main cause of death worldwide [4,5].

ECG tracing of each heartbeat is characterized by three signal features, which are one P-wave representing the atrial depolarization process, one QRS complex linked to the ventricular depolarization process, and one T-wave related to the ventricular repolarization. A normal cardiac cycle is featured by the sequence of P-wave, QRS complex, and T-wave interspersed with sections known as segments (Figure 1) [6,7]. Damage to the heart or

nerves can produce alterations to the heart's electrical activity, which corresponds to changes in ECG signal shape.

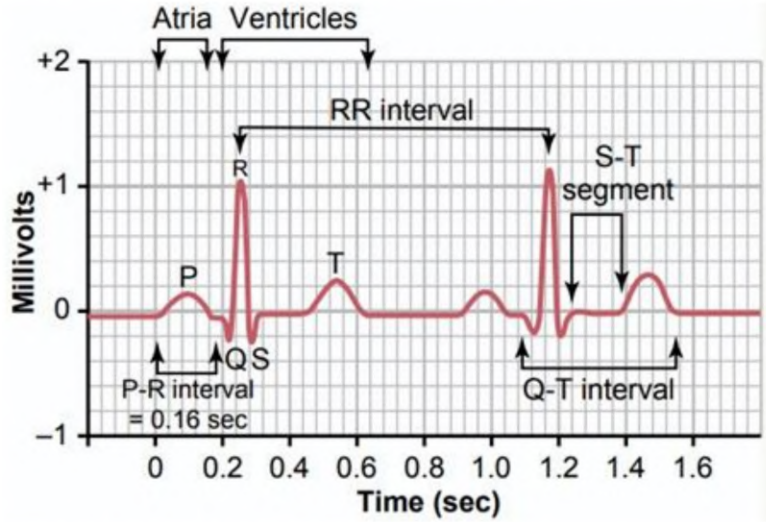


Figure 1. ECG typical waveform [7].

QRS complexes and related R peaks are the most used parameters for a basic evaluation of the health status of the heart. In fact, heart rate and other parameters can be evaluated to prevent the onset of some diseases, such as ischemia, after the QRS identification [8]. The analysis of RR-interval lengths (that is the time between two consecutive R peaks) makes the heart-rate variability (HRV) study possible. HRV measurement provides significant information regarding cardiac irregularities or injuries. The activity of the autonomous nervous system is also depicted by the HRV analysis, and it is used as a quantitative indicator of stress [9,10].

Cardiac arrhythmia is a common heart disease that could be defined as a disorder or an abnormality in the normal activation sequence of the myocardium, giving rise to an irregular heartbeat or abnormal rhythm [11]. Arrhythmia can take place in a healthy heart with minimal consequences; however, it may also indicate a serious problem, which can lead to stroke, sudden cardiac death, scarring of heart tissue, changes in heart structure, or premature beats due to blood flow failure in the body [12]. Analysis of RR intervals can be used to determine the heart rhythm because an abnormal heart rhythm causes characteristic variations in RR-interval lengths.

The Association for the Advancement of Medical Instrumentation (AAMI) recommendations indicate five more general classes of arrhythmia, although various classes of arrhythmia characterized by distinctive manifestations are indicated in the literature [13–18]. These classes are normal sinus rhythm (N), ventricular ectopic beats (V), supraventricular ectopic beats (S), fusion beats (F), and unclassified beats (Q) [19,20]. Bradycardia, tachycardia, atrial fibrillation, and ventricular tachycardia are the main heart rhythm disturbances. In case of regular hearth rhythm, bradycardia and tachycardia occur if the hearth rate is below 40–50 beats per minute (bpm) and above 120–140 bpm, respectively. Examples of heart rhythm conditions are shown in Figure 2 [21]. Although a great deal of research in the literature have focused on R-peak detection and RR-interval length evaluation to asses cardiac disorders [22–24], the lengthening of the QT interval has gained high significance as an arrhythmia risk predictor [25,26], and the prolongation of RS time has been considered both a useful index for diagnosing acute pulmonary embolism and a predictive index for short-term mortality in patients with acute pulmonary embolism [27,28].

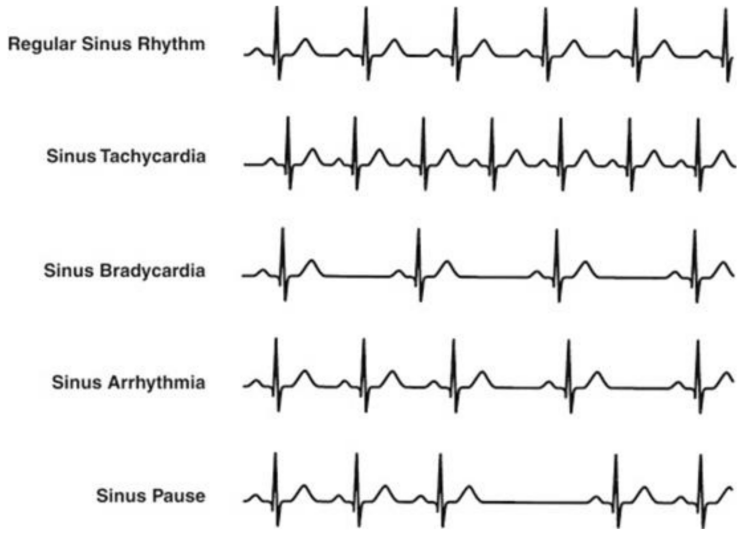


Figure 2. Main heart rhythm conditions [21].

Analysis of ECG patterns by physicians may have to be carried out over several hours, with a high probability of missing vital information owing to the unpredictability of arrhythmia onset. The adoption of a computer-aided diagnosis (CAD) system that implements an automatic signal processing classification procedure is advisable [29,30]. These decision support systems typically operate as automated "second opinion" systems that can indicate the onset of disturbances and/or type of abnormalities [31]. Technological innovation in CAD systems is not just limited to the development of software classification methods but involves the hardware implementation of real-time solutions [32–34].

In this paper, we design a real-time and low-power architecture for the diagnosis of the health status of the heart. We have developed an accurate software-based medical diagnostic approach able to detect the most common types of arrhythmias to refer the HRV with the related pathologies and to perform other unique tasks, such as an evaluation of the QT-segment lengthening and pulmonary embolism (PE) risk assessment. The conceived algorithm is optimized for real-time application and is implemented in the Matlab® environment. To provide a continuous monitoring of cardiac activity, we have also designed a hardware implementation of the aforementioned system based on an FPGA device. In summary, the main contributions of our paper are:

- The development of an automatic classifier, which should be suitable as a decision support system;
- The soft real-time implementation of the classifier on FPGA for a low-cost/low-power device;
- The evaluation of CAD (software) and hardware performance;
- Comparative benchmarking for assessing the method validity

The rest of the paper is organized as follows: In Section 2 of our paper, the conceived procedure is described, while Section 3 deals with the design of the FPGA-based embedded system. The functional test carried out, discussions, conclusions, and future developments complete the paper.

2. Implemented Diagnostic Procedure

The aim of the implemented tool is the development of a framework able to detect the occurrence of:

- Arrhythmias;
- Tachycardia;
- Bradycardia;
- Arrhythmias in presence of tachycardia;
- Arrhythmias in presence of bradycardia;

- Irregular heartbeat, followed by tachycardia/bradycardia, succeeded by normal cardiac rhythm;
- Pulmonary embolism risk;
- Variations (lengthening) of the QT segment.

The sequential pipeline of our decision support system is detailed below.

2.1. Preprocessing Phase

The aim of the signal preprocessing phase is baseband filtering and noise level reduction.

Baseline alignment by means of the Daubechies-6 wavelet transform was performed and then a tenth-order bandpass FIR filter with cutoff frequencies at 0.2 and 40 Hz was used. Wavelet transform was adopted for signal denoising because it has been shown to be an appropriate technique for the study of non-stationary signals [35]. The wavelet of orthogonal families was considered so as to ensure the absence of information redundancy represented by wavelet coefficients [36]. Coiflet5 wavelet was selected and three decomposition levels were used after validation procedure tests.

2.2. Segmentation

This phase performed the localization of the P, Q, R, S, and T points on each heartbeat of the ECG signal under test. Our procedure is designed to be used both for real-time applications and for FPGA implementation. The developed tool focuses on the width of the ECG signal for the detection of characteristic points. Some other QRS wave parameters were not considered, such as slope and duration. As a result, we avoided the introduction of high frequency noise components and the need for a large amount of RAM memory.

R points were firstly localized by setting an adequate threshold value. The following formula was adopted for the threshold value (U_{TH}) setting according to [37]:

$$U_{TH} = \frac{A}{2} + \frac{N}{A} \ln\left(\frac{P_0}{P_1}\right) \quad (1)$$

in which P_1 and P_0 are the probability of having and not having a QRS complex, respectively, A is the amplitude of the signal, and N represents the noise variance. A threshold value approximately equal to 70% of the maximum signal amplitude is obtained assuming characteristic figures compliant with the AAMI standard for the ECG signal (such as a typical pulse of 72 bmp, a QRS wave duration of 180 ms, and a noise power of 0.04 W) [37].

The preprocessed ECG signal is fed into a switch block whose output is 0 if the signal width is below the evaluated threshold value, otherwise it is equal to the input (Figure 3).

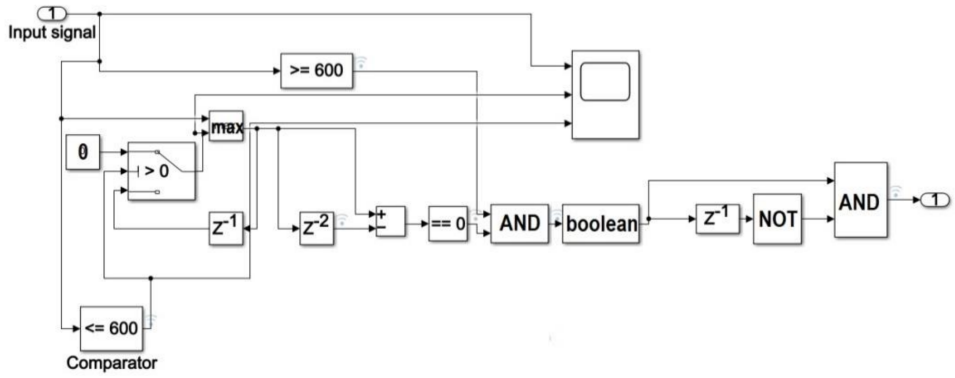


Figure 3. Block diagram of the procedure for R peak localization in Simulink environment.

The waveform of the output signal from the processing section composed of comparator–switch–delay is indicated in Figure 4. The section output is a replica of the input if the signal is above the selected threshold value, and it is an increasing function with time. The output retains the last increasing value as soon as the input signal decreases.

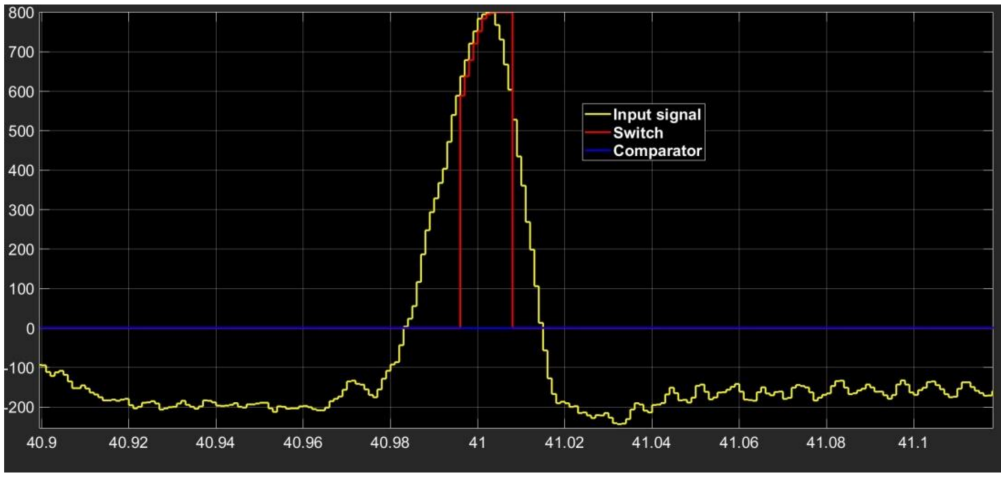


Figure 4. Waveform shape of input signal (yellow signal) and of outputs from comparator (blue signal) and switch (red signal).

A maximum search section is then implemented using both a MAX block, which processes two samples at once, and a block which produces a delay of two samples. Assuming a non-constant signal, a maximum value occurs when the outputs of the aforementioned blocks are equal, that is when the output from the subtractor block is zero (Figure 3). Denoting with x_i and x_{i+1} two generic input samples of the MAX block occurring at time t_i e t_{i+1}, respectively (with $1 \leq i \leq s-1$ and s equal to the number of samples in a single heart-beat), the detected R peak is located in correspondence of sample x_i if the output of the subtractor is equal to zero at time t_{i+1}.

The last section of our algorithm is conceived to produce a pulse in correspondence of every time at which an R peak is located. In Figure 5 the pulsed ECG signal is shown.

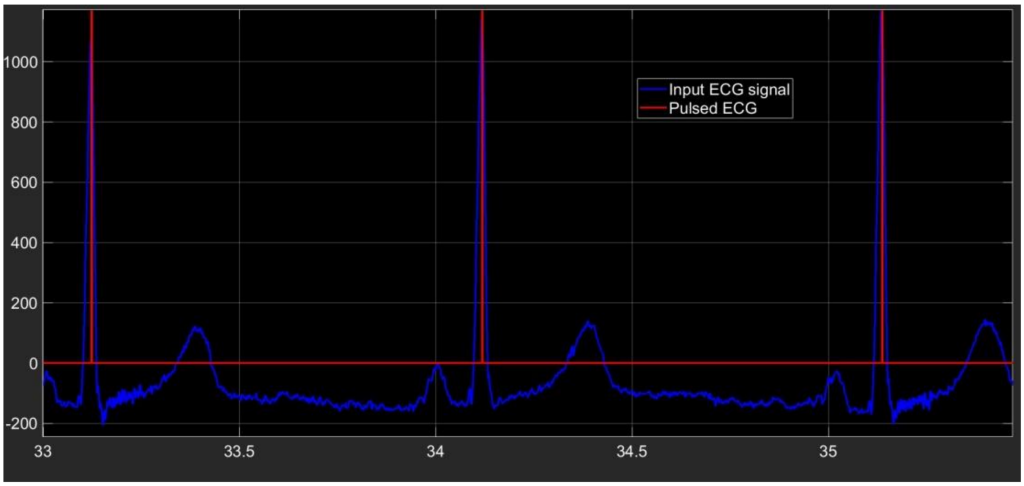


Figure 5. Pulsed ECG signal (red signal) and database ECG signal (light-blue signal).

Our procedure looks for the other ECG characteristic points for each cardiac cycle after all the R peaks have been localized. The generic i^{th} cardiac cycle is considered, which corresponds to the part of the ECG signal between the i^{th} R and the $(I + 1)^{th}$ R peaks. Our procedure detects:

✓ The S-wave by examining the ECG signal ranged between the i^{th} R point and the middle of the i^{th} cardiac cycle, looking for the minimum point. The following pseudo-code is used:
for ii = 1:(length(peakRLocend)−1)

[peakSMagend(ii)peakSLocend(ii)] = min ecg(peakRLocend(ii):(peakRLocend(ii) + (peakR-Locend(ii + 1)-peakRLocend(ii)))/2)));
peakSLocend(ii) = peakRLocend(ii) + peakSLocend(ii);
end

- ✓ The T-wave by considering the ECG signal ranged between the i^{th} S point and the middle of the i^{th} cardiac cycle, looking for the maximum point. The following pseudo-code is used:
for ii = 1:(length(peakRLocend)−1)
[peakTMagend(ii)peakTLocend(ii)] = max (ecg(peakSLocend(ii):(peakRLocend(ii) + (peakR-Locend(ii + 1)-peakRLocend(ii)))/2)));
peakTLocend(ii) = peakSLocend(ii) + peakTLocend(ii);
end
- ✓ The Q-wave by taking into account the portion of the ECG within the middle of the i^{th} cardiac cycle and the $(i + 1)^{th}$ R peak according to the following pseudo-code
for ii = 1:(length(peakRLocend)−1)
[peakQMagend(ii)peakQLocend(ii)] = min (ecg((peakRLocend(ii) + (peakRLocend(ii + 1)-peakRLocend(ii)))/2):(peakRLocend(ii + 1))));
peakQLocend(ii) = peakRLocend(ii) + (peakRLocend(ii + 1)-peakRLocend(ii)))/2 + peakQLocend(ii);
end
- ✓ The P-wave by seeking the maximum point in the ECG part ranged between the middle of the i^{th} cardiac cycle and the Q-wave belonging to the i^{th} cardiac cycle. The following pseudo-code is used:
for ii = 1:length(peakQLocend)
*a = round((peakRLocend(ii + 1)-peakRLocend(ii))*2/3);*
[peakPMagend(ii)peakPLocend(ii)] = max (ecg((peakRLocend(ii) + a):(peakQLocend(ii))));
peakPLocend(ii) = peakRLocend(ii) + a+peakPLocend(ii);
end

Characteristic points detected by the implemented tool are highlighted in Figure 6.

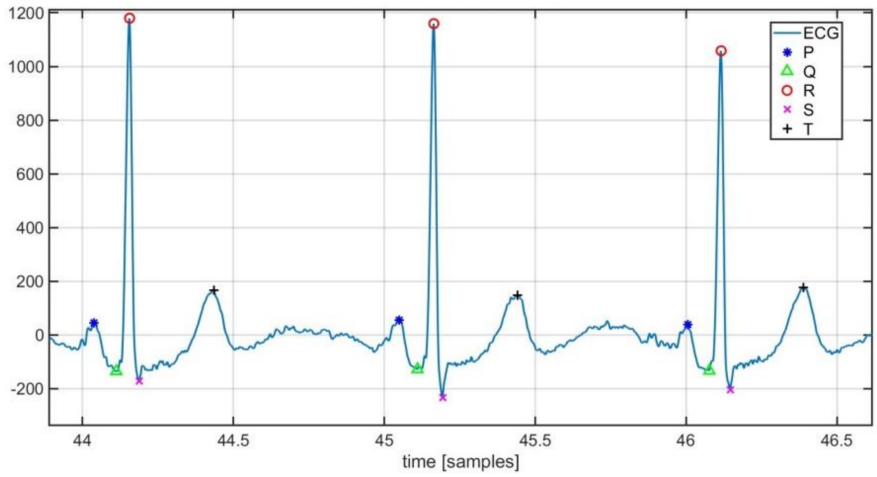


Figure 6. Localization of ECG characteristic points.

2.3. Classification Phase

The pulsed ECG signal was analyzed for assessing the health status of the heart and the diagnosis of cardiac diseases. Three pulses at a time were analyzed to make the procedure particularly suitable for real-time analysis and easily deployed by FPGA devices. A time window three pulses long was defined for the classification process. Denoting with p^j_i the generic i^{th} pulse of the j^{th} time window and with n the number of detected R peaks, the j^{th} time window is composed of p^j_{i-1}, p^j_i and p^j_{i+1} pulses ($2 \leq i \leq n-1$, for $1 \leq j \leq n-2$).

The time window was shifted one pulse right for the analysis of the whole pulsed ECG. Therefore, it follows that the time window always consists of three pulses. Our procedure evaluated the time difference between p^j_i and p^j_{i-1} ($d^j_{pi-1,pi}$), between p^j_i and p^j_{i+1} ($d^j_{pi,pi+1}$), and between p^j_{i-1} and p^j_{i+1} ($d^j_{pi-1,pi+1}$) for each time window (that is for $1 \leq j \leq n-2$).

According to the most widespread medical practice, a diagnosis of cardiac arrhythmia is suggested by the implemented procedure if [38]:

$$d^j_{pi-1,pi} < 0.4\, d^j_{pi-1,pi+1} \tag{2}$$

Moreover, the p^j_i pulse is also classified as tachycardic or bradycardic if $d^j_{pi-1,pi}$ or $d^j_{pi,pi+1}$ is above 140 bpm or below 40 bpm, respectively.

Pulmonary embolism risk assessment is possible by evaluating the RS distance for each heartbeat. Additionally, average HR, HRV, and QT intervals are measured after the analyzing process of the whole ECG is finished. The following expressions are used [12,39]:

$$HR = \frac{60}{\frac{1}{n}\sum_{i=1}^{n} d_{pi,pi+1}} \tag{3}$$

$$HRV = HRmax - HRmin \tag{4}$$

$$QTc_i = \frac{QT_i}{\sqrt{d_{pi,\ pi+1}}}\ 1 \leq i \leq n-1 \tag{5}$$

where QT_c, known as corrected QT, takes into account the QT dependence on heart rate, sex, and time of the day.

In Figures 7 and 8 the operating procedure of the classification phase is better detailed. These figures show the results in ModelSim, which is an environment for the simulation of hardware description languages in Quartus. As soon as the first QRS complex is locked, a time window with a duration equal to three pulses (triplet) is defined, onto which a reference clock signal is superimposed (Figure 7). After the first triplet has been analyzed, the system automatically moves to the second one (Figure 8) and so on in a way that any arrhythmias are detected.

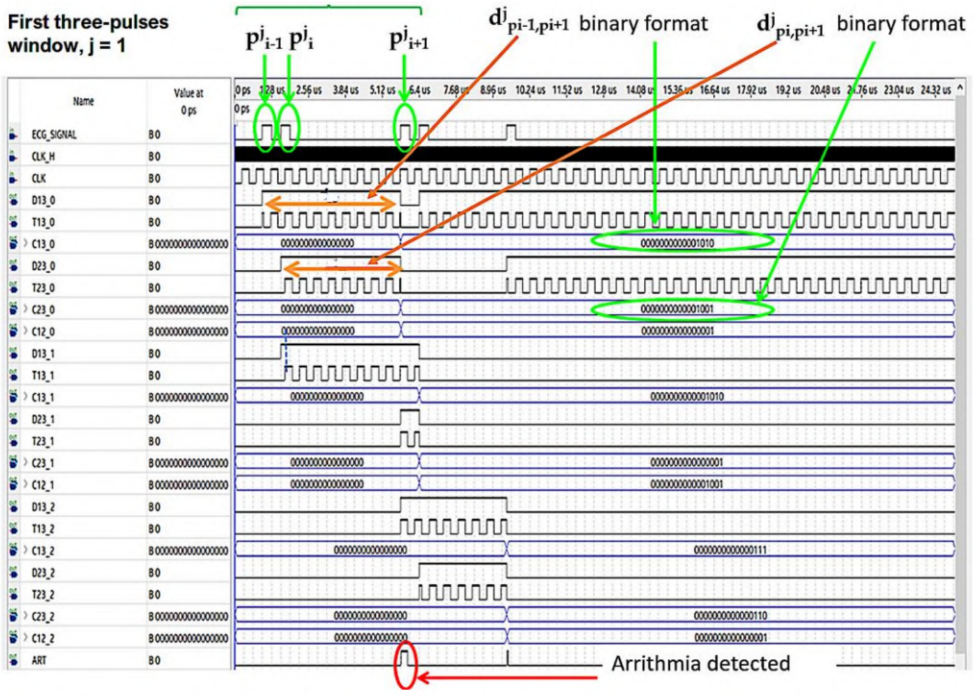


Figure 7. Analysis of the first time window during the classification phase.

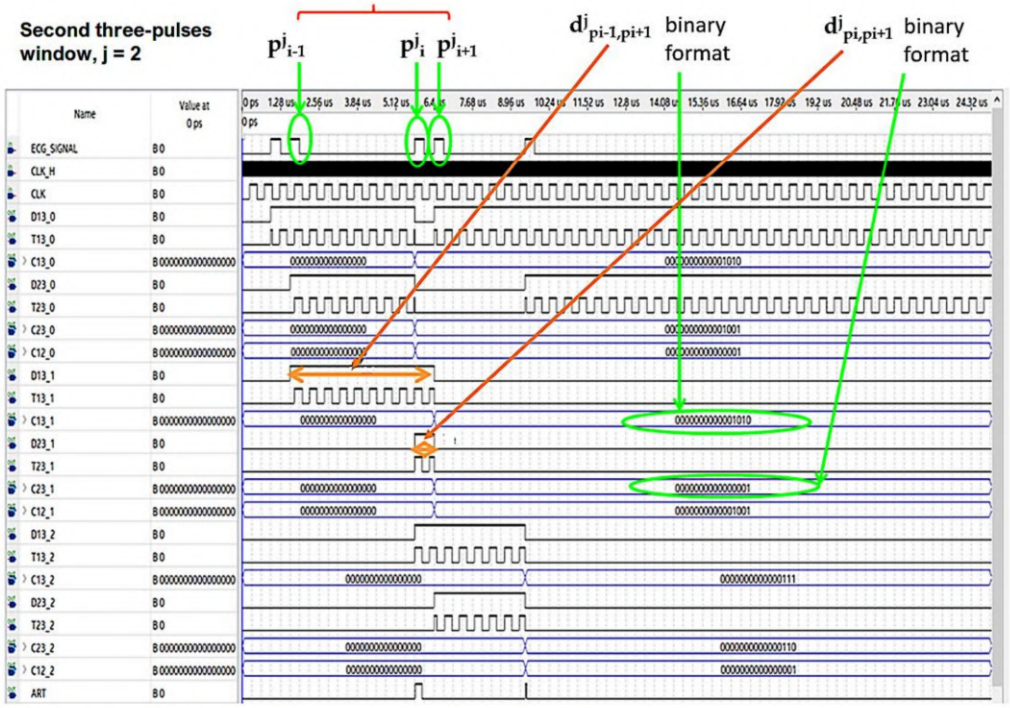


Figure 8. Analysis of the second time window during the classification phase.

2.4. Adopted Database

Real signals and properly modified real signals were used as our system test bench. Real signals were retrieved from the PTB diagnostic ECG database, which is provided by the National Metrology Institute of Germany, named Physikalisch-Technische Bundesanstalt (PTB). The collection of the ECG signals was obtained using a non-commercial, PTB prototype recorder, and they are from healthy volunteers and patients with different heart diseases. Each record includes 15 simultaneously measured signals, which are the conventional 12 leads together with the 3 Frank leads. The ECGs are characterized by a 1 kHz sample rate, 16-bit resolution with 0.5 microvolts/LSB, and last about 2 min [40,41]. In the ECG signal header, a detailed clinical summary is provided, which includes age, gender, diagnosis, etc.

Properly modified real signals were generated by using the model recently provided for free by Physionet [42]. This software enables the generation of datasets containing realistic simulated ECG and PPG signals with arrhythmia episodes and, consequently, simplifies the development and testing of arrhythmia detectors. ECG signals with atrial fibrillation, extreme bradycardia, and ventricular tachycardia were generated. The simulator makes it possible to control the properties of generated signals, such as the number of arrhythmic beats, the amount and amplitude of noise, and artifacts. Such flexibility allows a comprehensive investigation of arrhythmia detectors under different circumstances.

For testing the implemented DSS, the first 70 records of the PTB database and the properly modified real ECG signals in [43] were considered.

3. Hardware Architecture of the FPGA-Based Embedded System

The aim of this design was a compact hardware implementation suitable for wearable devices. A solution characterized by low power consumption and minimum hardware resource requirements was conceived.

Preprocessing filters and our R-peak detection algorithm were translated into HDL language by using the HDL Coder tool. This Matlab tool makes the custom block-wise design easier. A code optimized to run in FPGA devices was generated [44,45].

Fixed-point arithmetic was adopted for signal processing. The implemented procedure operates thus in real time without requiring an excessive power computing. The amplitude of the pulse-transformed ECG signal was converted to a 16-bit fixed-point format.

The block diagram of our diagnostic device is indicated in Figure 9. It is composed of three functional modules: the ROM block, the analyzer block, and the MCU block. The input of the system is the vector of ECG data and the outputs are the number of QRS waves detected, the number of bradycardic heartbeats, the number of tachycardic heartbeats, and the number of arrhythmias detected. Diagnoses relating to the PE and QT were analyzed by the MCU block and can be notified by a message on the display or by flashing LEDs.

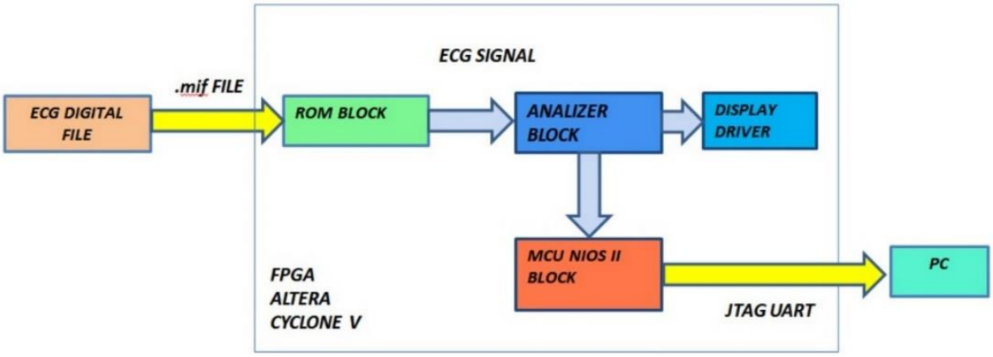


Figure 9. Functional block diagram of the designed hardware.

3.1. ROM Module

This block stores the pulse-transformed ECG (Figure 10). In particular, a string of 16 bits set to 1 represents the detection of an R peak, while a string of 16 bits set to 0 indicates the R peak absence. For debug purposes, the ROM block is not necessary because the designed hardware processes the real-time ECG signal.

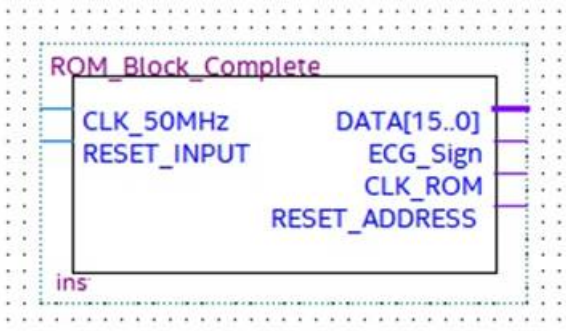


Figure 10. ROM block with input and output signals.

The two inputs of the ROM module, named CLK_50 MHz and Reset_Input, are the operating clock provided by the selected development board and the input for the ROM address reset, respectively. The four outputs are:

- DATA [15 . . . 0], which is a 16-bit word pointed to by the address counter, which tests and checks the block operations;
- ECG_Signal, which is the pulsed transformed ECG signal under test;
- CLK_ROM, which is the timing signal of the ROM address counter;
- Reset_Address, which is the reset signal generated after the whole ROM has analyzed, which stops the process.

The ROM unit consists of the below modules/circuits, which perform the following functions (Figures 11 and 12):

- Address Generator: generates both the clock signal to accurately reproduce the ECG signal acquisition frequency and the 16-bit address for driving the ROM memory bank. The number of bits composing the address is equal to the bits forming the binary representation of the ECG sample amplitude;
- AND Reset: generates a reset signal as soon as the Address Generator counter has reached the binary value 1111111111111111. In such a situation, the analysis can be stopped because the ROM has been completely read and the whole signal has been processed;
- OR_16Bit: makes the logical sum on each of the 16-bit words stored into the ROM. According to the Boolean algebra, OR gate output is set at logical value 1 if at least one input is equal to 1, while a 0 output happens if all inputs are set at logical value 0. A logic 1 output occurs when a pulse (R peak) is recorded into the ROM block (being the OR inputs equal to 1111111111111111), and a logic 0 output takes place when no R peak is stored in the ROM (since the OR inputs are 0000000000000000). The analysis is so restricted to a single bit, which is the OR output instead of 16 bits, because only the moment at which the pulse occurs is relevant for diagnosis purpose. Pulse amplitude has no diagnostic relevance in this instance.

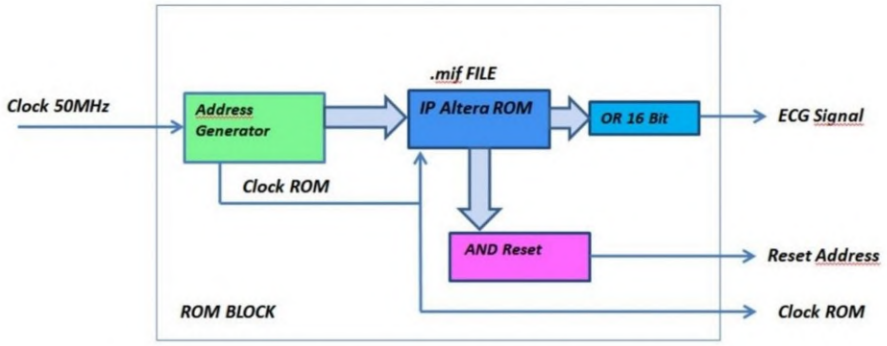


Figure 11. Functional and logical diagram of the ROM module.

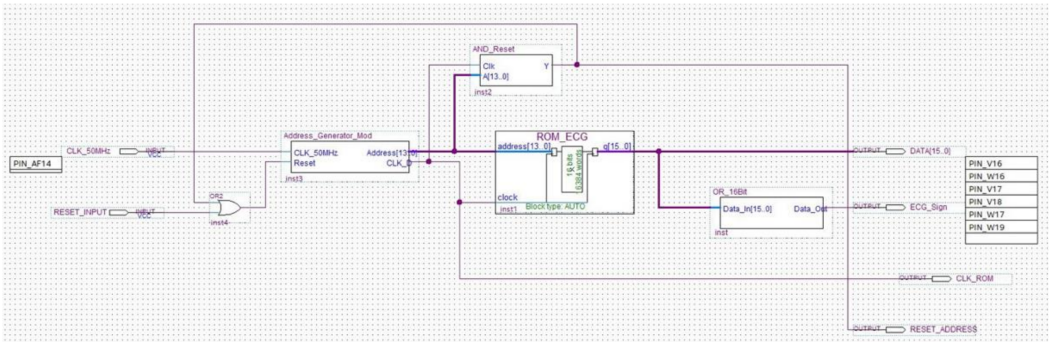


Figure 12. Schematic implementation of the ROM module.

3.2. Analyzer Block Module

The analyzer block module windows the pulsed ECG with a time frame three pulses long and implements the procedure previously indicated in the classification section. Figures 13 and 14 show elements comprising the analyzer module and its schematic, respectively. Figure 14 has been split, in lexicographical order, into three parts for the sake of visualization.

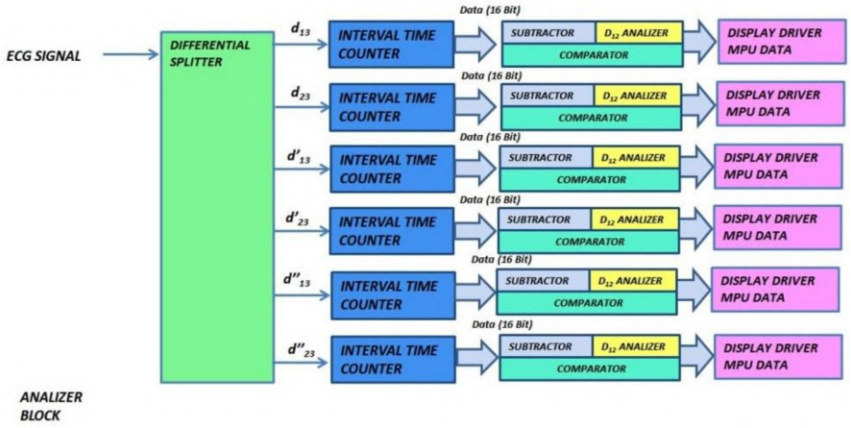
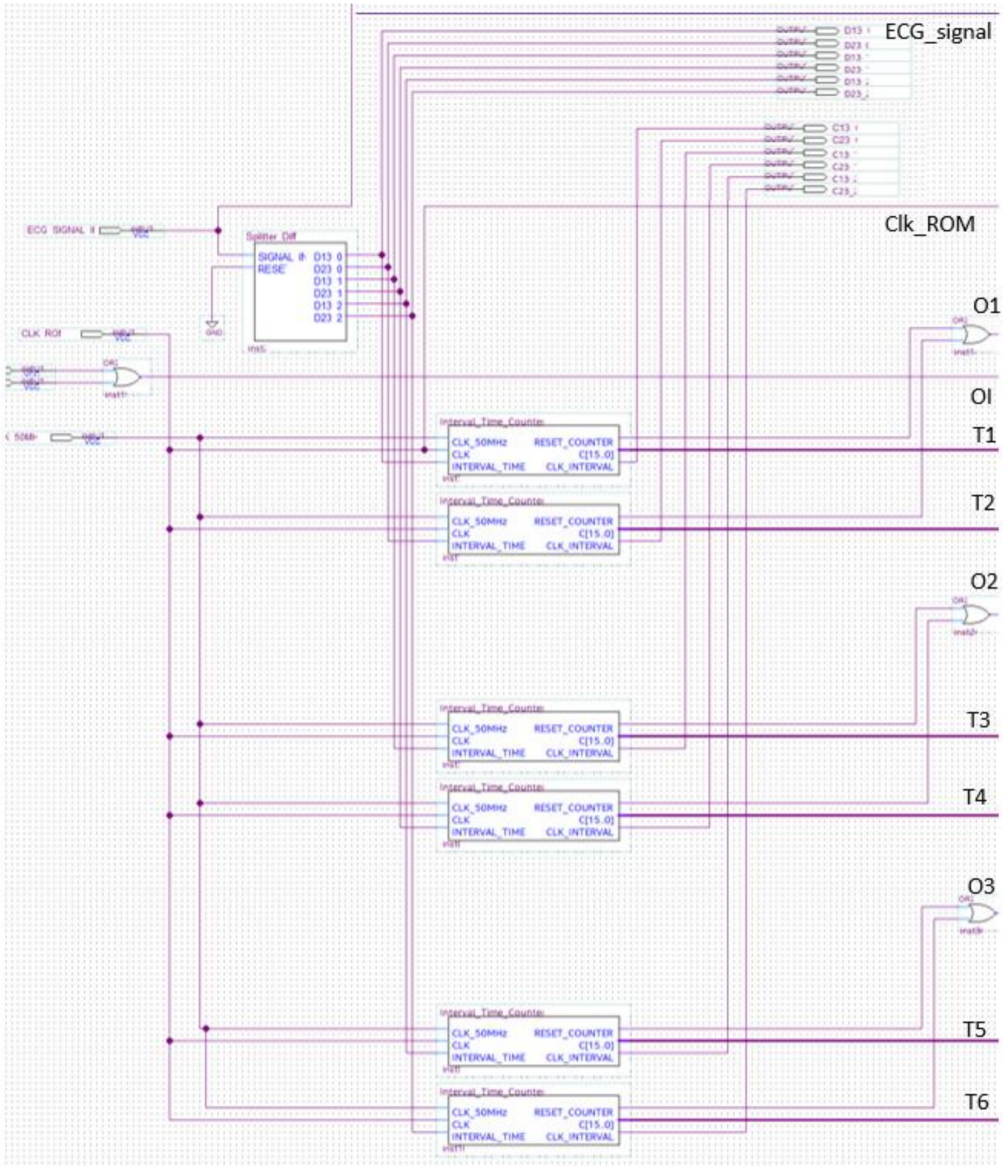


Figure 13. Functional and logic diagram of the analyzer.



(**a**)

Figure 14. *Cont.*

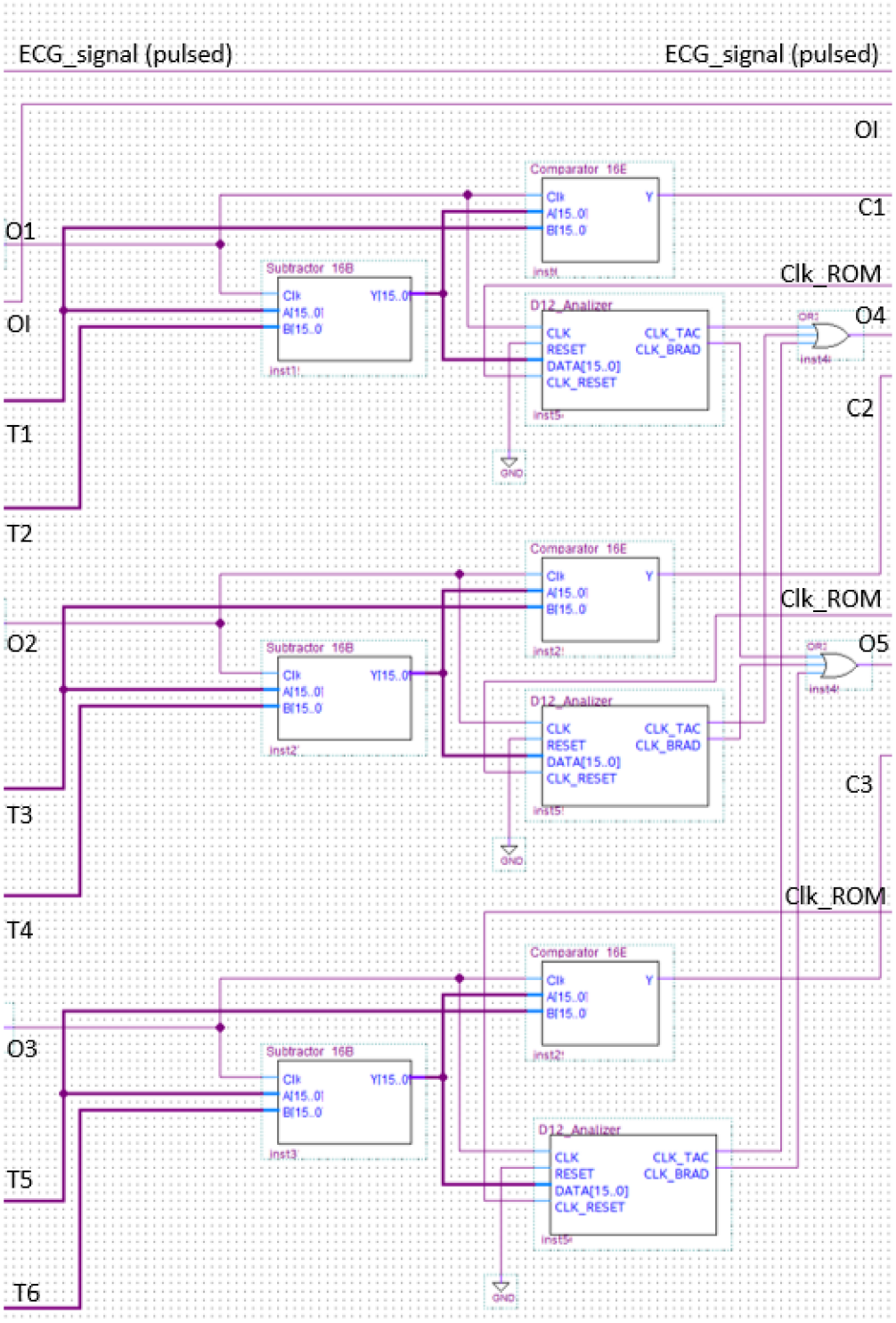
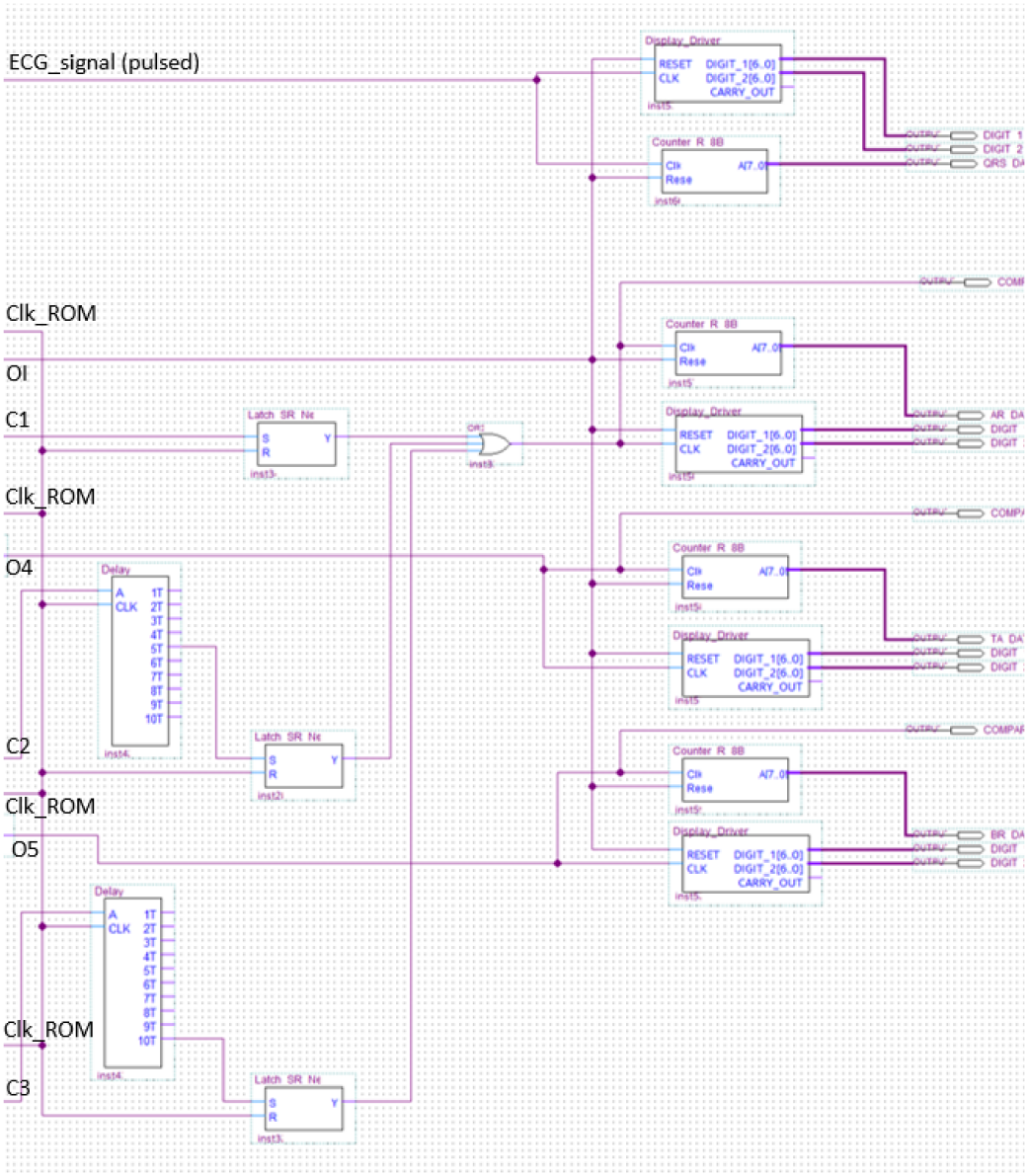


Figure 14. *Cont.*



(**c**)

Figure 14. The analyzer schematic. It is composed of three cascade blocks: (**a**) is the first block, (**b**) the second and (**c**) represents the last stage.

The aim of the differential splitter is both the splitting of the pulsed ECG signal into time frames composed of three consecutive pulses and the definition of the time window, which operates as stated in Section 2.3. The component at issue automatically locks the first pulse and maintains the link with the signal until the ROM locations have been completely scanned (Figure 15).

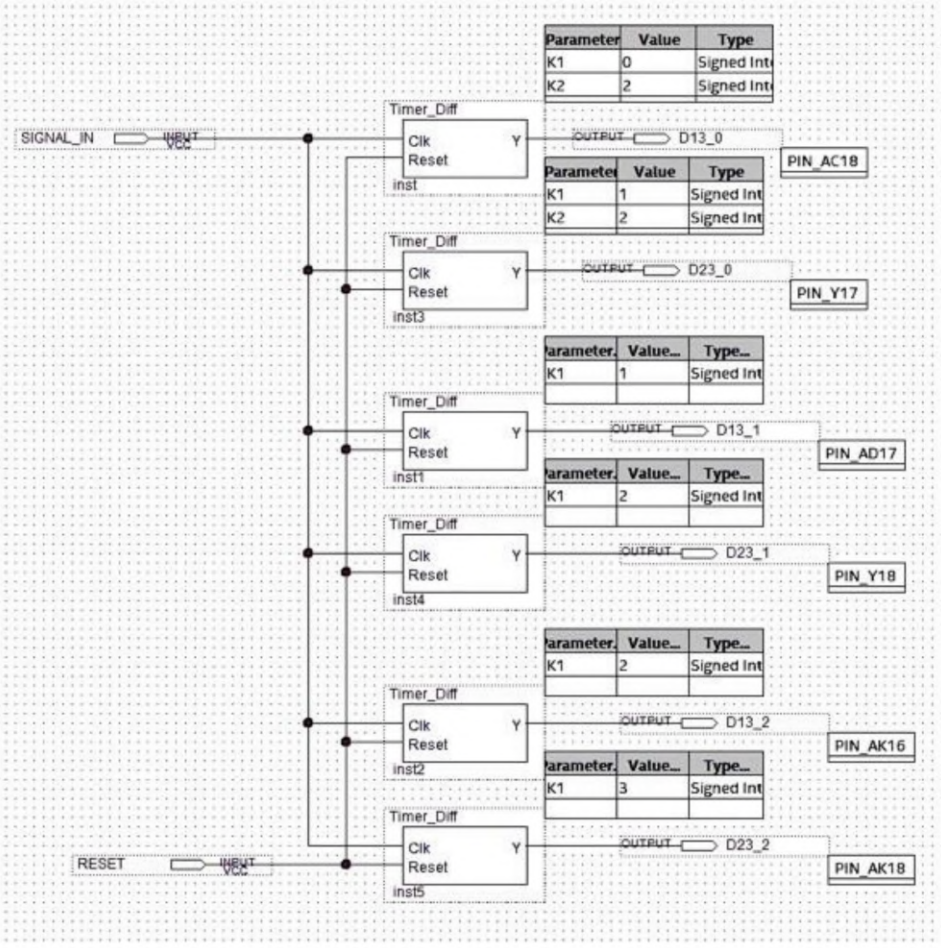


Figure 15. Schematic design of the differential splitter.

A reference clock signal at a stable and known frequency was superimposed by means of the Interval_Time_Counter. Distance between pulses was evaluated in terms of the number of clock periods occurring between them. The temporal distance between two ECG pulses was determined by counting the number of the clock periods between the two pulses. The signal generated by the differential splitter was fed into a 2-input AND gate with a reference clock signal (Figure 16). The Interval_Time_Counter counts the pulses of the clock signal obtained with the AND operation. The count result is a distance that is expressed in seconds, converted to a 16-bit binary number, and sent to the subsequent processing blocks.

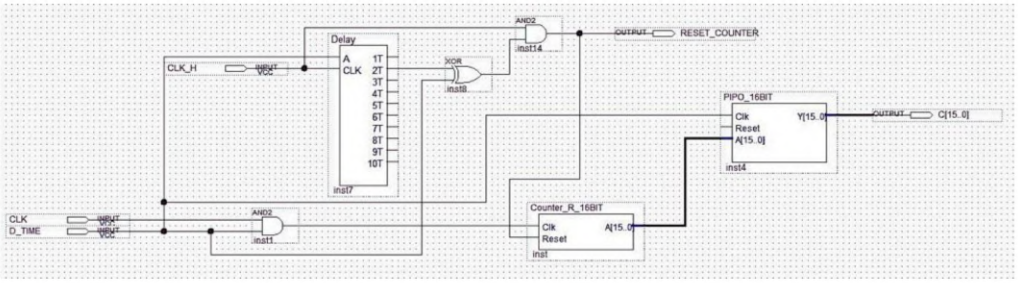


Figure 16. Schematic design of the Interval_Time_Counter.

The logic block making the classification of the detected arrhythmia in bradycardia or tachycardia is implemented and shown in Figure 17. One of the two outputs of the circuit in Figure 17 was set at a high logic value based on the subtractor output.

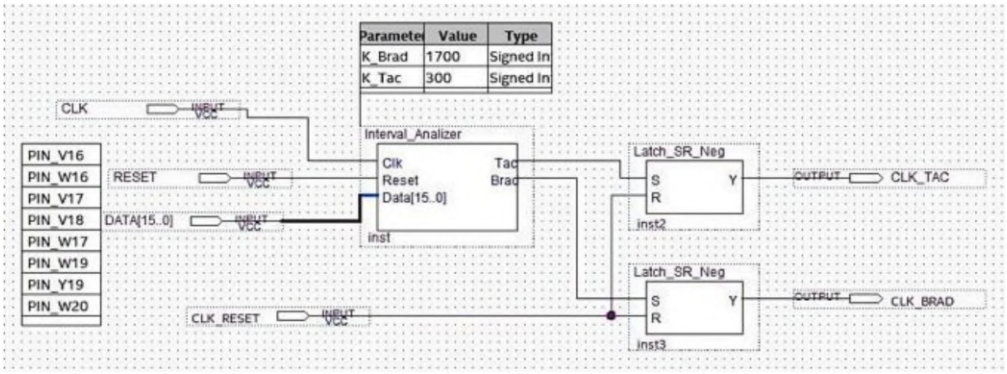


Figure 17. Schematic design of the logic block performing the analysis.

The schematic of the last block comprising the analyzer is indicated in Figure 18.

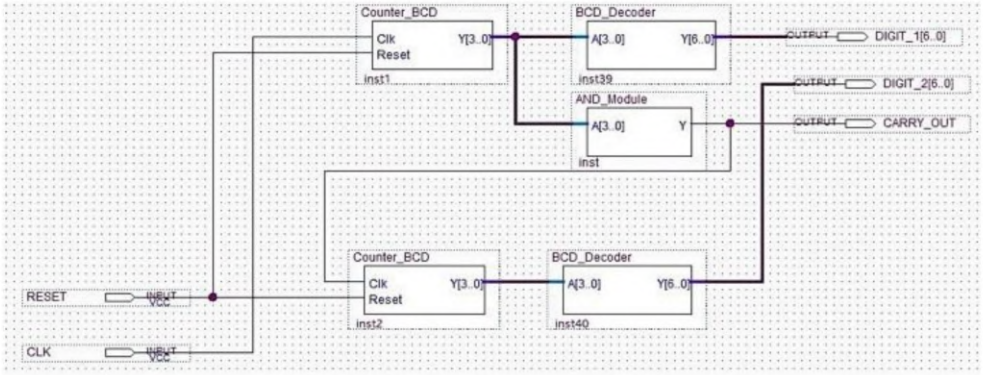


Figure 18. Schematic design of the display driver.

The analyzer symbol is indicated in Figure 19 with input and output signals. In particular:

- ECG_SIGNAL_IN is the pulses-transformed ECG signal coming from the ROM Block in debug mode, otherwise coming from the preprocessing and R-peak detection block in real-time operating mode;
- CLK_ROM is the input to which the clock generated by the ROM memory block is applied for the system synchronization;
- Reset_Address is the reset signal provided by the ROM block;
- Reset_Button is the reset signal sent to the FPGA through a switch of the development board for functional check;
- CLK_50MHz is the reference signal clock generated by the development board.
- D13_0, D13_1, and D13_2 are the signals generated by the differential splitter representing the distances $d^{j}_{pi-1,pi+1}$, $d^{j+1}_{pi-1,pi+1}$, and $d^{j+2}_{pi-1,pi+1}$, respectively;
- D23_0, D23_1, and D23_2 are the signals generated by the differential splitter and representing the $d^{j}_{pi,pi+1}$, $d^{j+1}_{pi,pi+1}$, and $d^{j+2}_{pi,pi+1}$, respectively;
- C13_0, C13_1, and C13_2 are the control signals for instrumental test of the system. They are generated by the Interval_Time_Counter and are expressed in 16-bit format. These signals represent the number of reference clock pulses counted in each window, which are D13_0, D13_1, and D13_2, respectively (that is the clock pulses counted by placing each of the signals D13_0, D13_1, and D13_2 in logic AND with the reference clock);
- C23_0, C23_1, and C23_2 are also control signals for the instrumental test of the system. They are generated by the Interval_Time_Counter and are expressed in 16-bit format. They represent the number of reference clock pulses counted in each window D23_0,

D23_1, and D23_2, respectively (that is the clock pulses counted by placing each of the signals D23_0, D23_1, and D23_2 in logic AND with the reference clock);

- DIGIT_1_QRS [6..0] and DIGIT_2_QRS [6..0], DIGIT_1_AR [6..0] and DIGIT_2_AR [6..0], DIGIT_1_TA [6..0] and DIGIT_2_TA [6..0], and DIGIT_1_BR [6..0] and DIGIT_2_BR [6..0] indicate the number of QRS, of arrhythmic, of tachycardic, and of bradycardic heartbeats detected, respectively. They are coded in binary-coded decimal (BCD) and visualized on the seven-segment display of the development board;
- QRS_DATA [7..0], AR_DATA [7..0], TA_DATA [7..0], and BR_DATA [7..0] are the 8-bit digital outputs that transmit the number of detected QRS, of arrhythmic, of tachycardic, and of bradycardic heartbeats to the data logger created with the FPGA-embedded processor;
- COMPARATOR OUT 1, 2, 3 are the output signals of the comparator inside the analyzer block, which are used as functional test outputs.

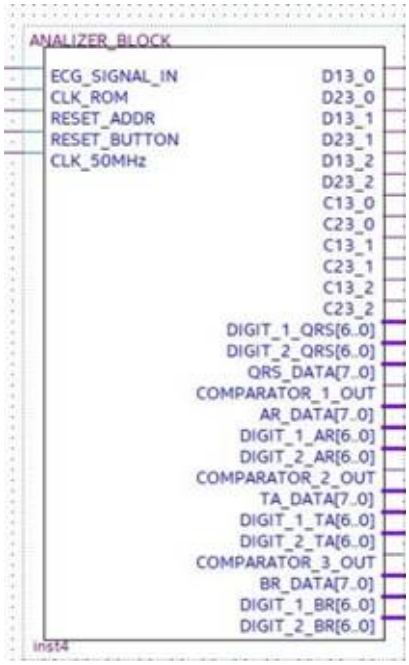


Figure 19. Black box representing the analyzer with the relevant input and output signals.

3.3. MCU Block

The microcontroller unit (MCU) data logger implemented inside the designed hardware is a functional block based on the selected FPGA soft or hard embedded processor. It performs calculations for diagnosis purposes (i.e., the PE risk, the QTc, and the QTc lengthening) and communicates with external peripherals, such as a personal computer displaying messages for debug purposes (for example log messages, arrhythmias warnings, number of pathological events counted, auto diagnosis results, etc.) [46]. Toward this aim, the MCU block is equipped with some PIOs (pin input/output). An adoption of interrupts is also avoided for real-time operation because the involved signals are slowly varying

4. Implementation of the FPGA-Based Embedded System

The FPGA CYCLONE V 5CSEMA5F31C6 by INTEL was adopted for system development [47]. The design was deployed on a DE1_SoC development board by TERASIC for test and debug purposes [48]. Our design environment was Quartus Prime by Intel/Altera [49]; however, it was portable on any FPGA foundry and development environment. The tool Platform Designer integrated in Quartus IDE was used for the MCU block implementation, while the Eclipse environment was selected for NIOS II firmware development. The PIOs

were read by using the "altera_avalon_pio_regs.h" library and were sent to the NIOSII console in string format through the JTAG UART.

For debug purposes, the system input was the ECG signal preprocessed and made impulsive by positioning a unit pulse in correspondence of each detected R peak. The signal was loaded in the ROM memory block. The 50 MHz operating clock provided by the DE1_SoC evaluation board was selected.

Efficiency of HW Design

For the designed FPGA-based system, the HW efficiency was quantified in terms of:

- ➢ Area occupancy and or amount of used hardware resources;
- ➢ Operating speed;
- ➢ Power consumption due to the system processing activity.

The implemented system occupies about 6% of the FPGA ALMs resources of the selected chip. Therefore, a good efficiency in terms of area consumption was achieved.

The timing performance was evaluated by the Timequest Timing Analyzer tool embedded in Quartus environment. The maximum operating frequency of the system clock is 1 GHz, which is far higher than the ECG signal processing needs. In fact, the sampling frequency of 1 kHz characterizes the ECG. Moreover, a positive slack was obtained, which ensures the fulfilment of timing requirements.

For power consumption and thermal power dissipation statistic evaluation, the power analyzer tool operating in post-fitting mode was adopted. This tool is powered by INTEL in the Quartus environment. Operating settings and conditions in terms of voltage and temperature are shown in Figure 20.

Device power characteristics	Typical
⌄ Voltages	
VCC	1.10 V
VCCA_FPLL	2.50 V
VCCPGM	1.80 V
VCCBAT	1.20 V
VCCE_GXB	1.10 V
VCCL_GXB	1.10 V
VCCH_GXB	2.50 V
VCCAUX	2.50 V
VCC_HPS	1.10 V
VCCRSTCLK_HPS	1.80 V
VCCPLL_HPS	2.50 V
VCCAUX_SHARED	2.50 V
2.5 V I/O Standard	2.5 V
⌄ Auto computed junction temperature	26.9 degrees Celsius
Ambient temperature	25.0 degrees Celsius
Junction-to-Case thermal resistance	2.30 degrees Celsius/Watt
Case-to-Heat Sink thermal resistance	0.10 degrees Celsius/Watt
Heat Sink-to-Ambient thermal resistance	2.10 degrees Celsius/Watt

Figure 20. Operating settings and conditions for voltage and temperature.

Adopting a power supply of 1.1 V, dynamic and static currents equal to 5.21 mA and 51.56 mA were drawn, respectively, resulting in 5.70 mW and 413.65 mW of FPGA dynamic and static power dissipation, respectively.

5. Results

5.1. Evaluation Parameters

The performance of our decision support system is evaluated by accuracy. In particular, the following expression is used [50]:

$$Accuracy\ (AC) = \frac{TP + TN}{TP + FP + TN + FN} \tag{6}$$

where TP (true positive) is the number of positives that are correctly identified as such (for example the number of arrhythmic ECG signals correctly classified). FN (false negative) is the number of positives that are classified as negatives (for example the number of arrhythmic ECG signals incorrectly classified as normal). FP (false positive) is the number of negatives classified as positives (such as the number of healthy ECGs classified as arrhythmic signals). TN (true negative) is the number of negatives that are correctly identified as such (for example the number of healthy ECGs correctly classified)

5.2. Results of Matlab Simulations and FPGA Classifier Performance

Simulations were performed by processing both real and properly modified real ECG signals with the proposed CAD system.

The implemented procedure detects all the R peaks of the tested signals. Properly modified real ECG signals corrupted by different noise values were used as a test bench to improve realism and the mimic signals acquired in free-living conditions. A mixture of muscle noise, electrode movement artifacts, and baseline wander was added to the ECG under test. Taking into account input ECG signals characterized by a signal to noise ratio (SNR) equal to 20 dB, the precision in identifying the correct R peak position is corrupted by a systematic error having an average value equal to 2 ms. The error standard deviation is 1.1 ms. It depends on residual noise superimposed on ECG signals after the preprocessing phase.

Figure 21 shows the obtained results of the simulation carried out in Matlab using record 11 of the database. The diagnosis in terms of arrhythmias, QT lengthening, and PE embolism risk is also shown. The graphical user interface (GUI) in Figure 21 has also been developed in the Matlab environment.

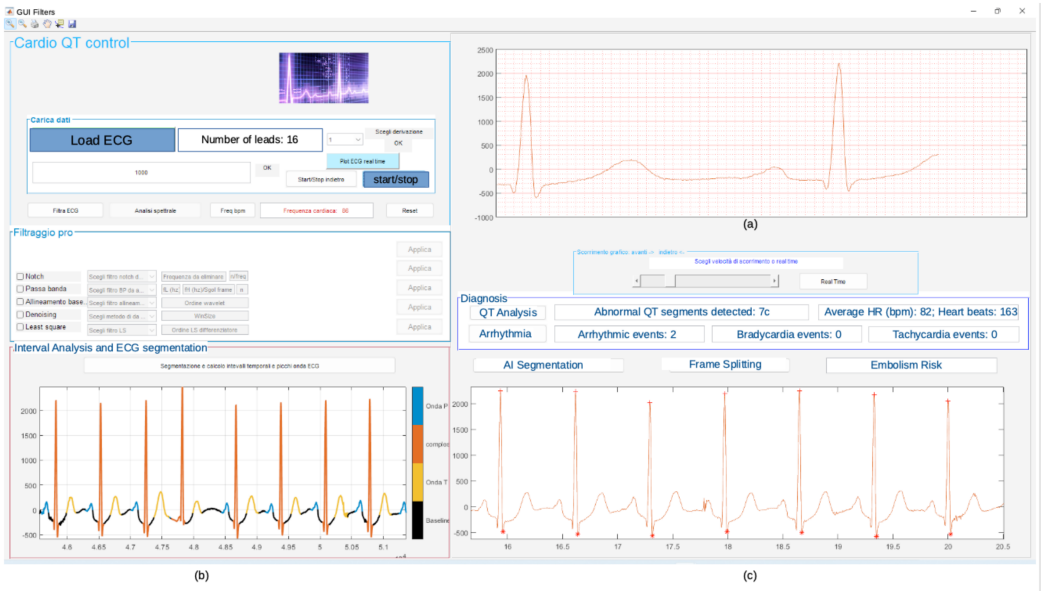


Figure 21. Results of Matlab simulation on record 11: (**a**) filtered ECG signal, (**b**) segmented signal, (**c**) diagnosis in terms of arrhythmias, QT lengthening, and PE risk evaluation.

The Signal Tap II Logic Analyzer (embedded in Quartus prime IDE) and the Zeroplus lab-c (an external USB logic analyzer) were also used for the system debug. Results of these analyses reflect specifications and simulations of the sequential machine performed by using the waveform editor tool of the Quartus IDE. In Figures 22 and 23, the results of the instrumental analysis are shown. After the accurate detection of R peaks, the time distance between two consecutive R peaks of the pulses-transformed ECG signal was evaluated and compared according to the conceived procedure. The detection of an arrhythmic event is indicated by the comparator by the generation of a clock signal, which enables a counter.

The high performance of the proposed system, which adopts the NIOS II architecture, led us to consider that it was unessential to use the hard macro ARM core (HPS hard processor), which is in the equipped Cyclone V FPGA.

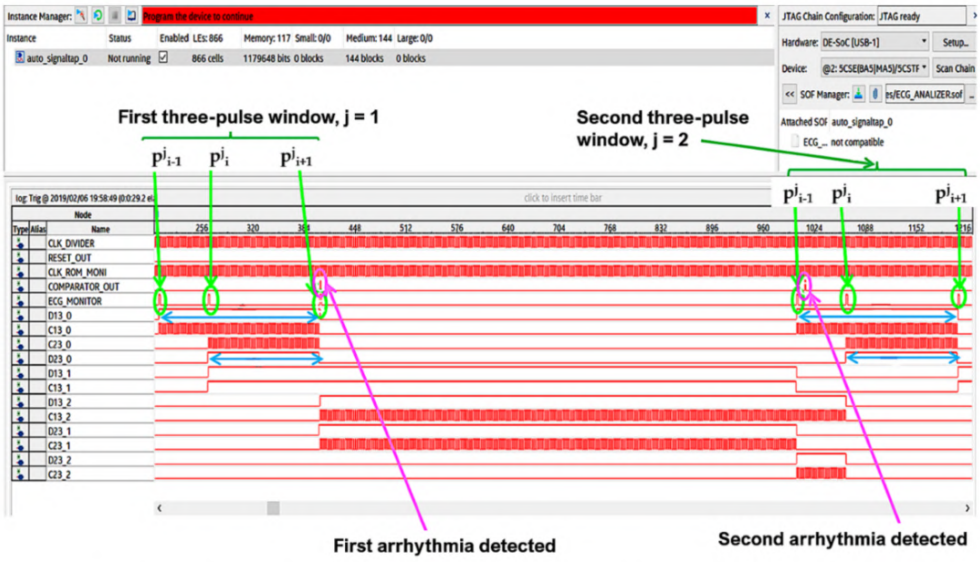


Figure 22. Arrhythmias detection by instrumental analysis performed using the Signal Tap II Logic Analyzer.

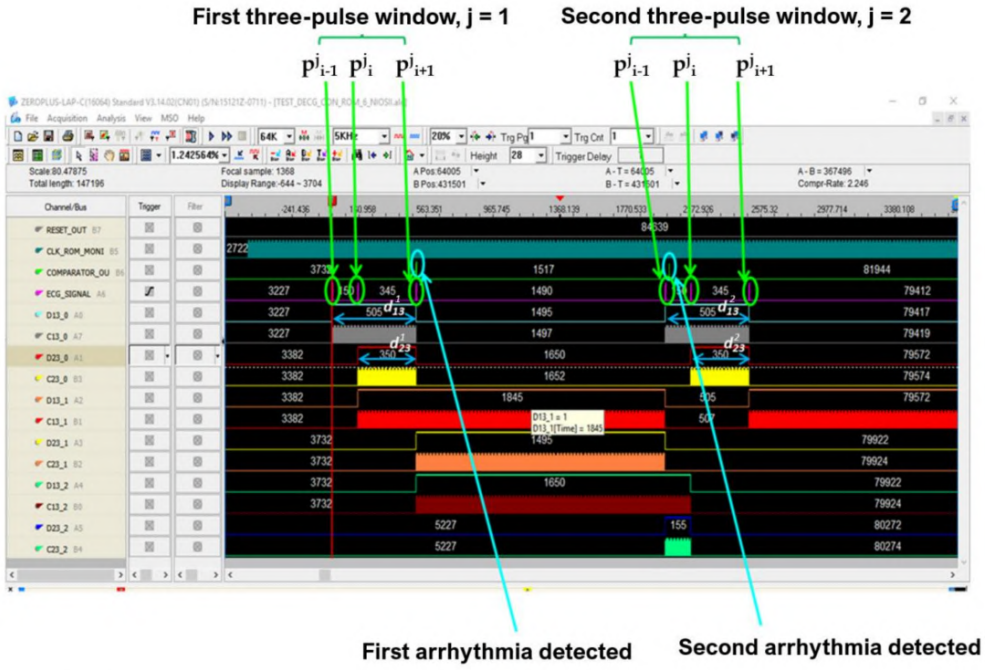


Figure 23. Arrhythmias detection by instrumental analysis performed using Zeroplus lab-c.

Successful results are also achieved by our CAD system in detecting arrhythmic disorders in stressed conditions. A value of 99.20% accuracy is achieved by taking into account 0.02 mV for the root mean square value of noise voltage (N_{rms}). The selected N_{rms} is referred to as typical value in the Physionet software, which is used for the dataset generation. Different N_{rms} values are also considered to test our system in stressed conditions. The performance reached by our method for each noise value added to the ECG signal is detailed in Table 1.

Table 1. Obtained performance with different root mean square values of noise voltage.

N_{rms} (mV)	Accuracy (%)
0.02	99.20
0.04	99.20
0.06	99.20
0.08	99.20
0.1	98.80
0.4	97.60

In order to evaluate the classification capacities of the algorithm implemented with the FPGA device, the same ECG records used for the procedure assessment are considered. Proper instrumental checks have been performed and pathologies have been detected once the Quartus project has been compiled and the FPGA has been programmed by using the Quartus programmer. The obtained performance results are not substantially different from the values obtained with the procedure developed in the Matlab environment.

6. Discussions

Development of new technologies has changed the approach with which physicians treat, prevent, and monitor cardiac illnesses. Decision support systems, which make it possible for the automatic processing and classification of ECG signals, are receiving clinical attention given that an early detection of cardiac disorders avoids severe health consequence for patients. Capturing ECG signals for arrhythmia detection is time consuming as ECG symptoms might need to be captured or monitored over several hours. For this reason, various research efforts are indicated in the literature to develop computer-aided detection and diagnosis systems for the automatic processing and real-time monitoring of ECG signals [51]. The implementation of new methods is not limited to software approaches, it also involves hardware design in order to optimize the system performance in terms of power consumption, area occupancy, and computational cost. FPGA-based chips are mostly considered to develop arrhythmia detectors. In [52], hardware and software implementations for heart-rate estimation are indicated, which are based on the RR interval evaluation. The ECG signal under test is enhanced and denoised using the empirical mode decomposition method. Automatic detection of noisy intrinsic mode functions is performed using spectral flatness measure and a threshold methodology is adopted for R peak localization. Xilinx Spartan 3E FPGA board using Verilog language is used for the design implementation.

Neural networks are also adopted as classifiers for arrhythmias recognition. Multilayer preceptors [53], probabilistic neural networks [54] and artificial neural networks [55], [56] are adopted in FPGA-based systems to discriminate the particular arrhythmia classes. Hermite functions are used in [57] to design and implement a hardware architecture that is able to characterize heartbeats in real time. Hermite fitting makes it possible to find the approximation of the QRS complex with the best minimum mean square error. The first stage of the conceived signal chain performs signal filtering and QRS peak detection, while the second stage evaluates a best Hermite–polynomial fit for the identified beat.

To reduce QRS complexity and artifacts, a peak envelope extraction algorithm is proposed in [58], which implements a Shannon energy envelope and Hilbert transform. In particular, the Shannon energy envelope employs peak detection, false noise, and false positive R-wave identification, while precise R-wave localization is reached through real-value fast Fourier transform and imaginary-value fast Fourier transform. A multiplier is used to detect various cardiac dysrhythmias.

An automated heartbeat classifier for wearable devices able to perform a real-time monitoring of cardiac activity is designed in [59]. The presented procedure is based on the well-known Pan–Tompkins algorithm [60]; however, it uses a different classifier. In fact, the implemented method adopts only one set of adaptive threshold computations and IIR filters instead of FIR filters.

In order to assess the performance of our DSS, a comparison was performed with the aforementioned systems, which are some of the most popular FPGA-based methods indicated in the literature in the last seven years. It has been seen from Table 2 that the proposed system has significant performance. In fact, our system is characterized by less area occupancy for the hardware implementation, high accuracy value, and reduced power dissipation compared with the other reported methods. The reduced hardware used for our system development provides the possibility to upgrade/enrich the designed circuit with new features in the future using the same chip. In addition, our system allows us to evaluate the QT-segment lengthening and the pulmonary embolism (PE) risk assessment.

Table 2. Comparative analysis with some FPGA-based arrhythmias detectors.

	HW Used	Power Supply	Power Dissipation	Area Occupancy	Accuracy (%)
Ref. [52]	Xilinx Spartan XC3S500	NA	NA	38%	94.76
Ref. [53]	Artix-7	NA	NA	NA	98.3
Ref. [54]	Artix-7	NA	NA	NA	98.27
Ref. [55]	Altera DE2-115	NA	NA	NA	95.3
Ref. [56]	Artix-7	NA	NA	NA	86
Ref. [57]	Artix-7	5 V	28 mW	NA	NA
Ref. [58]	Xilinx Spartan 3	NA	280 mW	NA	93.6
Ref. [59]	Xilinx Spartan 6	NA	0.48 mW	32%	99.65
Our system	Intel Cyclone V	1.1 V	5.70 mW	6%	99.20

7. Conclusions

Automatic ECG signal analysis is projected to play a greater role in patient monitoring and diagnosis. The application of computer-aided equipment is especially promising in supporting physicians in clinical practices. In this paper, we present a novel, dedicated implementation of the ECG signal processing chain for arrhythmia detection, QT-segment lengthening evaluation, and assessing pulmonary embolism risk. The method was first developed in Matlab® environment for debug purposes before the hardware implementation was validated on an FPGA device. We designed the conceived system using an algorithm-to-hardware compiler tool chain and characterized the hardware using the DE1_SoC development board by Terasic. Cost effectiveness and low power consumption characterize the system, which can be considered a home-based heart-monitoring or heart-screening device. The implemented procedure is suitable to be embedded in smartwatch sensors for ECG recording. In fact, as a consequence of multi-core chips and larger-memory adoption, improvements in the computation power and storage capacity of smartphones/smartwatches have established the popularity of sensor systems for the measuring and monitoring of environmental and health-care parameters. In this way, several anomalies can be detected in real time [61]. In addition, the designed system could be equipped with an IoT interface to transmit information and share data with medical specialists for consultations in real time. The transmission of patient diagnostic data and/or patient biological signals between hospitals and different administrative organizations

have become a common practice for many reasons, such as diagnosis, treatment, distance learning, training purposes, teleconferences between clinicians, and medical consultation between physicians and radiologists. For enhancing data interoperability and integrity regarding electronic health record sharing, Blockchain-based framework methods can be proposed to facilitate communication between medical providers, who store medical data in the cloud and share the electronic health data of patients [62]. Our system has not been synthetized to detect all heart-related diseases, which are detectable by physicians analyzing ECG signals. However, the designed method is a versatile system that allows making changes in each section in an independent way. Upgrades/improvements concerning cardiac illnesses and disorders that indirectly affect the heart can also be developed in the future.

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