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Silicon-Compatible Memristive Devices Tailored by Laser and Thermal Treatments

Maria N. Koryazhkina ^{1,*} , Dmitry O. Filatov ¹, Stanislav V. Tikhov ¹, Alexey I. Belov ¹, Dmitry S. Korolev ¹ , Alexander V. Kruglov ¹, Ruslan N. Kryukov ¹ , Sergey Yu. Zubkov ¹, Vladislav A. Vorontsov ¹, Dmitry A. Pavlov ¹ , David I. Tetelbaum ¹, Alexey N. Mikhaylov ¹ , Sergey A. Shchanikov ² , Sungjun Kim ³ and Bernardo Spagnolo ^{1,4}

¹ Research and Education Center “Physics of Solid State Nanostructures”, National Research Lobachevsky State University of Nizhny Novgorod, 603022 Nizhny Novgorod, Russia; dmitry_filatov@inbox.ru (D.O.F.); tikhov@phys.unn.ru (S.V.T.); belov@nifti.unn.ru (A.I.B.); dmkorolev@phys.unn.ru (D.S.K.); krualex@yandex.ru (A.V.K.); kriukov.ruslan@yandex.ru (R.N.K.); zubkov@phys.unn.ru (S.Y.Z.); vladislav.vorontsov1@gmail.com (V.A.V.); pavlov@unn.ru (D.A.P.); tetelbaum@phys.unn.ru (D.I.T.); mian@nifti.unn.ru (A.N.M.); bernardo.spagnolo@unipa.it (B.S.)

² Department of Information Technologies, Vladimir State University, 600000 Vladimir, Russia; seach@inbox.ru

³ Division of Electronics and Electrical Engineering, Dongguk University, Seoul 04620, Korea; sungjun@dongguk.edu

⁴ Dipartimento di Fisica e Chimica “Emilio Segrè”, Group of Interdisciplinary Theoretical Physics, Università degli Studi di Palermo and CNISM, Unità di Palermo, I-90128 Palermo, Italy

* Correspondence: mahavenok@mail.ru



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Abstract: Nowadays, memristors are of considerable interest to researchers and engineers due to the promise they hold for the creation of power-efficient memristor-based information or computing systems. In particular, this refers to memristive devices based on the resistive switching phenomenon, which in most cases are fabricated in the form of metal–insulator–metal structures. At the same time, the demand for compatibility with the standard fabrication process of complementary metal–oxide semiconductors makes it relevant from a practical point of view to fabricate memristive devices directly on a silicon or SOI (silicon on insulator) substrate. Here we have investigated the electrical characteristics and resistive switching of SiO_x- and SiN_x-based memristors fabricated on SOI substrates and subjected to additional laser treatment and thermal treatment. The investigated memristors do not require electroforming and demonstrate a synaptic type of resistive switching. It is found that the parameters of resistive switching of SiO_x- and SiN_x-based memristors on SOI substrates are remarkably improved. In particular, the laser treatment gives rise to a significant increase in the hysteresis loop in *I*–*V* curves of SiN_x-based memristors. Moreover, for SiO_x-based memristors, the thermal treatment used after the laser treatment produces a notable decrease in the resistive switching voltage.

Keywords: memristor; silicon oxide; silicon nitride; SOI technology; resistive switching; electrical characteristics; laser treatment; thermal treatment

1. Introduction

A memristor is a two-terminal nanoelectronic element that changes and remembers its resistance depending on the applied voltage and the charge flowing through it. Its main difference from semiconductor memory elements, which implement a binary code and two stable states, is the multilevel, synaptic nature of the conduction switching [1]. It is believed that this will make it possible to create next-generation computers (with a non-von-Neumann architecture) and neuromorphic artificial intelligence systems on the basis of memristors [2–12]. The main disadvantages of memristors fabricated in the form of metal–insulator–metal (MIM) or metal–insulator–semiconductor (MIS) structures are the reproducibility of resistive switching (RS) parameters, which is insufficient for practical

use (stochasticity), high values of RS voltages, and the complexity of integration into a standard complementary metal–oxide–semiconductor (CMOS) fabrication process. Currently, approaches to solving these problems are being developed: the use of new materials and various interfaces [13–16], the use of signals with a special shape for RS [17], the use of optical radiation [18] or noise [19–21] as parameters controlling the switching dynamics, programming the amplitudes and durations of switching pulses [22,23], etc. Indeed, the wider application of memristors is limited by their insufficient stability, the high variability of RS parameters, and a lack of understanding of the drift–diffusion processes responsible [24]. One of the fundamental origins of the instability of the memristor parameters is the essentially stochastic nature of RS [20]. Furthermore, the noise sources can induce new ordered dynamical structures and cause new phase transition phenomena [25,26]. Therefore, of all these approaches, the one based on the constructive role of both internal (thermal) and external noise sources is most promising due to the intrinsic stochastic nature of resistive switching in memristor devices [19–21].

Transition metal oxides (e.g., HfO_x [27,28], TaO_x [29,30], ZrO_x [31,32], TiO_x [33,34], and more complex compounds such as perovskites [35]), as well as SiO_x , and GeO_x , are considered promising insulator materials for memristors. Recently, intensive research has also been carried out on memristive structures based on SiN_x [36,37]. This is of practical interest due to their compatibility with the standard technology for creating modern integrated circuits. The use of SiO_x and SiN_x insulator films involves a number of practical advantages. For example, the authors of [38] carried out a comprehensive comparison of the RS parameters of memristive structures based on HfO_x and SiO_x and showed a lower variability in resistance in different states of SiO_x -based memristors. In turn, the authors of [39] demonstrated the absence of changes in the value of currents in resistive states of SiN_x -based memristors irradiated with As^+ during 10^5 cycles of RS and the minimum variability of switching voltages. It should be noted that SiO_x - and SiN_x -based memristors have a filamentary resistive switching mechanism [40,41].

The use of a semiconductor as one of the electrodes of a memristive structure is also important from the point of view of integrating memristors into a standard CMOS fabrication process [42,43]. One of the electrodes is silicon, which simplifies the technological process and allows the memory to be integrated monolithically on a single platform with a transistor [44,45]. In these articles, bulk silicon was used as an electrode. However, in the preparation of most semiconductor devices and microcircuits, preference is given to “silicon-on-insulator” (SOI) substrates due to its advantages over bulk silicon: lower power consumption and the higher performance and density of elements [46]. Therefore, from a practical point of view, it is advisable to implement memristive structures on SOI substrates. Despite the significant number of published studies of memristive structures with a bulk silicon electrode, structures on SOI substrates must be studied independently due to the peculiarities of morphology and structure of the latter. Thus, the development and investigation of memristive structures, in which the SOI substrate acts as an electrode, is of considerable theoretical and practical interest. However, such data are nearly absent in the literature, except for several separate reports on the use of SOI in memristive devices (see, for example, [47–50]).

Despite the practical advantages of using a semiconductor as an electrode in a memristive structure, one should not forget the presence of surface states (SS) at the insulator/semiconductor interface, which is undesirable from the point of view of creating memristive structures. These states make a significant contribution to the total serial resistance of the structure [51]. A decrease in their density leads to a redistribution of the external voltage, so that the electric field strength in the insulator increases, thereby stimulating resistive switching. Thermal treatment (TT) is a widely used method of dealing with such defects. Laser treatment (LT) can be used for the same purposes. In the latter case, the effect is achieved due to heating of the substrate because of the absorption of laser radiation in it. In addition, LT is used to modify the charge state of an insulator in a flash memory device, which is used to completely erase information in memory elements [52].

Therefore, LT and TT can be effectively used to change the electrical characteristics of memristive structures.

We propose a comprehensive approach to improving the parameters of RS: namely, increasing the resistance ratio in extreme resistive states and decreasing the RS voltages of memristive structures based on promising and accessible insulator layers— SiO_x and SiN_x , fabricated under industrial conditions on SOI substrates. This approach is based not only on the use of materials that are standard for the CMOS fabrication process, but also on the use of LT and TT, which are widely used in the microelectronic industry to control the electrical parameters of devices. In addition, the investigation of the frequency dependences of electrical characteristics of memristive structures carried out in this work makes it possible to obtain the necessary detailed information about the processes occurring in the insulator film and about the state of insulator/semiconductor interfaces in different resistive states [53]. Data in this paper are presented in the same order in which they were obtained, so that the reader can unambiguously determine the contribution of LT and TT to the change in resistive switching parameters.

To the best of our knowledge, such a comprehensive study of SiO_x - and SiN_x -based memristive structures fabricated on SOI substrates, including the influence of LT and TT on their electrical characteristics (RS parameters), has not been carried out previously.

2. Materials and Methods

SiO_x and SiN_x films (with a nominal thickness of 13 nm each) were deposited on commercial SOI substrates with a device layer thickness of 360 nm by plasma-enhanced chemical vapor deposition under the following conditions:

- SiO_x —using 5% SiH_4/N_2 (160 sccm), N_2O (1500 sccm) and N_2 (240 sccm) at a pressure of 550 mTorr and high frequency (HF) power of 60 W, with a deposition rate of 200 Å/min;
- SiN_x —using 5% SiH_4/N_2 (800 sccm), NH_3 (10 sccm) and N_2 (1200 sccm) at a pressure of 580 mTorr and HF-power 60 W, with a deposition rate of 100 Å/min.

Top Au electrodes (20 nm) with a Zr sublayer (8 nm) with an area of $S \sim 10^{-2}$ (in this study) and 10^{-3} cm^2 were deposited on the surface of insulators by magnetron sputtering at a temperature of 473 K. A schematic representation of the fabricated structures is shown in Figure 1. The devices were prepared in the form of a metal–insulator–semiconductor sandwich with a common bottom electrode (SOI) and local top (Au with a Zr sublayer) electrodes. Figure 2 is an optical image of a fragment of the device showing two top electrodes of a small area and one of a larger area. The optical image was obtained using a Leica DM 4000 M optical microscope (Wetzlar, Germany).

The electrical characteristics were measured using a semiconductor device parameter analyzer, Agilent B1500A (Santa Rosa, CA, USA). The sign of voltage across the structures corresponded to the potential of the top electrode relative to the potential of the bottom electrode. I – V curves and the small-signal C – f , G – f , and R – f characteristics of memristors were measured in parallel and series capacitor equivalent resistor–capacitor circuits (see Figure 1 for explanation) [54] in the frequency range 10^3 – 2×10^6 Hz. The values of parallel capacitance (C_p), parallel conductance loss (G_p/ω), dielectric loss tangent ($\text{tg}\delta$), parallel (R_p), and series (R_s) resistances were determined. The parameters of parallel capacitor equivalent circuit are determined by the electronic phenomena in an insulator, while the parameters featuring a serial capacitor equivalent circuit are determined by the resistance of electrodes and that of the transition layer between the electrode and insulator film [54].

The information on relaxation processes in the insulator was obtained by analyzing the Cole–Cole diagrams—the dependences of G_p/ω on C_p , which were obtained from corresponding frequency dependences [55]. As shown below, the obtained diagrams were either a circular arc or a semicircle. Thus, in the first case, the spectrum of SS at the insulator/semiconductor interface was continuous, while the second case indicates the presence of a mono-level of SS. An analysis of the Cole–Cole diagrams makes it possible

to estimate the effective density of SS at the Fermi level (N_{ss}). In the case of a continuous spectrum of SS, for such an estimate, one can use the following equation [56]:

$$N_{ss} = \frac{[G_p/\omega]_{max}}{0.4q^2S}, \quad (1)$$

where $[G_p/\omega]_{max}$ is the maximum value of parallel conductance loss, q is the electron charge, and S is the structure area (i.e., the area of the top electrode). In the case of a mono-level of SS, one can use the following equation [56]:

$$N_{ss} = \frac{8kT[G_p/\omega]_{max}}{q^2S}, \quad (2)$$

where k is the Boltzmann constant and T is the temperature.

In addition, measurements of capacitance–voltage and conductance–voltage characteristics were carried out in a parallel capacitor equivalent resistor–capacitor circuit at a small test signal frequencies of 10 and 100 kHz.

It should be noted that the investigated memristive structures initially had a conductive state. The investigations of the electrical characteristics of memristive structures were carried out in initial state (IS), in low-resistance state (LRS), and in high-resistance state (HRS).

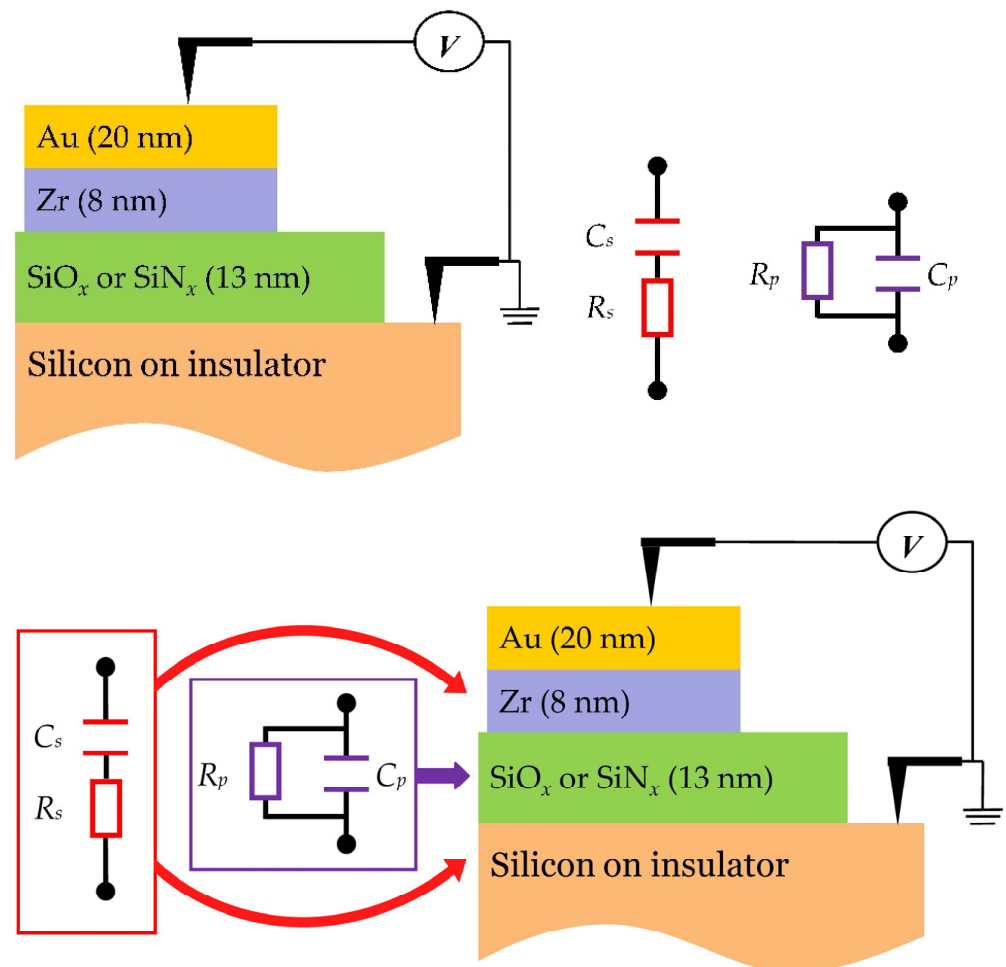


Figure 1. Schematic representation of SiO_x - and SiN_x -based memristors and the simplest capacitor equivalent resistor–capacitor circuits.

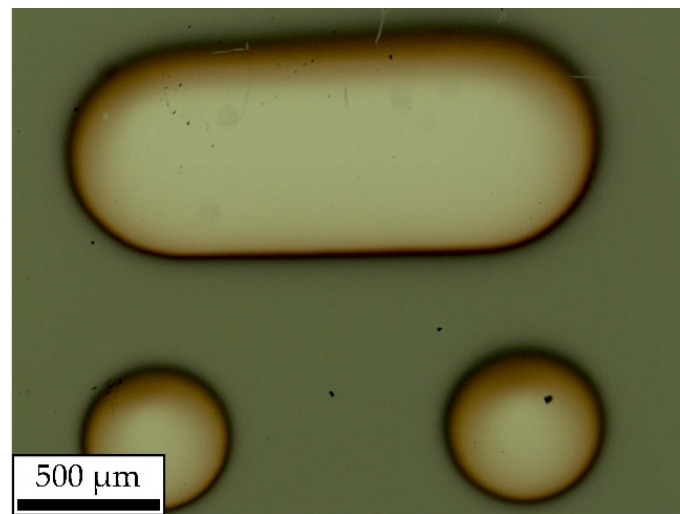


Figure 2. Optical image of a fragment of the device.

As mentioned above, LT can be used to change the electrical characteristics of memristive structures, which determine RS parameters. It is assumed that LT will make it possible to reduce the built-in charge in insulator films and to lower the density of SS at the insulator/semiconductor interface in memristive structures. Therefore, some memristive structures were subjected to LT. For this, a semiconductor laser with a power of 1.5 W and a wavelength of 460 nm, which corresponds to a photon energy of 2.7 eV, was used in the continuous mode. Irradiation was carried out through the top electrode for 10 min. It should be noted that the top Au electrodes with a thickness of 20 nm were semitransparent for the laser wavelength used [57]. Under the influence of laser radiation, the structure heats up to ≈ 473 K.

Thermal treatment is a widely used method for changing the density of SS at the insulator/semiconductor interface. Therefore, in order to improve the state of this interface, some of the SiO_x -based memristive structures were subjected to TT. For this purpose, memristive structures were placed in a hermetically closed metal thermostat, which was slowly heated at a rate of 13.5 K/min using an electric heater or cooled with liquid nitrogen. Investigations of electrical characteristics were carried out in a temperature range of 77–600 K in an atmosphere dried with silica gel. The temperature was maintained with an accuracy of 1 K.

Structural investigations of the SiO_x and SiN_x films and memristive structures based on them were carried out by X-ray photoelectron spectroscopy (XPS) and transmission electron microscopy (TEM). The profiling of samples using the XPS method implies the use of ion etching. The question arises of the correct determination of the etching rate and the existence of an error in determining the depth. If the rate can be determined using calibration samples, then the error is determined for each sample separately. A large contribution to the error when determining the depth is made by irregularities on the surface of the sample, due to which shading occurs during the etching process [58]. For correct interpretation of the data, information on the roughness obtained by atomic force microscopy (AFM) was used.

3. Results and Discussion

3.1. SiO_x -Based Memristive Structures on SOI Substrates

According to the AFM data (Figure 3a), the root mean square roughness of the SiO_x film is 1.8 nm. Figure 3b presents XPS data for SiO_x films before and after annealing at 550 K. The stoichiometry of the SiO_x film barely changes between before and after annealing, and is $x \approx 1.8$. One can also notice a transition layer at the SiO_x /SOI interface, the thickness of which is ~ 15 nm.

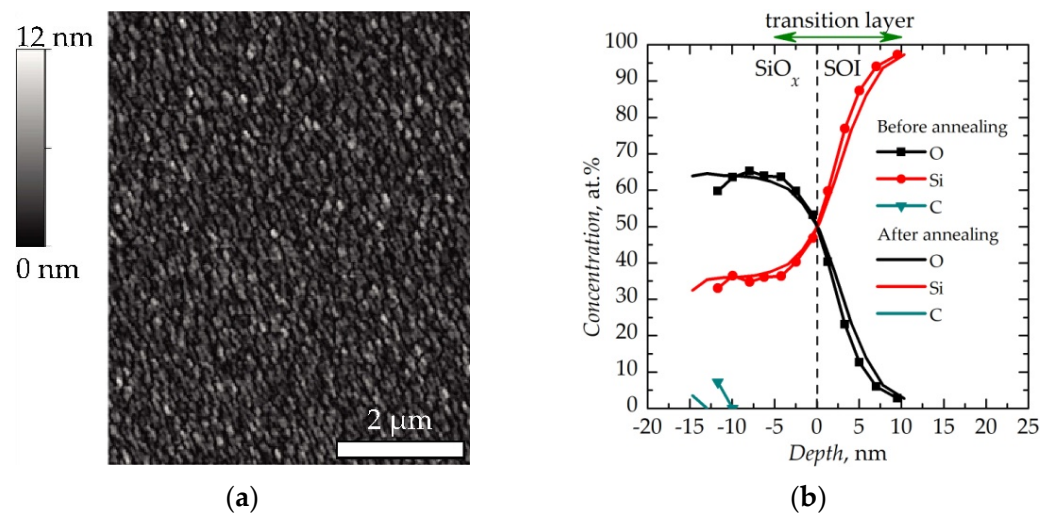


Figure 3. (a) AFM image of SiO_x film surface; (b) distribution of chemical elements over depth of SiO_x film before and after annealing at 550 K. The origin of the coordinates along the abscissa coincides with the SiO_x/SOI interface.

Figure 4 shows TEM images of a cross section of a SiO_x -based memristive structure after LT and TT. According to Figure 4, the SiO_x film has an amorphous structure. At the same time, Si (area 4), ZrO (areas 1 and 3) and ZrO_2 (area 2) nanocrystallites were found in the Zr sublayer and at the interface with the insulator. The structure of the observed nanocrystallites was determined by comparing the interplanar spacing in TEM images with the literature data. This means partial oxidation of Zr electrode and silicon oxide reduction in contact with this electrode during treatments.

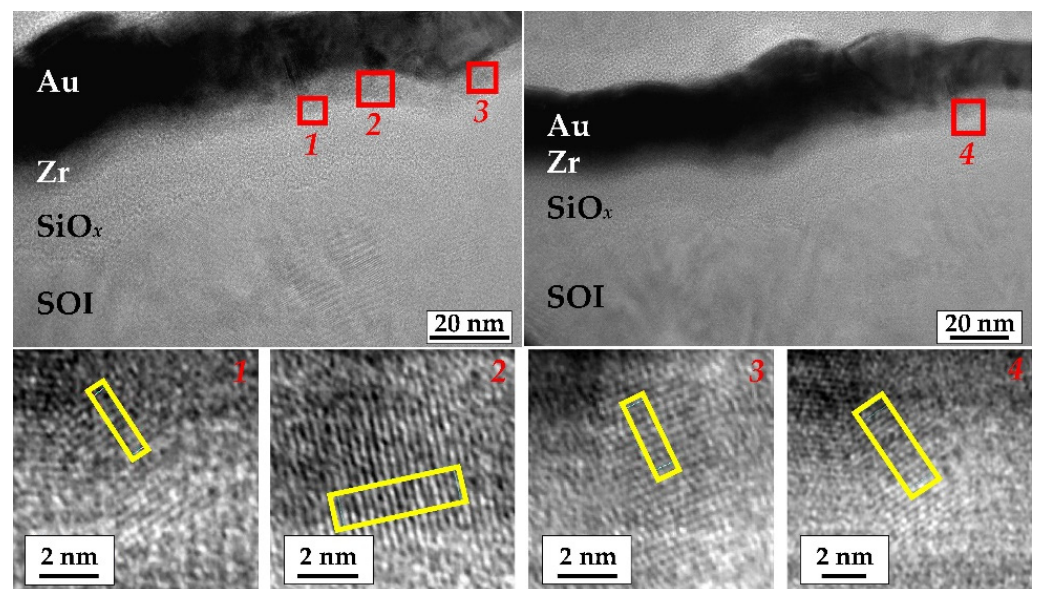


Figure 4. High-resolution TEM images of two cross-sectional regions of a SiO_x -based memristive structure after LT and TT. The inset shows scaled images of the nanocrystallites (parts that were used to determine the interplanar spacing are highlighted by yellow rectangles).

The SiO_x -based memristive structures before LT and TT did not require electroforming [59], since initially they had a conductive state (Figure 5a, curve 1). When a voltage of -6 V was applied, the memristive structure switched from LRS to HRS (Figure 5a, curve 2). Subsequent application of voltage of $+6$ V did not lead to switching of the structure (Figure 5a, curve 3). In the absence of switching (Figure 5a, curves 1 and 3), the values

of the current through the device in the forward and reverse directions of the voltage sweep hardly differed.

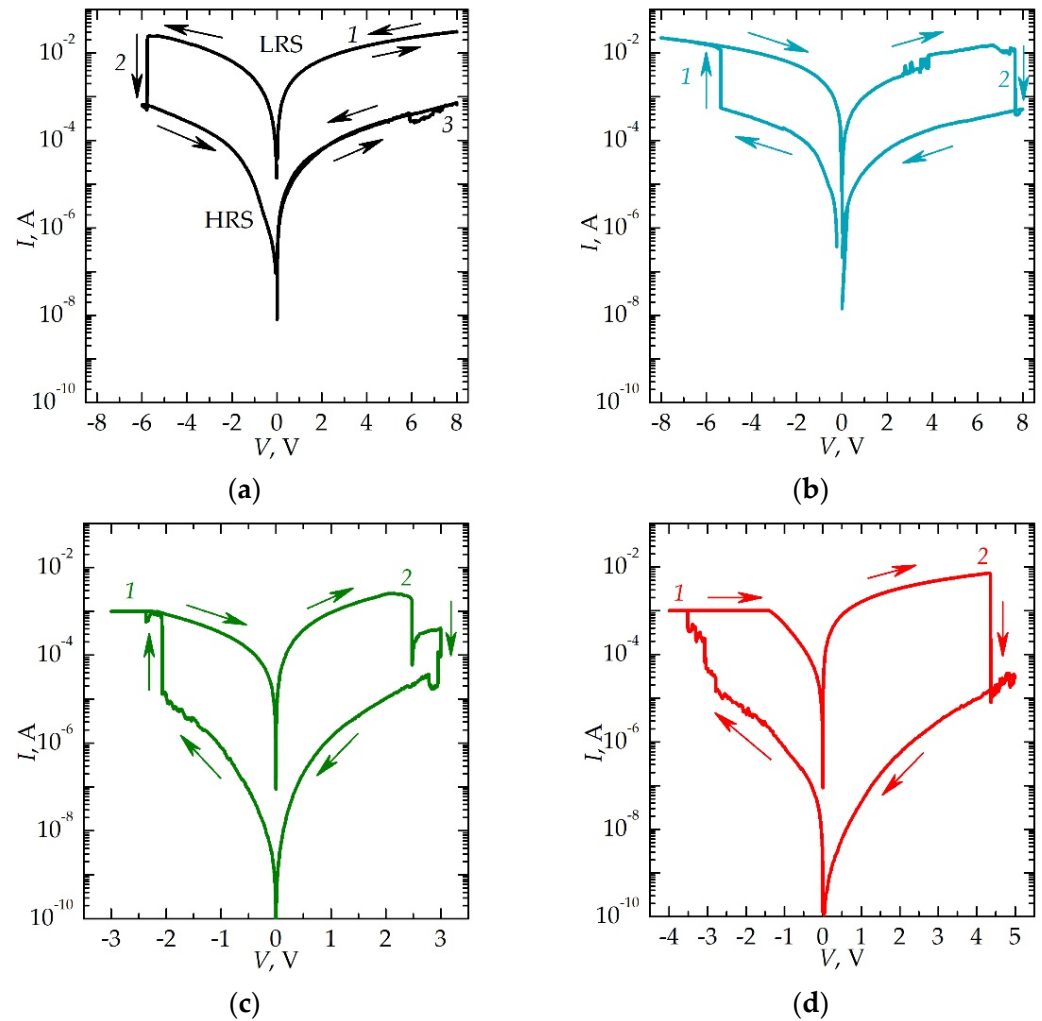


Figure 5. I – V curves of SiO_x -based memristive structure (a) before LT and TT, (b) after LT, (c) after TT and (d) after multiple RS. In the absence of switching (Figure 5a, curves 1 and 3), the values of the current through the device in the forward and reverse directions of the voltage sweep almost did not differ. The direction of the voltage sweep is shown by arrows.

The frequency dependences of the parameters of equivalent circuit of memristive structures in IS (i.e., for curve 1 in Figure 5a) and HRS (i.e., for curve 2 in Figure 5a) are shown in Figure 6. The structure in IS is characterized by large ohmic losses at a low frequencies (Figure 6, curves 2, 3) and a low parallel resistance R_p shunting the structure (Figure 6, curve 5). After switching into HRS, the losses decreased by three orders of magnitude (Figure 6, curves 7, 8), and the value of R_p , respectively, increased by three orders of magnitude (Figure 6, curve 10).

Note that the values of the relative permittivity of SiO_x films calculated from the value of C_p by the equation for a parallel plate capacitor at a frequency of 1 kHz do not change with RS, while the value of $\text{tg}\delta$ changes by three orders of magnitude. This behavior of low-signal HF parameters indicates the filamentary mechanism of RS [60]. In this case, the active part of the film impedance changes locally, i.e., on a small (compared to the total electrode area) memristor area, while the resistance and dielectric losses remain almost unchanged for the rest of the film under the electrode.

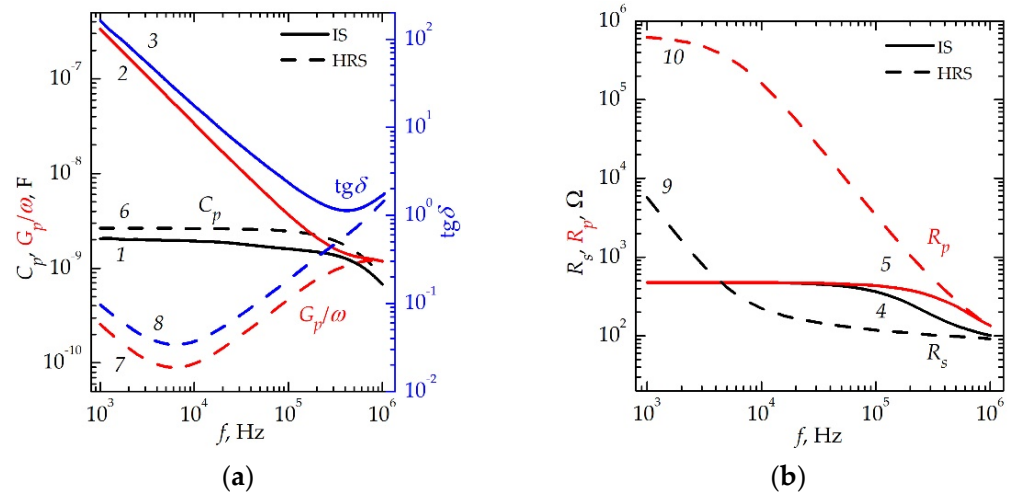


Figure 6. Frequency dependences of (a) C_p (1, 6), G_p/ω (2, 7), $\text{tg}\delta$ (3, 8) and (b) R_s (4, 9), R_p (5, 10) obtained for memristive structure in IS (1–5) and HRS (6–10).

Dependences of C_p and G_p/ω on V (Figure 7) show that the semiconductor corresponds to the n -type, since the capacitance at a frequency of 100 kHz (see inset in Figure 7b) is in the form of a step with an increase towards the voltage $V > 0$ [56]. The concentration of equilibrium electrons in a silicon electrode can be estimated using the following equation [61]:

$$N_D = \frac{2(2\phi_0 - \frac{kT}{q})}{\epsilon_s \epsilon_0 q} \cdot \left(\frac{\frac{C_{ox}}{C_{min}} - 1}{C_{ox}} \right)^{-2}, \quad (3)$$

where N_D is the donor concentration in the semiconductor, ϕ_0 is the height of the potential barrier at the insulator/semiconductor interface, ϵ_s is the relative permittivity of the semiconductor, ϵ_0 is the vacuum permittivity, C_{ox} is the oxide capacity, equal to the maximum value of capacity in Figure 7b in the dark, and C_{min} is the minimum value of capacity in Figure 7b in the dark. The obtained value varied in the range of $\sim 3 \times 10^{19} - 3 \times 10^{20} \text{ cm}^{-3}$. This variation is associated with strong fluctuations in capacitance due to the nonuniform distribution of impurities over the thickness of the silicon electrode.

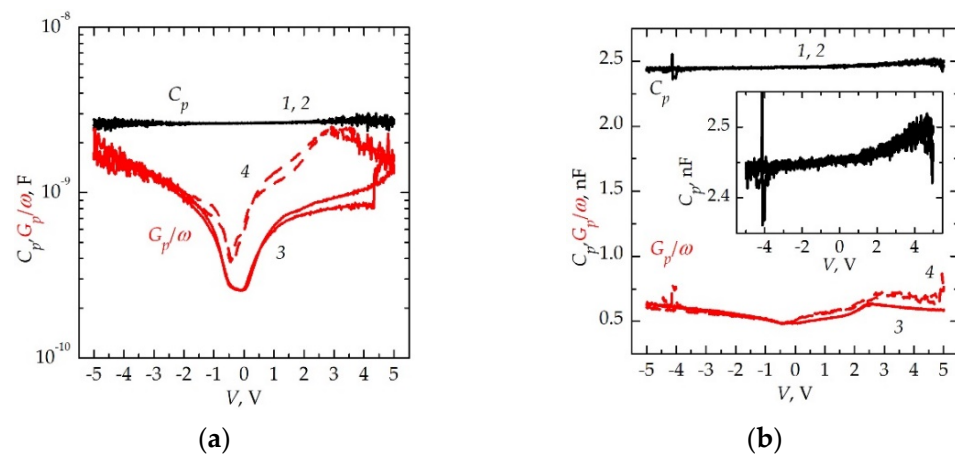


Figure 7. Dependences of C_p (1, 2) and G_p/ω (3, 4) on V measured at a frequency of a small test signal (a) 10 and (b) 100 kHz and in the dark (1, 3) or under laser radiation (2, 4). Voltage sweep from -5 V to $+5 \text{ V}$ and vice versa.

The maxima in the dependences of G_p/ω on V (Figure 7a, curve 4 and Figure 7b, curves 3 and 4) in the theory of MIS structures are usually associated with SS at the

insulator/semiconductor interface. If one assumes a quasicontinuous SS distribution, the N_{ss} value can be estimated using Equation (1). The value of N_{ss} is, under laser radiation, $-3.6 \cdot 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ (at a frequency of 10 kHz) and $1.1 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ (at a frequency of 100 kHz), and in the dark $-1 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ (at a frequency of 100 kHz). Thus, the density of SS on the conductive Si electrode is large and increases with decreasing frequency and under laser radiation. The capture of carriers to these states should decrease the response time of memristors in the same way as a large series resistance.

Figure 5b shows the I - V curves of a memristive structure after LT. It can be seen that LT leads to a change in the polarity of RS: applying a negative voltage leads to the switching of the structure in LRS, and applying a positive voltage leads to the switching of the structure in HRS. Similar behavior was observed in AZO/CeO₂/ITO/glass memory devices [62]. The effect can be explained in terms of the change in the active electrode of the structure, which plays the main role in the formation and oxidation of the filament; however, this requires additional investigation. The obtained I - V curves demonstrate a ratio of currents in LRS and HRS of more than 2 orders of magnitude.

The results of the effect of LT on electrical characteristics of memristive structure are shown in Figure 8. Frequency dependences of the parameters of equivalent circuit of the structure in LRS (i.e., after curve 1 in Figure 5b) and HRS (i.e., after curve 2 in Figure 5b) are shown. These data also indicate a change in the polarity of RS after LT and an almost unchanged value of the resistance of the bottom semiconductor electrode ($\sim 100 \Omega$). In addition, higher values of $\text{tg}\delta$ in HRS at a low frequency, as compared to structures before LT (Figure 6a), indicate incomplete oxidation of filaments.

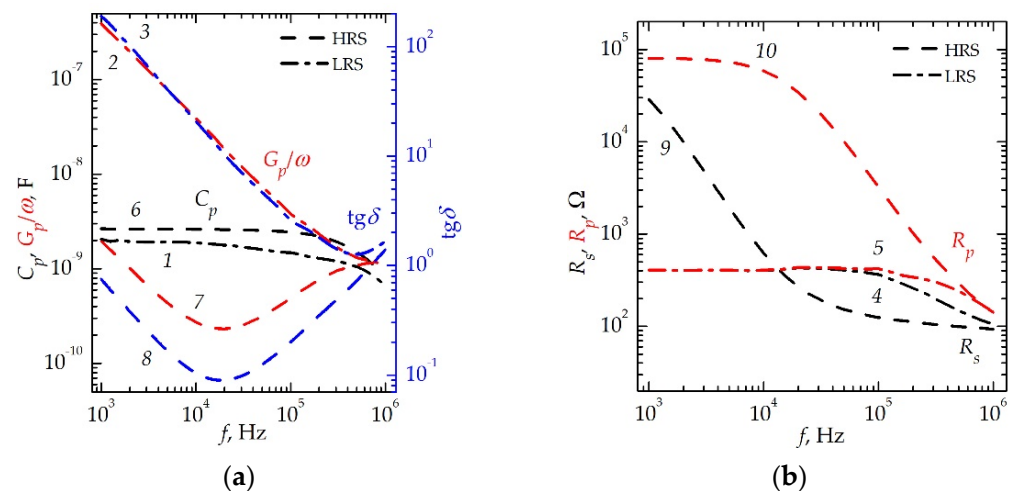


Figure 8. Frequency dependences of (a) C_p (1, 6), G_p/ω (2, 7), $\text{tg}\delta$ (3, 8) and (b) R_s (4, 9), R_p (5, 10) obtained for memristive structure in LRS (1–5) and HRS (6–10). The data were obtained after LT.

TT in a dried atmosphere at 540 K in a hermetically closed metal thermostat also changes the electrical characteristics of SiO_x-based memristive structures. This is evidenced by the frequency dependences of the parameters of equivalent circuit shown in Figure 9. Nonstandard behavior of dielectric losses and the value of parallel resistance with an increase in temperature from 77 to 540 K are noteworthy. Namely, usually, with an increase in the temperature, the concentration of free carriers in the insulator increases, so the values of $\text{tg}\delta$ [63] increase and those of R_p decrease. However, in this case, the values show the opposite tendency. The observed behavior is unusual for insulators and is probably associated with an irreversible change in the properties of the insulator because of TT. The polarity of RS after TT corresponds to the polarity after LT (Figure 5c). It should be noted that the RS voltage decreases after the TT of the structures.

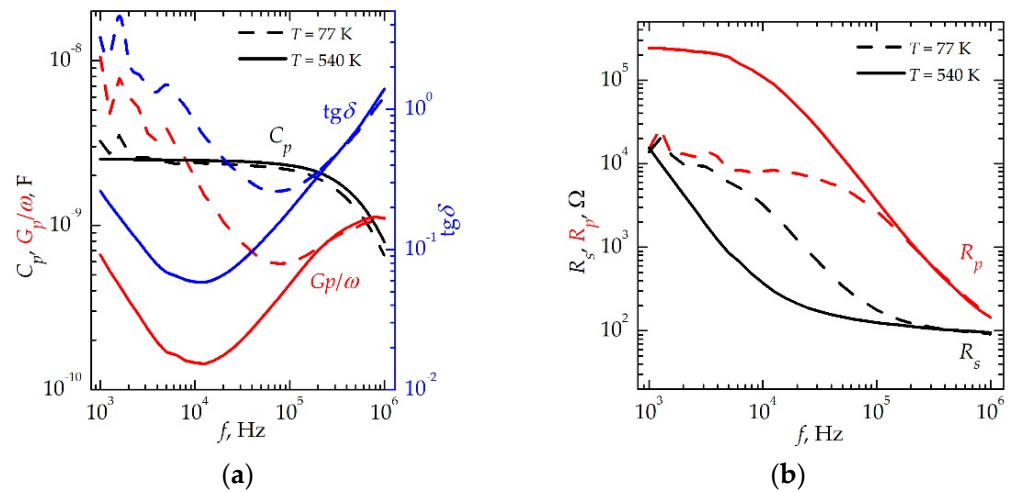


Figure 9. Frequency dependences of (a) C_p , G_p/ω , $\text{tg}\delta$ and (b) R_s , R_p of memristive structure in HRS obtained at a temperature of 77 (dashed line) and 540 K (solid line).

Figure 10 shows the results of studying the stability of the parameters of equivalent circuit and RS parameters of memristive structures after TT under multiple switching in the mode of I – V curve, shown in Figure 5c. The experiment was carried out as follows. After switching the structure in LRS (i.e., for curve 1 in Figure 5c), the frequency dependences of the parameters of equivalent circuit were measured. Furthermore, after switching the structure in HRS (i.e., for curve 2 in Figure 5c), the frequency dependences of the parameters of equivalent circuit were measured again. Thus, multiple (within ~ 2 h) switching of memristive structure from LRS to HRS and vice versa occurred, with sequential measurement of the parameters of equivalent circuit. The times for which the parameters of equivalent circuit were measured were significantly shorter than the time intervals between switches. Therefore, changes in the parameters during the testing of structures could be neglected. Thus, the observed changes in parameters occur due either to the stochasticity of RS processes, or, less likely, to changes in structures in the intervals between switching.

Figure 10a,b shows that the parameters of equivalent circuit after switching into HRS are relatively reproducible in comparison with the parameters obtained after switching into LRS; this is indicated by the weak time dependence of C_{p0} , R_{p0} , and $\text{tg}\delta_0$ (Figure 10a,b, curves 2, 4, 6). When switching into LRS, the time dependences of C_{p0} , R_{p0} , and $\text{tg}\delta_0$ are characterized by non-monotonic behavior, which is reflected in significant (by more than two orders of magnitude for R_{p0} and $\text{tg}\delta_0$) chaotic changes (Figure 10a,b, curves 1, 3, and 5). The last result can be interpreted as follows. The selected mode of switching into HRS allows each time to destroy the active filament, and each switching into LRS leads to the formation of different (in terms of shape and location) filaments. It should be noted that, with multiple switching, regardless of the sign of the switching voltage and the state of the memristive structure, a monotonic decrease in the series resistance $R_{s\infty}$ from $\sim 650 \Omega$ to $\sim 160 \Omega$ was observed (Figure 10b, curve 7). It should be recalled that the value of series resistance is determined by the resistance of the semiconductor electrode. The observed behavior indicates the occurrence of electrochemical reactions on the semiconductor electrode and the accumulation of a positive charge on its surface during the recharging of the memristive structure.

Figure 10c,d shows the results of a statistical study for 10 I – V curves of memristive structures after TT. It can be seen that the currents through the structure in LRS and HRS differ by at least one order of magnitude (Figure 10c), and the voltages for RESET (switching from LRS to HRS, V_{RESET}) and SET (switching from HRS to LRS, V_{SET}) processes have a value in the selected range (Figure 10d).

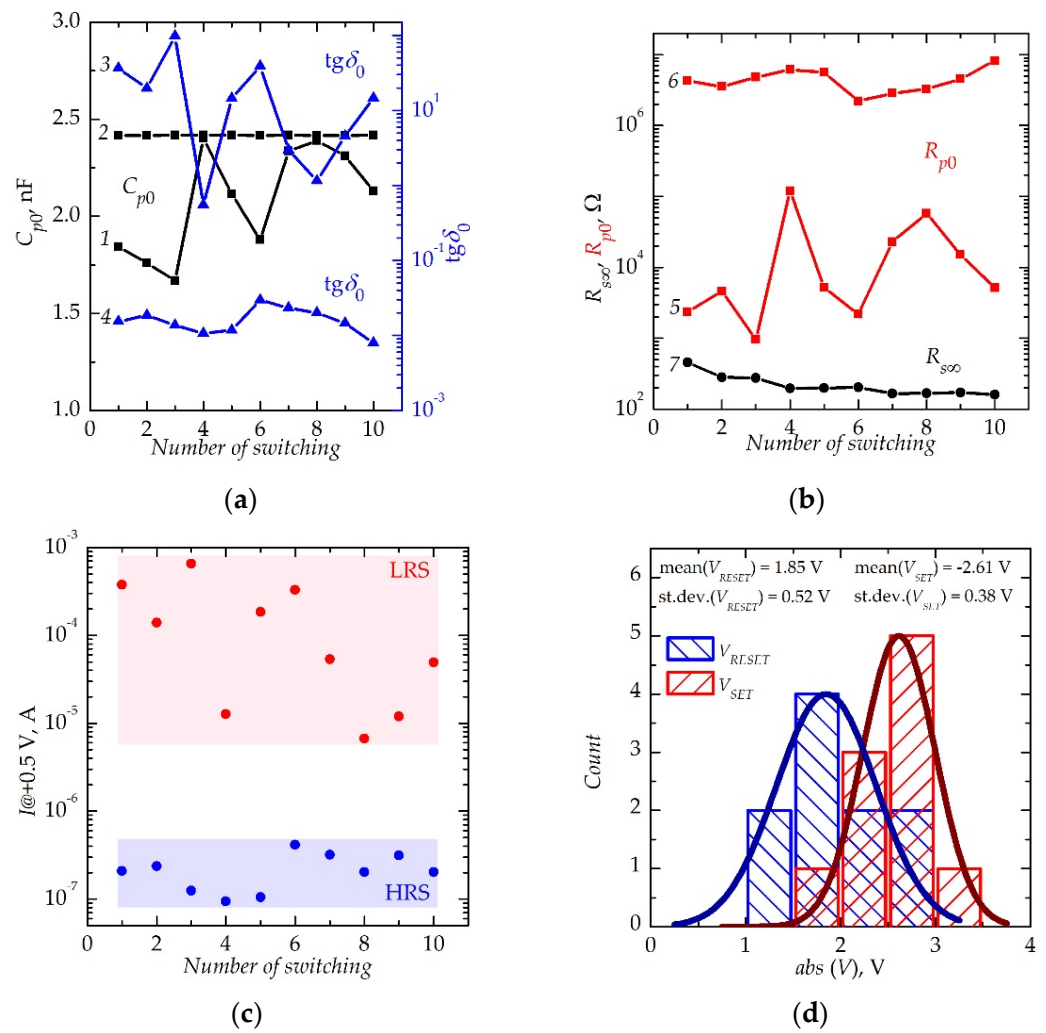


Figure 10. (a,b) The parameters of equivalent circuit of memristive structure after TT and switching into LRS (1, 3, 5) and HRS (2, 4, 6) obtained at a frequency of a small test signal of 1 kHz (C_{p0} , $\text{tg}\delta_0$, R_{p0}) and 2 MHz (R_{∞}); (c) dependences of the currents (at a reading voltage of +0.5 V) of memristive structure in LRS (red) and HRS (blue) after TT on the number of RS cycles; (d) distribution of voltages of SET (red) and RESET (blue) processes of memristive structure after TT.

Figure 5d shows the I – V curves of memristive structures after multiple RS. An increase in the voltage values of RESET and SET processes is seen, which indicates a significant change in electrical characteristics of the structure under multiple RS.

Figure 11 shows the frequency dependences of the parameters of equivalent circuit obtained for the memristive structure in HRS (i.e., for curve 2 in Figure 5d) after multiple switching. It should be emphasized that, in contrast to the dependencies shown above, these data indicate the complete oxidation of filaments when the structure is switched in HRS. This fact is seen, in particular, from a comparison with the frequency dependence of the $\text{tg}\delta$ structure in HRS in a low-frequency region. An increase in the $\text{tg}\delta$ and G_p/ω of the structures (Figure 11a) can be explained by the fact that there is no shunting of memristor by the value of R_p and the implementation of a series connection of the capacitance C_p and memristor electrodes. In this case, the losses at low frequencies are small, the parallel capacitance is equal to the series capacitance, and the series resistance is determined by the resistance of the semiconductor electrode ($\sim 170 \Omega$).

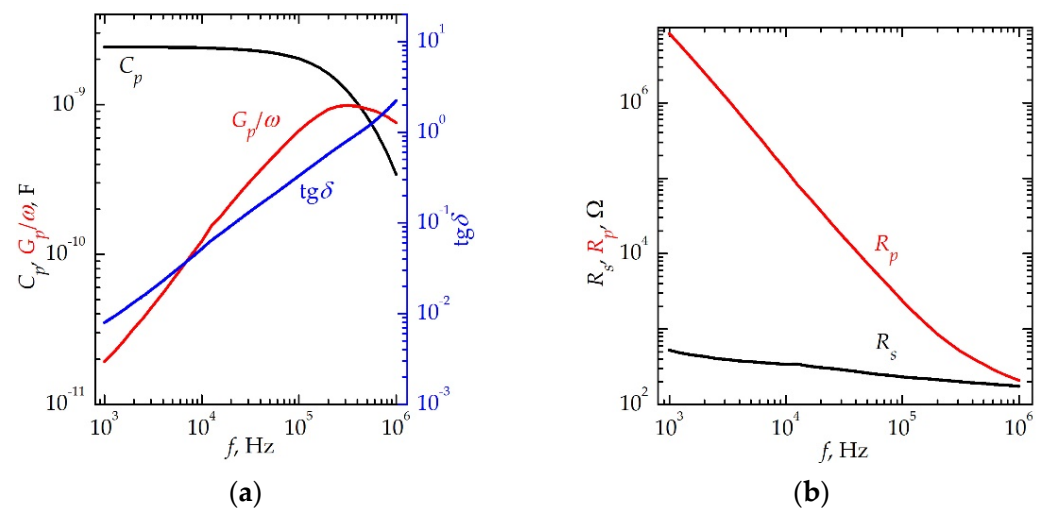


Figure 11. Frequency dependences of (a) C_p , G_p/ω , $\text{tg}\delta$ and (b) R_s , R_p of memristive structure in HRS after multiple RS.

For a quantitative comparison, Table 1 shows the values of C_p , G_p/ω , $\text{tg}\delta$, R_p , and R_s , obtained at the frequencies of 1 and 100 kHz (indices 0 and ∞ , respectively). Data were obtained for the SiO_x -based memristor in different resistive states before LT and TT, after LT, during TT, and after multiple RS.

Table 1. SiO_x -based memristor equivalent circuit parameters.

Treatment	Resistive State	C_{p0} , nF	$C_{p\infty}$, nF	G_{p0}/ω , nF	$G_{p\infty}/\omega$, nF	$\text{tg}\delta_0$	$\text{tg}\delta_\infty$	R_{p0} , Ω	$R_{p\infty}$, Ω	R_{s0} , Ω	$R_{s\infty}$, Ω
Before LT and TT	IS	2.05	1.60	334	3.68	163	2.30	476	433	476	364
	HRS	2.65	2.46	0.26	0.47	0.10	0.19	621,296	3400	5732	119
After LT	LRS	2.06	1.49	390	3.78	189	2.54	409	422	409	365
	HRS	2.65	2.45	1.98	0.49	0.75	0.20	80,309	3253	28,806	125
During TT	HRS at 77 K	3.24	2.17	11	0.59	3.24	0.27	15,124	2701	13,812	179
	HRS at 540 K	2.52	2.31	0.66	0.44	0.26	0.19	241,206	3637	15,457	126
After multiple RS	HRS	2.42	2.02	0.02	0.66	0.01	0.33	8,259,960	2396	525	234

Figure 12 shows the Cole–Cole diagrams obtained for SiO_x -based memristive structures in HRS. The data were obtained from the frequency dependences of the G_p/ω and C_p of memristive structure before LT and TT (see Figure 6a), after LT (see Figure 8a), and after TT and multiple switching (Figure 11a). It can be seen that all diagrams have a circular arc shape, i.e., the spectrum of SS at insulator/semiconductor interface is continuous in all cases. The values of N_{ss} were estimated using Equation (1) and are 1.9×10^{12} , 1.8×10^{12} , and $1.5 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$, respectively.

Thus, only the LT of the $\text{Au/Zr/SiO}_x/\text{SOI}$ memristive structures is not sufficient for a significant change in the value of the density of SS. Additional use of TT leads to a decrease in this value by a factor of ~ 1.3 . Nevertheless, the combined effect of LT and TT on the $\text{Au/Zr/SiO}_x/\text{SOI}$ memristive structures results in a decrease in RS voltages of almost 2-fold. The effect is probably associated with the annealing of SS, which, in turn, leads to a decrease in the resistance of the structure. According to the model [64], the appearance of SS is associated with the disordering of silicon subsurface near the interface with the insulator. From this point of view, annealing promotes a decrease in the density of SS due to the relaxation of this disorder. However, one should also consider that annealing can lead

to a change in the concentration of electrically active impurities in both the semiconductor and the insulator. As a result, the Fermi level at the insulator/semiconductor interface can shift towards a lower density of states.

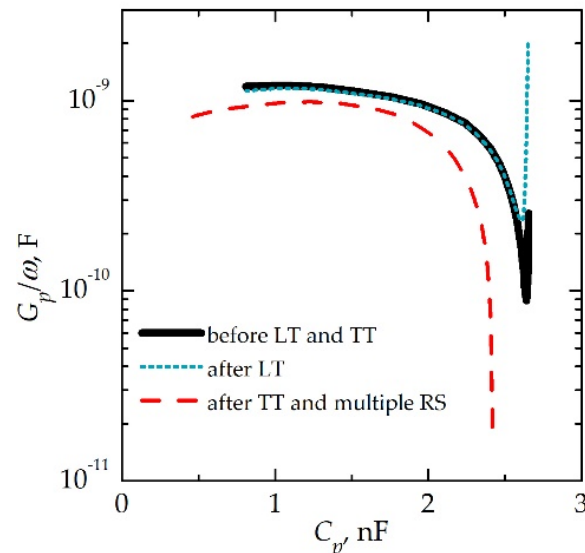


Figure 12. The Cole–Cole diagrams obtained for SiO_x -based memristive structures in HRS. The data were obtained before LT and TT, after LT, and after TT and multiple RS.

It should be noted that, along with the abovementioned influence of treatments on the density of SS, they can be responsible for the occurrence of RS. It can be assumed that the nanocrystallites observed by TEM are responsible for the initial conductive state of SiO_x -based memristors. According to the estimates from TEM images, nanocrystallites reach diameters of ~ 7 nm. Note that TEM studies were carried out after LT and TT. Thus, probably, such treatments led to significant and irreversible oxidation of nanocrystallites and, before treatments, the sizes of nanocrystallites could be comparable to the thickness of the insulator film. The latter could lead to shunting the devices. This explanation is indirectly confirmed by the unusual behavior of dielectric losses and the value of parallel resistance, with an increase in temperature from 77 to 540 K.

3.2. SiN_x -Based Memristive Structures on SOI Substrates

According to AFM data (Figure 13a), the root mean square roughness of the SiN_x film is 1.9 nm. In Figure 13b, XPS data for SiN_x film before and after annealing at 550 K are reported. It is shown that the stoichiometry of SiN_x film before and after annealing hardly changes and $x \approx 1.25$. One can also notice the presence of a transition layer at the SiN_x/SOI interface, the thickness of which is ~ 18 nm.

In Figure 14, the TEM images of a cross section of SiN_x -based memristive structures after LT are shown. According to Figure 14, the SiN_x film has an amorphous structure. At the same time, the presence of ZrN (areas 1, 3, 5–7) and Si (area 4) nanocrystallites is confirmed inside amorphous SiN_x . ZrO_2 (area 2), ZrO (area 8), and ZrN (area 9) nanocrystallites are found in the Zr sublayer and at the interface with the insulator. The presence of Si_3N_4 nanocrystallites should also be noted (area 10). The structure of the observed nanocrystallites was determined by comparing the interplanar spacing in TEM images with the literature data. Like for the SiO_x -based memristive structures, the SiN_x -based structures considered in this section initially had a conductive state. It should be noted that SiN_x -based memristive structures did not demonstrate RS before LT (Figure 15a, curve 1).

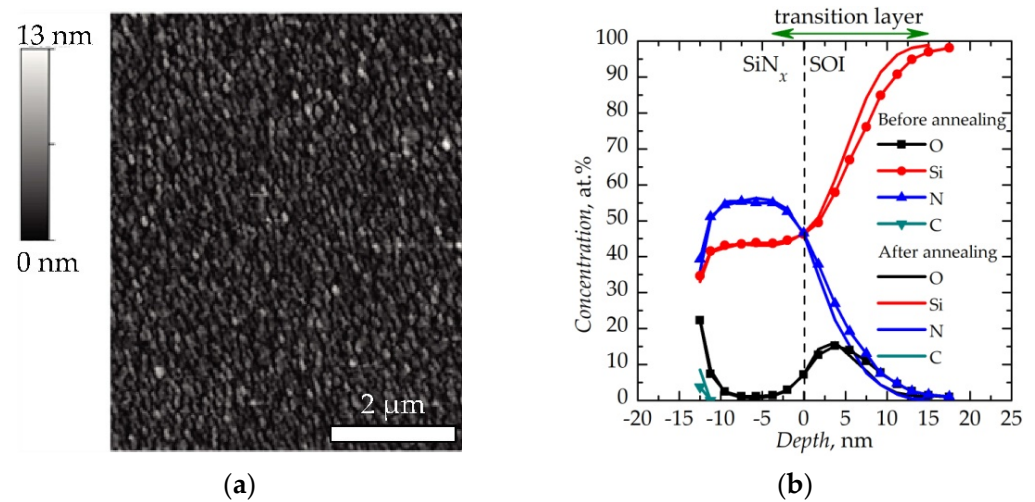


Figure 13. (a) AFM image of SiN_x film surface; (b) distribution of chemical elements over depth of SiN_x film before and after annealing at 550 K. The origin of coordinates along the abscissa coincided with the SiN_x /SOI interface.

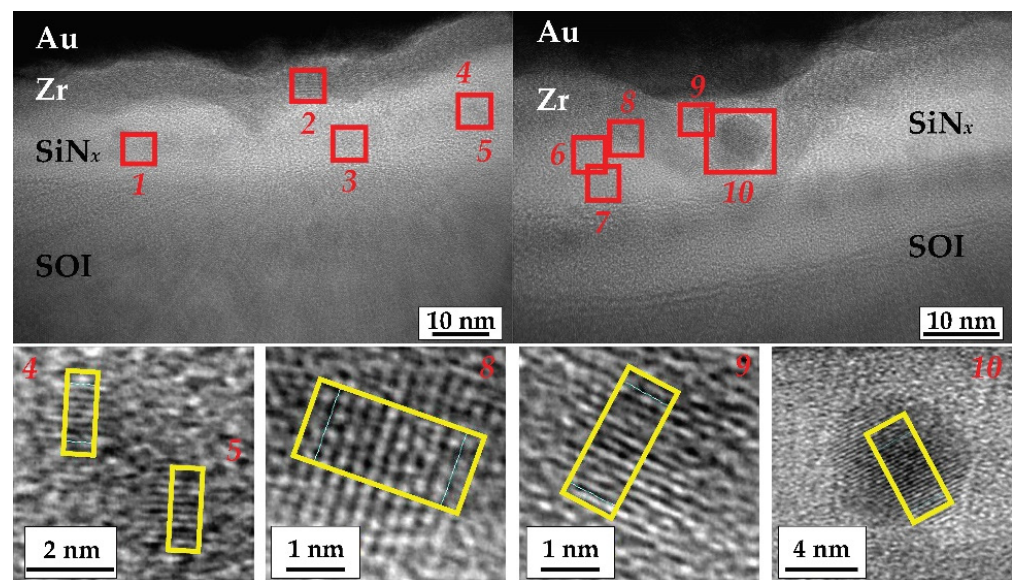


Figure 14. High-resolution TEM images of two cross-sectional regions of SiN_x -based memristive structure after LT. The inset shows scaled images of the nanocrystallites (parts that were used to determine the interplanar spacing are highlighted by yellow rectangles).

In Figure 16, the frequency dependences of the parameters of equivalent circuit of memristive structure before LT are shown. The series resistance in the structure at a high frequency, which, as determined by the resistance of memristor electrodes, is $\sim 110 \Omega$.

In the theory of MIS structures, using high-frequency $C-V$, it is possible to determine the type of dopant: as a DC sweep voltage is applied to the metal, a positive slope of $1/C^2$ vs. V indicates acceptors and a negative slope indicates donors [65,66]. The $1/C^2$ value increases with increasing absolute voltage value (Figure 17), which indicates the n -type conductivity of the semiconductor film. The nonlinearity of this dependence can be a consequence of inhomogeneous doping of the semiconductor film.

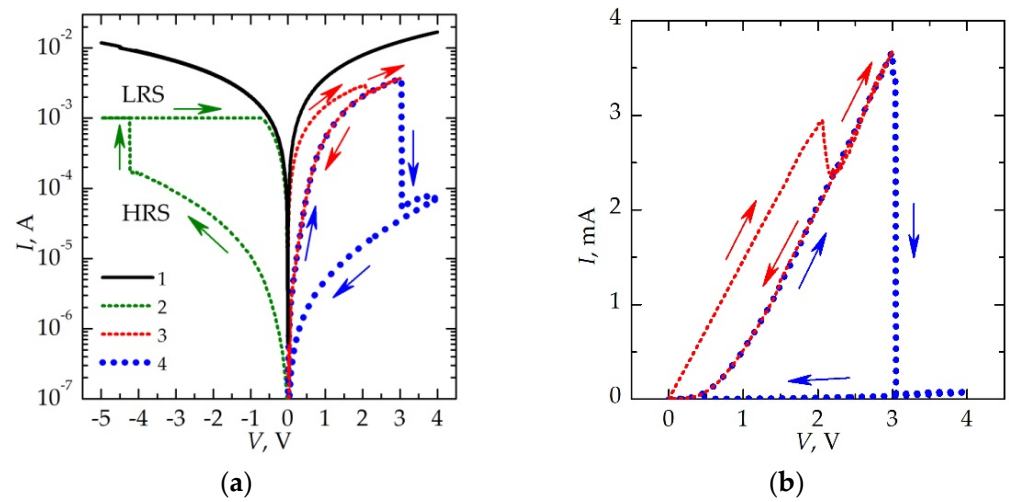


Figure 15. (a) I - V curves of SiN_x -based memristive structure before (solid line) and after (dotted line) LT in semi-log plot. Curves 3 and 4 in linear plot (b). The direction of the voltage sweep is shown by arrows.

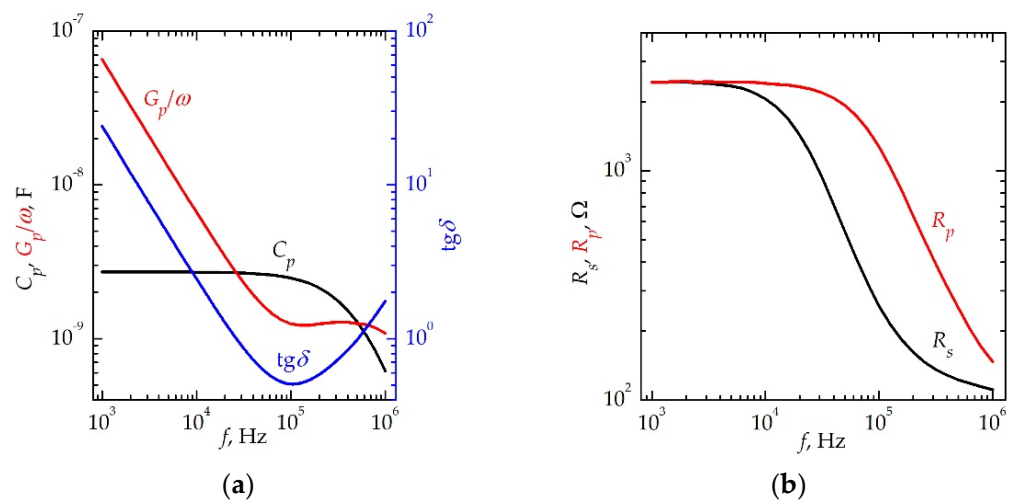


Figure 16. Frequency dependences of (a) C_p , G_p/ω , $\text{tg}\delta$ and (b) R_s , R_p obtained for memristive structure before LT.

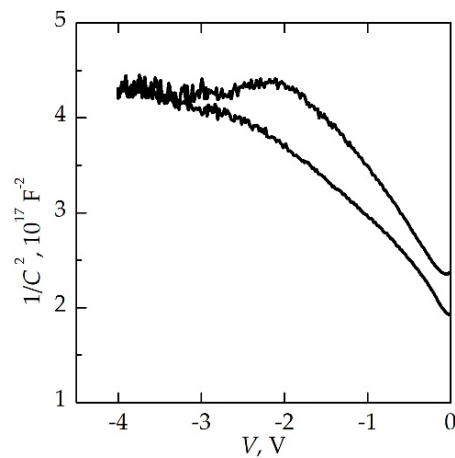


Figure 17. Dependence of nonequilibrium capacitance on voltage in coordinates $1/C^2$ - V obtained for memristive structure before LT. Data were measured at a small test signal frequency of 100 kHz.

The donor concentration N_D can be estimated using the slope of the straight line, which extrapolates the data in Figure 17, and the following equation [56]:

$$N_D = \frac{2}{\epsilon_s \epsilon_0 q S^2} \frac{\Delta V}{\Delta \frac{1}{C^2}}. \quad (4)$$

The N_D value is $\sim 5 \times 10^{18} \text{ cm}^{-3}$. It should be noted that the obtained value is probably underestimated due to the presence of horizontal areas in the dependence.

The frequency dependence of the parameters of the equivalent circuit shows almost no changes when measured in the dark and under short-term laser radiation. This indicates the presence of an electron-enriched layer at the insulator/semiconductor interface. Therefore, like for the SiO_x -based memristive structures considered above, the structures based on SiN_x were subjected to LT in air in order to change the charge state of the traps in SiN_x . Figure 15a (curves 2–4) shows I – V curves demonstrating a significant increase in the hysteresis loop (change in the current by ~ 3 orders of magnitude) after LT of the structures. It should be noted that the structures also demonstrated a synaptic nature of switching (Figure 15b) [67,68]. After LT, memristive structures showed an increased value of the relative permittivity (before LT, it was 4; after, it was ~ 4.85). This value was calculated using the equation for a parallel plate capacitor at a frequency of 1 kHz. This behavior indicates the contribution of the space charge region in the semiconductor electrode to the capacitance of the capacitor before LT.

The effect of LT on the electrical characteristics of the memristive structure is illustrated in Figure 18. Frequency dependences of the parameters of equivalent circuit of the structure in LRS (i.e., for curve 2 in Figure 15a) and in HRS (i.e., for curve 4 in Figure 15a) after LT are shown.

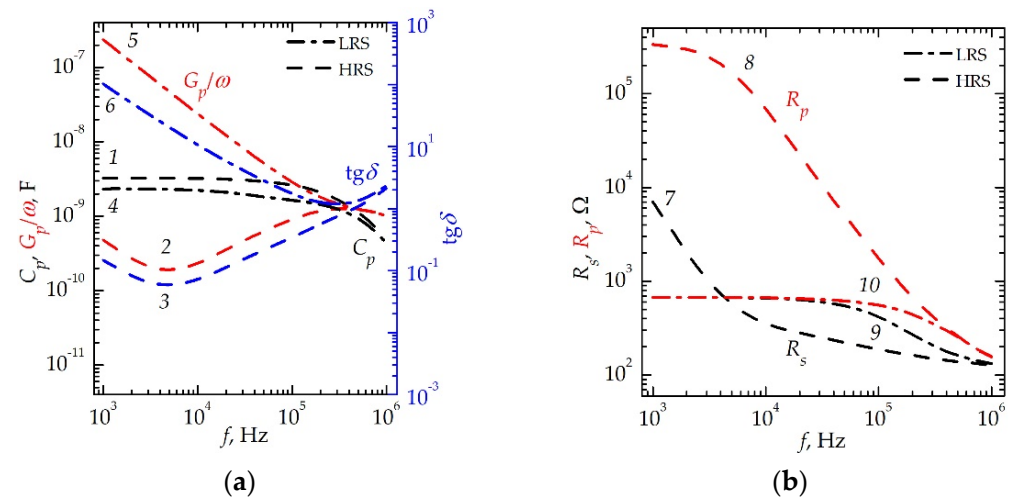


Figure 18. Frequency dependences of (a) C_p (1, 4), G_p/ω (2, 5), $\text{tg } \delta$ (3, 6) and (b) R_s (7, 9), R_p (8, 10) obtained for memristive structure in LRS (4, 5, 6, 9, 10) and HRS (1, 2, 3, 7, 8). The data were obtained after LT.

It is worth noting the presence of large losses in the structures after switching into LRS with a voltage of -5 V , which is probably due to the presence of filaments; at the same time, the losses in the structure were significantly reduced (at a low frequency up to two orders of magnitude) after switching into HRS with a voltage of $+4 \text{ V}$. However, there was no complete destruction of filaments. This was indicated by the presence of losses at a frequency of $< 10^4 \text{ Hz}$, which are characterized for losses due to leakage currents at low frequencies [55]. Also, in the memristive structure in HRS at a low frequency, the parallel resistance increased (up to 2 orders of magnitude), shunting it. In this case, the resistance of the silicon electrode remained almost unchanged.

For a quantitative comparison, Table 2 shows the values of C_p , G_p/ω , $\text{tg}\delta$, R_p , and R_s obtained at the frequencies of 1 and 100 kHz (indices 0 and ∞ , respectively). Data were obtained for the SiN_x -based memristor in different resistive states before and after LT.

Table 2. SiN_x -based memristor equivalent circuit parameters.

Treatment	Resistive State	C_{p0} , nF	$C_{p\infty}$, nF	G_{p0}/ω , nF	$G_{p\infty}/\omega$, nF	$\text{tg}\delta_0$	$\text{tg}\delta_\infty$	R_{p0} , Ω	$R_{p\infty}$, Ω	R_{s0} , Ω	$R_{s\infty}$, Ω
Before LT	IS	2.71	2.48	65	1.25	24	0.50	2436	1276	2432	258
After LT	LRS	2.30	1.64	236	2.86	102	1.74	675	558	675	419
	HRS	3.26	2.61	0.48	0.90	0.15	0.35	334,200	1764	6992	188

Figure 19 shows the Cole–Cole diagrams obtained for SiN_x -based memristive structures. The data were obtained from the frequency dependences of the G_p/ω and C_p of memristive structure before LT (see Figure 16a) and after LT (see Figure 18a). Note that the memristive structure did not demonstrate resistive switching before laser treatment; therefore, the diagram for this case was obtained in the initial highly conductive state of memristive structure. At the same time, after LT, the two resistive states of memristive structure became distinguishable; therefore, the diagram for the second case was obtained under the conditions of HRS of the memristive structure.

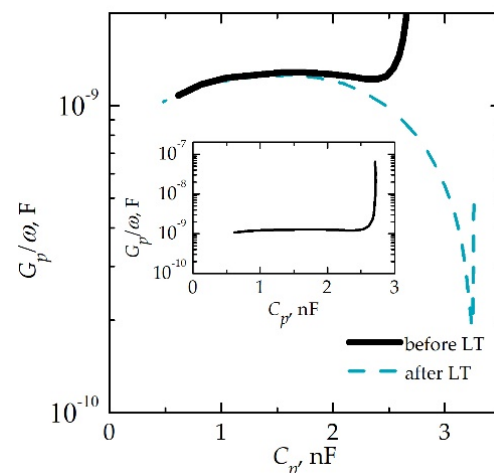


Figure 19. The Cole–Cole diagrams obtained for SiN_x -based memristive structures. The data were obtained before and after LT. Inset: same Cole–Cole diagram as before LT, but at full scale.

In the first case (before LT), the diagram had a circular arc shape, which indicates a uniform spectrum of SS at the insulator/semiconductor interface. The value of N_{ss} was estimated using Equation (1) and is equal to $1.6 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$. SS with such a high-density value can reduce response times and contribute to the variability in RS voltage values. The sharp increase in G_p/ω at high values of C_p is due to the presence of conductive channels (see inset in Figure 19). In the second case (after LT), the shape of the diagram is close to a semicircle, which indicates the presence of a mono-level of SS. The value of N_{ss} , estimated using Equation (2), was $1.5 \times 10^{11} \text{ cm}^{-2}$, which is an order of magnitude lower than before LT.

Figure 20a,b shows the results of a statistical study for 10 I – V curves of memristive structures after LT. It can be seen that the currents through the structure in LRS and HRS differ by at least 8-fold (Figure 20a), and the voltages for RESET and SET processes have a value in the selected range (Figure 20b).

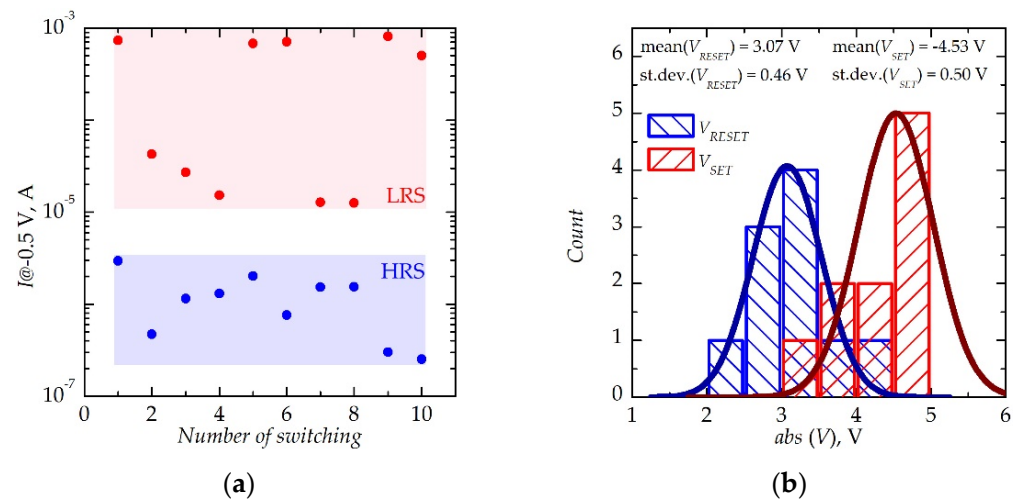


Figure 20. (a) Dependences of the currents (at a reading voltage of -0.5 V) of memristive structure in LRS (red) and HRS (blue) after LT on the number of RS cycles; (b) distribution of voltages of V_{SET} (red) and V_{RESET} (blue) processes of memristive structure after LT.

Thus, one can conclude that LT leads to a change in the spectrum of SS at the SiN_x/SOI interface. This is probably due to the more significant, in comparison with SiO_x -based structures, effect of LT on the charge state of traps in SiN_x , which determine the conductivity with the optical activation energy (for $\text{SiN}_{x < 4/3}$, this value is equal to 2.6 eV [69]). It was reported in [70] that these traps can play a decisive role in the rupture and restoration of filaments during switching in SiN_x -based memristors. Therefore, LT is an effective method for changing RS parameters in metal/ SiN_x /semiconductor memristive structures.

It should be noted that, along with the abovementioned influence of LT on the spectrum of SS, it can be responsible for the occurrence of RS. It can be assumed that the nanocrystallites observed by TEM are responsible for the initial conductive state of SiN_x -based memristors. According to the estimates from TEM images, nanocrystallites reach diameters of $\sim 5\text{--}10\text{ nm}$. Note that TEM studies were carried out after LT. Thus, probably, such treatment led to significant and irreversible oxidation of nanocrystallites and, before LT, the sizes of nanocrystallites could be comparable to the thickness of the insulator film. The latter could lead to shunting the devices.

4. Conclusions

This work demonstrates the robustness of the memristive phenomenon in thin-film structures based on promising and accessible insulator layers— SiO_x and SiN_x —fabricated on SOI substrates and subjected to additional laser and thermal treatments. It was shown that laser treatment leads to a significant increase in the hysteresis loop in $I\text{--}V$ curves of the $\text{Au/Zr/SiN}_x/\text{SOI}$ memristive structures. The effect was explained by the positive charging of traps in the insulator and a decrease in the density of surface states at the insulator/semiconductor interface (by an order of magnitude). Moreover, laser treatment of the $\text{Au/Zr/SiO}_x/\text{SOI}$ memristive structures was not sufficient to produce a significant change in the value of the density of the surface states. Additional use of thermal treatment led to a decrease in this value by a factor of ~ 1.3 . Furthermore, the combined effect of laser treatment followed by thermal treatment on the $\text{Au/Zr/SiO}_x/\text{SOI}$ memristive structures led to a near doubling of the resistive switching voltages. The effect was, probably, associated with the annealing of surface states, which, in turn, led to a decrease in the resistance of the structure.

The CMOS compatibility of memristive devices in our study was provided by two factors. First, it is a SOI substrate, which is used in the technology of integrated circuits, including radiation-resistant ones. Secondly, it is a switching layer material, which is also fabricated using industrial technology. In this sense, the top electrode is of no fundamental

importance, since in the framework of BEOL (back-end-of-line) integration it does not affect the basic FEOL (front-end-of-line) process. We chose a composite Au/Zr electrode, since it had previously proven itself well in MIM devices based on SiO_x [71] and is semitransparent, which is important for laser treatment. However, as part of the further optimization of these devices, other combinations of oxidizable and inert metals can be selected and tested.

It should be emphasized that the device layer of silicon in the SOI structure can differ greatly from bulk silicon in terms of structure and surface quality. The latter significantly affects the surface state, which can play an important role in the resistive switching mechanism. Therefore, the use of a SOI substrate in combination with specific switching insulators and additional treatment methods is of fundamental importance.

Author Contributions: Conceptualization, S.V.T. and A.N.M.; methodology, S.V.T. and D.S.K.; software, A.I.B.; validation, M.N.K., D.O.F., D.I.T., A.N.M., S.K. and B.S.; formal analysis, M.N.K., D.O.F. and S.V.T.; investigation, S.V.T., A.I.B., A.V.K., R.N.K., S.Y.Z., V.A.V. and D.A.P.; resources, A.N.M. and S.K.; data curation, M.N.K., D.O.F., S.V.T., A.I.B., D.I.T. and A.N.M.; writing—original draft preparation, M.N.K., D.O.F., S.V.T. and A.I.B.; writing—review and editing, D.I.T., A.N.M., S.A.S., S.K. and B.S.; visualization, M.N.K., S.V.T. and A.I.B.; supervision, D.O.F., D.I.T., A.N.M., S.A.S., S.K. and B.S.; project administration, A.N.M. and S.A.S.; funding acquisition, A.N.M. and S.A.S. All authors have read and agreed to the published version of the manuscript.

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Data Availability Statement: The data that support the findings of this study are available from the corresponding author upon reasonable request.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Zhang, W.; Gao, B.; Tang, J.; Li, X.; Wu, W.; Qian, H.; Wu, H. Analog-type resistive switching devices for neuromorphic computing. *Phys. Status Solidi RRL* **2019**, *13*, 1900204. [\[CrossRef\]](#)
2. Wang, Z.; Joshi, S.; Savel'ev, S.E.; Jiang, H.; Midya, R.; Lin, P.; Hu, M.; Ge, N.; Strachan, J.P.; Li, Z.; et al. Memristors with diffusive dynamics as synaptic emulators for neuromorphic computing. *Nat. Mater.* **2017**, *16*, 101–108. [\[CrossRef\]](#) [\[PubMed\]](#)
3. Slipko, V.A.; Pershin, Y.V. Metastable memristive lines for signal transmission and information processing applications. *Phys. Rev. E* **2017**, *95*, 042213. [\[CrossRef\]](#)
4. Wang, Z.; Joshi, S.; Savel'ev, S.; Song, W.; Midya, R.; Li, Y.; Rao, M.; Yan, P.; Asapu, S.; Zhuo, Y.; et al. Fully memristive neural networks for pattern classification with unsupervised learning. *Nat. Electron.* **2018**, *1*, 137–145. [\[CrossRef\]](#)
5. Pershin, Y.V.; Slipko, V.A. Dynamical attractors of memristors and their networks. *Europhys. Lett.* **2019**, *125*, 20002. [\[CrossRef\]](#)
6. Pershin, Y.V. A demonstration of implication logic based on volatile (diffusive) memristors. *IEEE Trans. Circuits Syst. II Express Briefs* **2019**, *66*, 1033–1037. [\[CrossRef\]](#)
7. Mehonic, A.; Sebastian, A.; Rajendran, B.; Simeone, O.; Vasilaki, E.; Kenyon, A.J. Memristors—From in-memory computing, deep learning acceleration, and spiking neural networks to the future of neuromorphic and bio-inspired computing. *Adv. Intell. Syst.* **2020**, *2*, 2000085. [\[CrossRef\]](#)
8. Serb, A.; Corna, A.; George, R.; Khat, A.; Rocchi, F.; Reato, M.; Maschietto, M.; Mayr, C.; Indiveri, G.; Vassanelli, S.; et al. Memristive synapses connect brain and silicon spiking neurons. *Sci. Rep.* **2020**, *10*, 2590. [\[CrossRef\]](#)
9. Demin, V.A.; Nekhaev, D.V.; Surazhevsky, I.A.; Nikiruy, K.E.; Emelyanov, A.V.; Nikolaev, S.N.; Rylkov, V.V.; Kovalchuk, M.V. Necessary conditions for STDP-based pattern recognition learning in a memristive spiking neural network. *Neural Netw.* **2021**, *134*, 64–75. [\[CrossRef\]](#)
10. Johnson, B.A.; Brahim, K.; Balanov, A.G.; Savel'ev, S.; Borisov, P. Transition from noise-induced to self-sustained current spiking generated by a NbO_x thin film threshold switch. *Appl. Phys. Lett.* **2021**, *118*, 023502. [\[CrossRef\]](#)
11. Ushakov, Y.; Akther, A.; Borisov, P.; Pattnaik, D.; Savel'ev, S.; Balanov, A.G. Deterministic mechanisms of spiking in diffusive memristors. *Chaos Solitons Fractals* **2021**, *149*, 110997. [\[CrossRef\]](#)
12. Du, N.; Zhao, X.; Chen, Z.; Choubey, B.; Di Ventra, M.; Skorupa, I.; Bürger, D.; Schmidt, H. Synaptic plasticity in memristive artificial synapses and their robustness against noisy inputs. *Front. Neurosci.* **2021**, *15*, 696. [\[CrossRef\]](#) [\[PubMed\]](#)

13. Mikhaylov, A.; Belov, A.; Korolev, D.; Antonov, I.; Kotomina, V.; Kotina, A.; Gryaznov, E.; Sharapov, A.; Koryazhkina, M.; Kryukov, R.; et al. Multilayer metal-oxide memristive device with stabilized resistive switching. *Adv. Mater. Technol.* **2020**, *5*, 1900607. [\[CrossRef\]](#)
14. Nikiruy, K.E.; Iliasov, A.I.; Emelyanov, A.V.; Sitnikov, A.V.; Rylkov, V.V.; Demin, V.A. Memristors based on nanoscale layers LiNbO_3 and $(\text{Co}_{40}\text{Fe}_{40}\text{B}_{20})_x(\text{LiNbO}_3)_{100-x}$. *Phys. Solid State* **2020**, *62*, 1732–1735. [\[CrossRef\]](#)
15. Matsukatova, A.N.; Emelyanov, A.V.; Minnekhanov, A.A.; Sakharutov, D.A.; Vdovichenko, A.Y.; Kamyshinskii, R.A.; Demin, V.A.; Rylkov, V.V.; Forsh, P.A.; Chvalun, S.N.; et al. Memristors based on poly(*p*-xylylene) with embedded silver nanoparticles. *Tech. Phys. Lett.* **2020**, *46*, 73–76. [\[CrossRef\]](#)
16. Sun, K.; Chen, J.; Yan, X. The future of memristors: Materials engineering and neural networks. *Adv. Funct. Mater.* **2021**, *31*, 2006773. [\[CrossRef\]](#)
17. La Torre, C.; Fleck, K.; Starschich, S.; Linn, E.; Waser, R.; Menzel, S. Dependence of the SET switching variability on the initial state in HfO_x -based ReRAM. *Phys. Status Solidi A* **2016**, *213*, 316–319. [\[CrossRef\]](#)
18. Ungureanu, M.; Zazpe, R.; Golmar, F.; Stoliar, P.; Llopis, R.; Casanova, F.; Hueso, L.E. A light-controlled resistive switching memory. *Adv. Mater.* **2012**, *24*, 2496–2500. [\[CrossRef\]](#)
19. Patterson, G.A.; Fierens, P.I.; Grosz, D.F. On the beneficial role of noise in resistive switching. *Appl. Phys. Lett.* **2013**, *103*, 074102. [\[CrossRef\]](#)
20. Mikhaylov, A.N.; Guseinov, D.V.; Belov, A.I.; Korolev, D.S.; Shishmakova, V.A.; Koryazhkina, M.N.; Filatov, D.O.; Gorshkov, O.N.; Maldonado, D.; Alonso, F.J.; et al. Stochastic resonance in a metal-oxide memristive device. *Chaos Solitons Fractals* **2021**, *144*, 110723. [\[CrossRef\]](#)
21. Ntinis, V.; Rubio, A.; Sirakoulis, G.C.; Aguilera, E.S.; Pedro, M.; Crespo-Yepes, A.; Martin-Martinez, J.; Rodriguez, R.; Nafria, M. Power-efficient noise-induced reduction of ReRAM cell's temporal variability effects. *IEEE Trans. Circuits Syst. II Express Briefs* **2021**, *68*, 1378–1382. [\[CrossRef\]](#)
22. Ielmini, D.; Nardi, F.; Cagli, C. Resistance-dependent amplitude of random telegraph-signal noise in resistive switching memories. *Appl. Phys. Lett.* **2010**, *96*, 053503. [\[CrossRef\]](#)
23. Marchewka, A.; Waser, R.; Menzel, S. Physical simulation of dynamic resistive switching in metal oxides using a Schottky contact barrier model. In Proceedings of the International Conference on Simulation of Semiconductor Processes and Devices (SISPAD), Washington, DC, USA, 9–11 September 2015; IEEE: New York, NY, USA, 2015; pp. 297–300. [\[CrossRef\]](#)
24. Strukov, D.B.; Alibart, F.; Stanley Williams, R. Thermophoresis/diffusion as a plausible mechanism for unipolar resistive switching in metal-oxide-metal memristors. *Appl. Phys. A* **2012**, *107*, 509–518. [\[CrossRef\]](#)
25. Guarcello, C.; Valenti, D.; Spagnolo, B. Phase dynamics in graphene-based Josephson junctions in the presence of thermal and correlated fluctuations. *Phys. Rev. B* **2015**, *92*, 174519. [\[CrossRef\]](#)
26. Carollo, A.; Spagnolo, B.; Valenti, D. Uhlmann curvature in dissipative phase transitions. *Sci. Rep.* **2018**, *8*, 9852. [\[CrossRef\]](#) [\[PubMed\]](#)
27. Jiang, H.; Han, L.; Lin, P.; Wang, Z.; Jang, M.H.; Wu, Q.; Barnell, M.; Yang, J.J.; Xin, H.L.; Xia, Q. Sub-10 nm Ta channel responsible for superior performance of a HfO_2 memristor. *Sci. Rep.* **2016**, *6*, 28525. [\[CrossRef\]](#) [\[PubMed\]](#)
28. Lu, K.; Li, Y.; He, W.F.; Chen, J.; Zhou, Y.X.; Duan, N.; Jin, M.M.; Gu, W.; Xue, K.H.; Sun, H.J.; et al. Diverse spike-timing-dependent plasticity based on multilevel HfO_x memristor for neuromorphic computing. *Appl. Phys. A* **2018**, *124*, 438. [\[CrossRef\]](#)
29. Lian, X.; Wang, M.; Rao, M.; Yan, P.; Yang, J.J.; Miao, F. Characteristics and transport mechanisms of triple switching regimes of TaO_x memristor. *Appl. Phys. Lett.* **2017**, *110*, 173504. [\[CrossRef\]](#)
30. Choi, S.; Jang, S.; Moon, J.H.; Kim, J.C.; Jeong, H.Y.; Jang, P.; Lee, K.J.; Wang, G. A self-rectifying TaO_y /nanoporous TaO_x memristor synaptic array for learning and energy-efficient neuromorphic systems. *NPG Asia Mater.* **2018**, *10*, 1097–1106. [\[CrossRef\]](#)
31. Abbas, Y.; Han, I.S.; Sokolov, A.S.; Jeon, Y.R.; Choi, C. Rapid thermal annealing on the atomic layer-deposited zirconia thin film to enhance resistive switching characteristics. *J. Mater. Sci. Mater. Electron.* **2020**, *31*, 903–909. [\[CrossRef\]](#)
32. Upadhyay, N.K.; Sun, W.; Lin, P.; Joshi, S.; Midya, R.; Zhang, X.; Wang, Z.; Jiang, H.; Yoon, J.H.; Rao, M.; et al. A memristor with low switching current and voltage for 1S1R integration and array operation. *Adv. Electron. Mater.* **2020**, *6*, 1901411. [\[CrossRef\]](#)
33. Gambuzza, L.V.; Samardžić, N.; Dautovic, S.; Xibilia, M.G.; Graziani, S.; Fortuna, L.; Stojanovic, G.; Frasca, M. A data driven model of TiO_2 printed memristors. In Proceedings of the 8th International Conference on Electrical and Electronics Engineering (ELECO), Bursa, Turkey, 28–30 November 2013; pp. 1–4. [\[CrossRef\]](#)
34. Kim, M.; Yoo, K.; Jeon, S.P.; Park, S.K.; Kim, Y.H. The effect of multi-layer stacking sequence of TiO_x active layers on the resistive-switching characteristics of memristor devices. *Micromachines* **2020**, *11*, 154. [\[CrossRef\]](#) [\[PubMed\]](#)
35. Cvejic, K.; Mojić, B.; Samardžić, N.; Srdić, V.V.; Stojanović, G.M. Dielectric studies of barium bismuth titanate as a material for application in temperature sensors. *J. Mater. Sci. Mater. Electron.* **2013**, *24*, 1243–1249. [\[CrossRef\]](#)
36. Vasileiadis, N.; Karakolis, P.; Mandylas, P.; Ioannou-Sougleridis, V.; Normand, P.; Perego, M.; Komninou, P.; Ntinis, V.; Fyrgos, I.A.; Karafyllidis, I.; et al. Understanding the role of defects in silicon nitride-based resistive switching memories through oxygen doping. *IEEE Trans. Nanotechnol.* **2021**, *20*, 356–364. [\[CrossRef\]](#)
37. Vasileiadis, N.; Ntinis, V.; Fyrgos, I.A.; Karamani, R.E.; Ioannou-Sougleridis, V.; Normand, P.; Karafyllidis, I.; Sirakoulis, G.C.; Dimitrakis, P. A new 1P1R image sensor with in-memory computing properties based on silicon nitride devices. In Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS), Daegu, Korea, 22–28 May 2021; IEEE: New York, NY, USA, 2021; pp. 1–5. [\[CrossRef\]](#)

38. Ambrosi, E.; Bricalli, A.; Laudato, M.; Ielmini, D. Impact of oxide and electrode materials on the switching characteristics of oxide ReRAM devices. *Faraday Discuss.* **2019**, *213*, 87–98. [\[CrossRef\]](#)
39. Yen, T.-J.; Chin, A.; Gritsenko, V. Improved device distribution in high-performance SiN_x Resistive Random Access Memory via Arsenic ion implantation. *Nanomaterials* **2021**, *11*, 1401. [\[CrossRef\]](#)
40. Duchamp, M.; Migunov, V.; Tavabi, A.H.; Mehonic, A.; Buckwell, M.; Munde, M.; Kenyon, A.J.; Dunin-Borkowski, R.E. In situ transmission electron microscopy of resistive switching in thin silicon oxide layers. *Resolut. Discov.* **2016**, *1*, 27–33. [\[CrossRef\]](#)
41. Jiang, X.; Ma, Z.; Yang, H.; Yu, J.; Wang, W.; Zhang, W.; Li, W.; Xu, J.; Xu, L.; Chen, K.; et al. Nanocrystalline Si pathway induced unipolar resistive switching behavior from annealed Si-rich SiN_x/SiN_y multilayers. *J. Appl. Phys.* **2014**, *116*, 123705. [\[CrossRef\]](#)
42. Islamov, D.R.; Gritsenko, V.A.; Chin, A. Charge transport in thin hafnium and zirconium oxide films. *Optoelectron. Instrument. Proc.* **2017**, *53*, 184–189. [\[CrossRef\]](#)
43. Gismatulin, A.A.; Orlov, O.M.; Gritsenko, V.A.; Kruchinin, V.N.; Mizginov, D.S.; Krasnikov, G.Y. Charge transport mechanism in the metal–nitride–oxide–silicon forming-free memristor structure. *Appl. Phys. Lett.* **2020**, *116*, 203502. [\[CrossRef\]](#)
44. Bishop, M.D.; Wong, H.S.P.; Mitra, S.; Shulaker, M.M. Monolithic 3-D integration. *IEEE Micro* **2019**, *39*, 16–27. [\[CrossRef\]](#)
45. Saylan, S.; Aldosari, H.M.; Humood, K.; Abi Jaoude, M.; Ravaux, F.; Mohammad, B. Effects of top electrode material in hafnium-oxide-based memristive systems on highly-doped Si. *Sci. Rep.* **2020**, *10*, 19541. [\[CrossRef\]](#) [\[PubMed\]](#)
46. Popov, V.P.; Antonova, A.I.; Frantsuzov, A.A.; Safronov, L.N.; Feofanov, G.N.; Naumova, O.V.; Kilanov, D.V. Properties of silicon-on-insulator structures and devices. *Semiconductors* **2001**, *35*, 1030–1037. [\[CrossRef\]](#)
47. Hoessbacher, C.; Fedoryshyn, Y.; Emboras, A.; Melikyan, A.; Kohl, M.; Hillerkuss, D.; Hafner, C.; Leuthold, J. The plasmonic memristor: A latching optical switch. *Optica* **2014**, *1*, 198–202. [\[CrossRef\]](#)
48. Puppo, F.; Doucey, M.A.; Di Ventra, M.; De Micheli, G.; Carrara, S. Memristor-based devices for sensing. In Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS), Melbourne, VIC, Australia, 1–5 June 2014; IEEE: New York, NY, USA, 2014; pp. 2257–2260. [\[CrossRef\]](#)
49. Li, C.; Han, L.; Jiang, H.; Jang, M.-H.; Lin, P.; Wu, Q.; Barnell, M.; Yang, J.J.; Xin, H.L.; Xia, Q. Three-dimensional crossbar arrays of self-rectifying Si/SiO₂/Si memristors. *Nat. Commun.* **2017**, *8*, 15666. [\[CrossRef\]](#)
50. Pragnya, P.; Pinkowitz, A.; Hull, R.; Gall, D. Electrochemical memristive devices based on submonolayer metal deposition. *APL Mater.* **2019**, *7*, 101121. [\[CrossRef\]](#)
51. Baltakesmez, A. Improved barrier parameters and working stability of Au/*p*-GO/*n*-InP/Au–Ge Schottky barrier diode with GO interlayer showing resistive switching effect. *Vacuum* **2019**, *168*, 108825. [\[CrossRef\]](#)
52. Skorobogatov, S. Local heating attacks on flash memory devices. In Proceedings of the IEEE International Workshop on Hardware-Oriented Security and Trust (HOST), San Francisco, CA, USA, 27 July 2009; IEEE: New York, NY, USA, 2009; pp. 1–6. [\[CrossRef\]](#)
53. Kärkkäinen, I.; Shkabko, A.; Heikkilä, M.; Vehkamäki, M.; Niinistö, J.; Aslam, N.; Meuffels, P.; Ritala, M.; Leskelä, M.; Waser, R.; et al. Impedance spectroscopy study of the unipolar and bipolar resistive switching states of atomic layer deposited polycrystalline ZrO₂ thin films. *Phys. Status Solidi A* **2015**, *212*, 751–766. [\[CrossRef\]](#)
54. Epshtein, S.L. *Measuring of Capacitor Characteristics*; Energiya: Moscow, Russia, 1965; 236p. (In Russian)
55. Oreshkin, P.T. *Physics of Semiconductors and Dielectrics*; Vysshaya Shkola: Moscow, Russia, 1977; 448p. (In Russian)
56. Ovsyuk, V.N. *Electronic Processes in Semiconductors with Space-Charge Regions*; Nauka: Novosibirsk, Russia, 1984; 254p. (In Russian)
57. Antipov, A.; Arakelian, S.; Vartanyan, T.; Gerke, M.; Istratov, A.; Kutrovskaia, S.; Kucherik, A.; Osipov, A. Optical properties of multilayer bimetallic films obtained by laser deposition of colloidal particles. *Opt. Spectrosc.* **2016**, *121*, 765–768. [\[CrossRef\]](#)
58. Hofmann, S. *Auger- and X-ray Photoelectron Spectroscopy in Materials Science*; Springer: Berlin/Heidelberg, Germany, 2013; 528p. [\[CrossRef\]](#)
59. Wang, T.Y.; Meng, J.L.; Li, Q.X.; Chen, L.; Zhu, H.; Sun, Q.Q.; Ding, S.J.; Zhang, D.W. Forming-free flexible memristor with multilevel storage for neuromorphic computing by full PVD technique. *J. Mater. Sci. Technol.* **2021**, *60*, 21–26. [\[CrossRef\]](#)
60. Gorshkov, O.N.; Mikhaylov, A.N.; Kasatkin, A.P.; Tikhov, S.V.; Filatov, D.O.; Pavlov, D.A.; Belov, A.I.; Koryazhkina, M.N.; Bobrov, A.I.; Malekhonova, N.V.; et al. Resistive switching in the Au/Zr/ZrO₂-Y₂O₃/TiN/Ti memristive devices deposited by magnetron sputtering. *J. Phys. Conf. Ser.* **2016**, *741*, 012174. [\[CrossRef\]](#)
61. Gurtov, V.A. *Solid State Electronics*; Tekhnosfera: Moscow, Russia, 2008; 512p. (In Russian)
62. Ismail, M.; Kim, S. Negative differential resistance effect and dual bipolar resistive switching properties in a transparent Ce-based devices with opposite forming polarity. *Appl. Surf. Sci.* **2020**, *530*, 147284. [\[CrossRef\]](#)
63. Kumar, N.; Chand, S. Effects of temperature, bias and frequency on the dielectric properties and electrical conductivity of Ni/SiO₂/*p*-Si/Al MIS Schottky diodes. *J. Alloys Compd.* **2020**, *817*, 153294. [\[CrossRef\]](#)
64. Hasegawa, H.; Sawada, T. On the electrical properties of compound semiconductor interfaces in metal/insulator/semiconductor structures and the possible origin of interface states. *Thin Solid Films* **1983**, *103*, 119–140. [\[CrossRef\]](#)
65. Chaabouni, F.; Abaab, M.; Rezig, B. Characterization of *n*-ZnO/*p*-Si films grown by magnetron sputtering. *Superlattices Microstruct.* **2006**, *39*, 171–178. [\[CrossRef\]](#)
66. Hu, C. *Modern Semiconductor Devices for Integrated Circuits*; Pearson: London, UK, 2010; p. 351.
67. Wang, L.G.; Zhang, W.; Chen, Y.; Cao, Y.Q.; Li, A.D.; Wu, D. Synaptic plasticity and learning behaviors mimicked in single inorganic synapses of Pt/HfO_x/ZnO_x/TiN memristive system. *Nanoscale Res. Lett.* **2017**, *12*, 65. [\[CrossRef\]](#) [\[PubMed\]](#)

68. Krishnaprasad, A.; Choudhary, N.; Das, S.; Dev, D.; Kalita, H.; Chung, H.S.; Aina, O.; Jung, Y.; Roy, T. Electronic synapses with near-linear weight update using MoS₂/graphene memristors. *Appl. Phys. Lett.* **2019**, *115*, 103104. [[CrossRef](#)]
69. Nasyrov, K.A.; Shaimeev, S.S.; Gritsenko, V.A.; Han, J.H.; Kim, C.W.; Lee, J.-W. Electron and hole injection in metal-oxide-nitride-oxide-silicon structures. *J. Exp. Theor. Phys.* **2006**, *102*, 810–820. [[CrossRef](#)]
70. Gismatulin, A.A.; Gritsenko, V.A.; Yen, T.-J.; Chin, A. Charge transport mechanism in SiN_x-based memristor. *Appl. Phys. Lett.* **2019**, *115*, 253502. [[CrossRef](#)]
71. Mikhaylov, A.N.; Belov, A.I.; Guseinov, D.V.; Korolev, D.S.; Antonov, I.N.; Efimovych, D.V.; Tikhov, S.V.; Kasatkin, A.P.; Gorshkov, O.N.; Tetelbaum, D.I.; et al. Bipolar resistive switching and charge transport in silicon oxide memristor. *Mater. Sci. Eng. B* **2015**, *194*, 48–54. [[CrossRef](#)]