Journal of
Low Power Electronics and Applications

MDPI

Article

Improved Frequency Compensation Technique for Three-Stage Amplifiers

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Abstract: Improved frequency compensation is proposed for a three-stage amplifier with reduced total capacitance, improved slew rate, and reduced settling time. The proposed compensation uses an auxiliary feedback to increase the total effective compensation capacitance without loading the output node. The proposed compensation scheme is validated in simulation by implementing a three-stage amplifier driving 10 pF load capacitor in a 0.18 µm CMOS process. A detailed comparison of the compensation with a conventional nested Miller compensation is also presented. The simulation results showed a reduction in total compensation capacitance and improvement in slew rate compared to conventional nested Miller compensation and the other reported techniques in the literature.

Keywords: frequency compensation; nested Miller compensation; high slew rate; low settling time; three-stage amplifier; Routh–Hurwitz stability criterion

Citation: Loera, A.R.; Veerabathini, A.; Oropeza, L.A.F.; Martínez, L.A.C.; Frias, D.M. Improved Frequency Compensation Technique for Three-Stage Amplifiers. *J. Low Power Electron. Appl.* **2021**, *11*, 11. https://doi.org/10.3390/jlpea11010011

Academic Editor: Fabian Khateb

Received: 25 January 2021
Accepted: 8 March 2021
Published: 12 March 2021

1. Introduction

Recent furtherance in the field of analog circuit design allowed for the evolution of new electronic devices supporting various applications. A wide market opportunity has been created for battery-operated portable devices such as smartphones, health monitor watches, home assistants, earphones, etc. The two essential characteristics of devices for such applications are device runtime on battery and the form-factor [1,2]. The device runtime is extended by either using a low power consumption circuits for the application or using high-efficiency DC–DC converters. Restriction of power consumption on the application core circuitry can compromise the performance of system. The use of high-efficiency DC–DC converters increases the runtime, and the use of fully-integrated converters, such as switched-capacitor converters, further helps to reduce the overall solution size [3]. Additionally, increasing the switching frequency of the DC–DC converter reduces the size of the energy element such as the inductor or capacitor [4].

Switching converters have output voltage ripples that make them not suitable for all applications. Low drop-out (LDO) regulators are popular when a clean and quiet power supply is required [5]. The LDO regulators are efficient when the output voltage is close to the input supply voltage, and its efficiency is the ratio of output to input voltage. As the supply voltage rails are reduced in lower CMOS process technologies, where the length of the FET is shrunk, the gain obtained from a single stage amplifier is lower. The DC accuracy and transient response of an LDO is directly set by the closed-loop gain and bandwidth of the error amplifier. Moreover, the design for such high frequency requires transistor models to include all the parasitic capacitances [6].

Multi-stage amplifiers are used for overall high gain. Increasing the number of stages creates additional high impedance nodes making the amplifier unstable due to

multiple poles [7]. A simple Miller compensation (SMC) and nested Miller compensation (NMC) are commonly used in two-stage and three-stage amplifiers for closed-loop stability, respectively. However, these multi-stage amplifiers suffers from bandwidth reduction as explained in [8,9]. In deep submicron CMOS process, a three-stage amplifier is sufficient to achieve acceptable overall gain for many applications.

Nested Miller compensation (NMC) is a popular frequency compensation technique used to stabilize three-stage amplifiers [10], this compensation scheme is shown in Figure 1. It must be noticed that if R_C is 0, the circuit shown in Figure 1 configures to a traditional NMC circuit. The compensation in a NMC scheme uses two capacitors connected between the output node and intermediate nodes of the amplifier. The nulling resistor, R_C allows cancellation of the RHP zero created by g_{m10}, and increasing $R_C > 1/g_{m10}$ creates an LHP zero which helps in phase boost [11]. This variant of an NMC circuit is denominated as nested Miller compensation with nulling resistor (NMCNR). The transfer function of NMC with nulling resistor is given by:

$$H(s) = A_{DC}\frac{\left(1 - C_{C2}\left(\frac{1}{g_{m10}} - R_C\right)s - \frac{C_{C1}C_{C2}}{g_{m7}g_{m10}}s^2\right)}{\left(1 + \frac{s}{w_{p3dB}}\right)\left(1 + \frac{C_{C2}(k_1 g_{m10} - g_{m7})}{g_{m7}g_{m10}}s + \frac{C_{C2}C_L k_2}{g_{m7}g_{m10}}s^2\right)} \tag{1}$$

where $A_{DC} = g_{m1}R_1 g_{m7}R_3 g_{m10}R_O$, $w_{p3dB} = \frac{1}{R_1(g_{m7}R_3 g_{m10}R_O)C_{C1}}$, $k_1 = 1 + g_{m7}R_c$, $k_2 = 1 + \frac{R_c}{R_2}$. Resistors R_1, R_2 and R_3 are the output impedance at nodes V_1, V_2 and V_3, respectively. The transfer function of a traditional NMC can be obtained by evaluating the Equation (1) with $R_C = 0$.

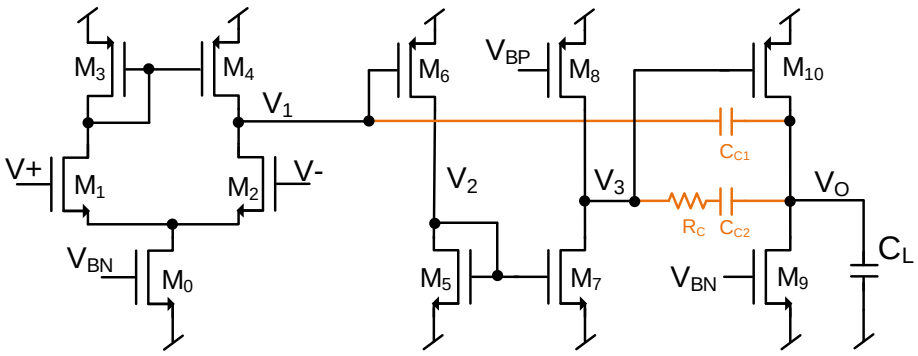


Figure 1. Nested Miller compensation.

NMC has one RHP zero, one LHP zero and three LHP poles when $k_1 g_{m10} \geq g_{m7}$. As the compensation capacitors are loading the output, this amplifier suffers from poor slew rate at high frequency. Under the slewing condition, V_O is required to pull up by charging the load capacitor C_L, the internal node V_3 is pulled down towards the ground to allow more current to flow through M_{10}. When V_3 is pulled low, the compensation capacitor C_{C2} appears to be in parallel with C_L loading the output node causing a slow slew rate. Moreover, this changes the overall compensation of the circuit where C_{C2} disappears and the entire circuit is compensated by C_{C1} only. This changes the amplifier stability conditions considerably and increases the settling time. To design a stable NMC amplifier, the compensation capacitors must be chosen with the following conditions [7]:

$$C_{C1} = 4\left(\frac{g_{m1}}{g_{m10}}\right)C_L \tag{2}$$

$$C_{C2} = 2\left(\frac{g_{m7}}{g_{m10}}\right)C_L \tag{3}$$

The load capacitor affects the location of non-dominant poles and gain bandwidth (GBW) product making this compensation suitable only for applications with small range of load capacitance. GBW for NMC is given by [12]:

$$GBW = \frac{g_{m1}}{C_{C1}} = \frac{1}{4}\left(\frac{g_{m10}}{C_L}\right) \tag{4}$$

Reverse nested Miller compensation (RNMC) is another compensation where the output of the first stage of the amplifier is loaded with both compensation capacitors causing the internal voltage to be slew limited [13,14]. Referring to Figure 2, RNMC requires non-inverting configuration in the third stage between V_2 and V_O. This limits the driving capability of the output stage due to limited voltage swing on V_{2A}. The transfer function of RNMC is given by [13]:

$$H(s) = A_{DC}\frac{1 - \left(\frac{C_{C2}}{g_{m6}} + \frac{C_{C1}}{g_{m6}g_{m9}R_2}\right)s - \frac{C_{C1}C_{C2}}{g_{m6}g_{m9}}s^2}{\left(1 + \frac{s}{\omega_{P1}}\right)\left[1 + \left(\frac{C_{C2}C_L}{g_{m9}C_{C1}} - \frac{C_{C2}}{g_{m6}} + \frac{C_{C2}}{g_{m9}}\right)s + \frac{C_{C2}C_L}{g_{m6}g_{m9}}s^2\right]} \tag{5}$$

where $A_{DC} = g_{m1}R_1g_{m6}R_2g_{m9}R_O$, and $\omega_{P1} = 1/R_1(g_{m6}R_2g_{m9}R_O)C_{C1})$.

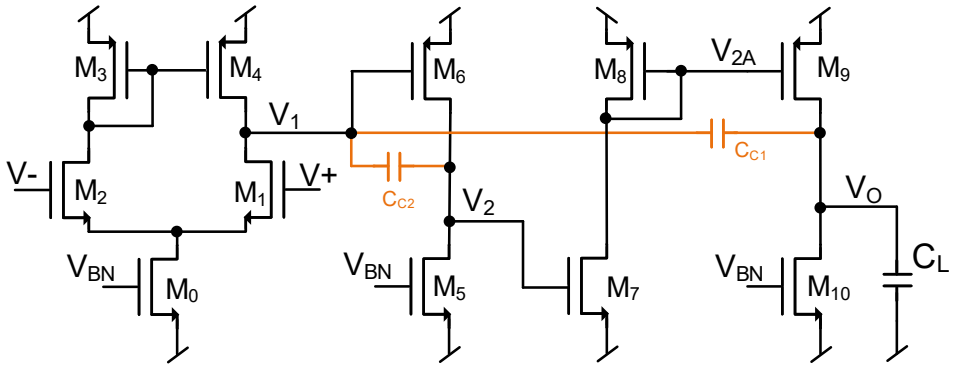


Figure 2. Reverse nested Miller compensation.

Multiple advanced compensation techniques are published in the literature to extend the bandwidth, such as the double pole–zero canceling technique [15], multipath NMC (MNMC) [10], nested Gm-C compensation (NGCC) [16] and damping factor control frequency compensation (DFCFC) [7]. However, all these compensation techniques have strong dependency on output load capacitor for stability. NMC and RNMC with combination of voltage and current buffers are proposed in the literature to isolate the output node or compensate for RHP zero [17]. The proposed compensation scheme described in the next section solves these challenges.

2. Proposed Improved Frequency Compensation

An improved frequency compensation method is proposed using a single capacitor with auxiliary feedback loop connected between the two intermediate nodes as shown in Figure 3. Typically, the internal nodes of a multi-stage amplifier have a finite voltage swing compared to its output voltage swing. The use of the compensation capacitor on the high-swing output node severely affects the circuit slew rate compared to loading compensation capacitors on internal nodes where the voltage swing is limited. Using this advantage, the proposed compensation scheme uses internal circuit nodes V_1 and V_2 for compensation.

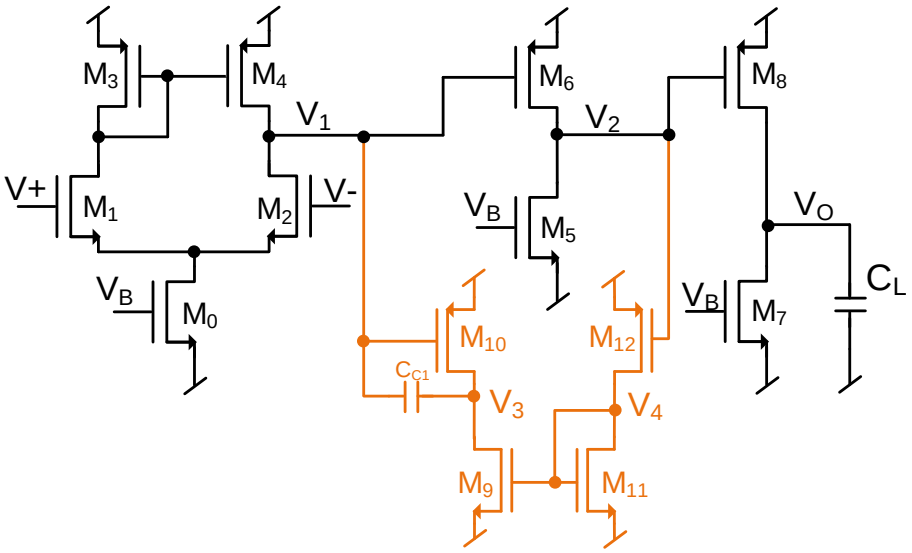


Figure 3. Proposed improved frequency compensation.

Referring to Figure 3, M_{0-4}, $M_{5,6}$ and $M_{7,8}$ are the three stages of the amplifier. M_{9-12} are used for compensation, where M_9 and M_{10} generate a Miller effect over C_C adding one LHP zero-pole pair to the amplifier transfer function. The small-signal model for the proposed compensation is shown in Figure 4, where R_1, R_2, R_3, R_4 and R_O are the output impedance, and C_1, C_2, C_3, C_4 are the total parasitic capacitances at nodes V_1, V_2, V_3, V_4 and C_L is the load capacitor at node V_O. The transfer function is given by:

$$H(s) = A_{DC}\frac{(1+R_3C_{C1}s)}{\left(1+\frac{s}{\omega_{p3dB}}\right)(1+R_OC_Ls)\left(1+\frac{C_2}{g_{m6}}s+\frac{C_1C_2}{g_{m10}g_{m6}}s^2\right)} \quad (6)$$

where $A_{DC} = g_{m1}R_1g_{m6}R_2g_{m8}R_O$, and $\omega_{p3dB} = \frac{1}{R_1(g_{m6}R_2g_{m10}R_3)C_{C1}}$.

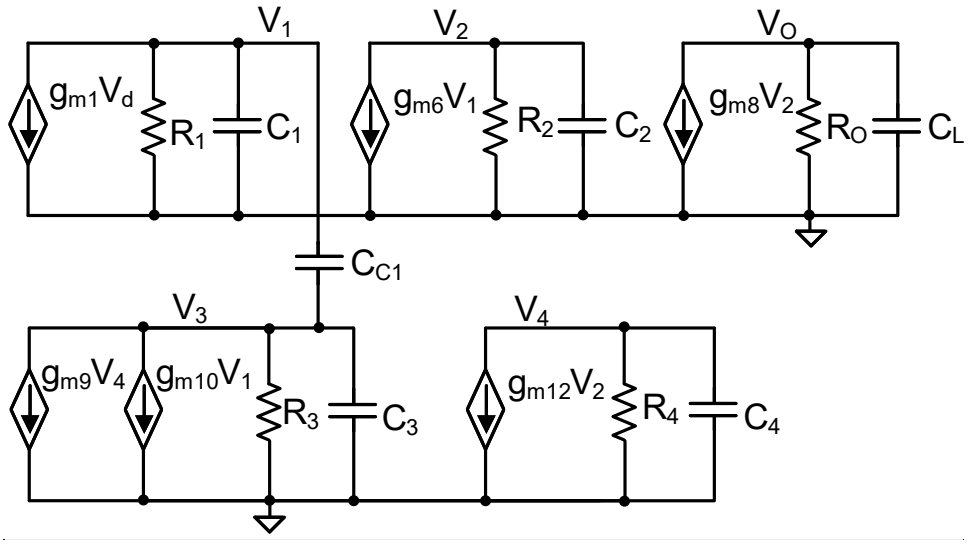


Figure 4. Small signal model of the proposed improved frequency compensation.

The proposed compensation has one LHP zero and four LHP poles. Two of these poles $\omega_{p2,3}$ are high frequency poles set by C_1 and C_2 parasitic capacitaces at nodes V_1 and V_2, respectively. Observe that C_4 is connected to a low impedance node and the pole associated with C_4 is located at a very high frequency and can be neglected. Similarly, parasitic capacitance C_3 is connected to a node where the effect of C_{C1} capacitor is dominant;

therefore, it can be also neglected. Additionally, a pole-zero cancellation can be achieved by selecting $R_3C_{C1} \approx mR_OC_L$, and this condition is controlled by the relationship between the transconductances g_{m8} and g_{m10}, where $g_{m10} = n \times g_{m8}$. The compensation capacitor C_{C1} can be selected by using $C_{C1} = C_L/n$. Observe that the compensation capacitor C_{C1} can be reduced by increasing the output transconductace g_{m10}. The dominant pole ω_{p3db} at node V_1 is set by $g_{m6} \times R_2$ and $g_{m10} \times R_3$, where these gains divide the node frequency pole $(1/(R_1C_{C1})$ to move the pole to a low frequency. Sizing C_{C1} adequately, the non-dominant pole $(1 + R_OC_Ls)$ can be compensated. If parasitic capacitors are neglected such as most of the models reported in the literature, the transfer of Equation (6) can be approximated to a single pole transfer function. The pole zero location illustration is shown in Figure 5, where ω_{pHF} and ω_{ZHF} are a very high frequency pole and zero from intermediate nodes.

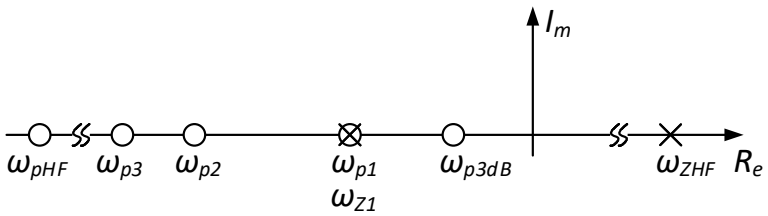


Figure 5. Pole zero location illustration (not to scale).

Phase margin is given by:

$$PM = 180^\circ - \tan^{-1}\left(\frac{GBW}{\omega_{p3db}}\right) - \tan^{-1}\left(\frac{GBW}{p_1}\right) + \tan^{-1}\left(\frac{GBW}{z_1}\right) - \tan^{-1}\left(\frac{GBW}{p_2}\right) - \tan^{-1}\left(\frac{GBW}{p_3}\right) \quad (7)$$

$$PM \approx 180^\circ - \tan^{-1}\left(\frac{GBW}{\omega_{p3db}}\right) \quad (8)$$

Observe that the pole-zero cancelled transfer function in Equation (9) yields similar response when well-known techniques such as voltage followers, current followers, and multipath Miller approaches are used [15]; except that in the proposed compensation, the second and third poles are located at high frequency, which is set by parasitic capacitances at the output of the first and second stages instead of compensation capacitors to provide a phase boost.

$$H(s) = A_{DC}\frac{1}{\left(1 + \frac{s}{\omega_{p3dB}}\right)\left(1 + \frac{C_2}{g_{m6}}s + \frac{C_1C_2}{g_{m10}g_{m6}}s^2\right)} \quad (9)$$

Referring to the slew-rate degradation in NMC, the proposed compensation scheme remains connected in the original configuration during slewing condition, and no settling time degradation is observed. The proposed compensation can be used for improved load transient response in LDOs where high output load capacitance is used.

3. Stability Analysis

Phase margin and gain margin are the two essential parameters used to characterize the stability of an amplifier, and they are measured in an open-loop configuration. Nevertheless, these parameters do not guarantee a good stability in closed-loop operation as explained in detail in [1]. Routh–Hurwitz stability criterion is an alternative method that can be used to identify conditions that make the closed-loop configuration unstable [18,19].

For Routh–Hurwitz stability criterion, consider an unitary feedback with a closed-loop gain transfer function given by $T(s)$ in Equation (10). Observe that the open-loop zero of $H(s)$ in Equation (6) is part of the characteristic polynomial, and the closed-loop poles positions in the denominator are modified. Therefore, a closed-loop stability should be analyzed using Routh–Hurwitz stability criterion.

$$T(s) = A_{DC}\frac{(1 + C_{C1}R_3 s)}{(1 + C_L R_O s)\left(1 + \frac{s}{\omega_{p3dB}}\right)\left(\frac{C_1 C_2 s^2}{gm_1 0 gm_6} + \frac{C_2 s}{gm_6} + 1\right) + A_{DC}(1 + C_{C1}R_3 s)} \tag{10}$$

The characteristic polynomial of poles in the Equation (10) can be simplified and represented by:

$$a_4 s^4 + a_3 s^3 + a_2 s^2 + a_1 s + a_0$$

According to the Routh–Hurwitz stability criterion, it can be concluded that the closed-loop transfer function with fourth-degree polynomial characteristics should meet the following criteria to avoid any RHP pole creation [1]:

$$a_2 > \frac{a_4 \cdot a_1}{a_3}$$

Solving for parameters a_4, a_3, a_2 and a_1 from the characteristic polynomial of the transfer function $T(s)$, the closed-loop stability criterion for the proposed compensation scheme is given by:

$$C_L > \frac{C_1 gm_1 gm_8}{gm_{10}{}^2} \tag{11}$$

4. Simulation Results

A conventional three-stage amplifier with the proposed improved frequency compensation is implemented in a 0.18 µm CMOS process. A conventional three-stage amplifier with NMC, NMCNR and RNMC is also implemented for comparison. All amplifiers are designed to drive a load capacitance of 10 pF with VDD = 1.8 V and DC gain = 90 dB. Transistor parameters are given in Table 1.

Table 1. Transistor parameters.

	Devices	Value	Units
$\frac{W}{L}$	M_0x2, M_1, M_2, M_5, M_7x5, M_9, M_{11}	1.8/0.72	µm/µm
	M_3, M_4, M_6, M_8x5, M_{10}, M_{12}	7.2/0.72	µm/µm
g_m	M_1, M_2, M_6, M_9, M_{10}, M_{12}	160	µV/A
	M_8	800	µV/A
	I_{BIAS}	125	µA
	V_{DD}	1.8	V

The transfer function shown in Equation (6) is verified with a simulation of transfer function equation and a transistor level implementation. The ac response of both implementations is shown in Figure 6. Observe that both AC responses overlap with each other to match up to high frequency. The mismatch at high frequency is due to high-frequency parasitic capacitances that are neglected in the transfer function for simplicity.

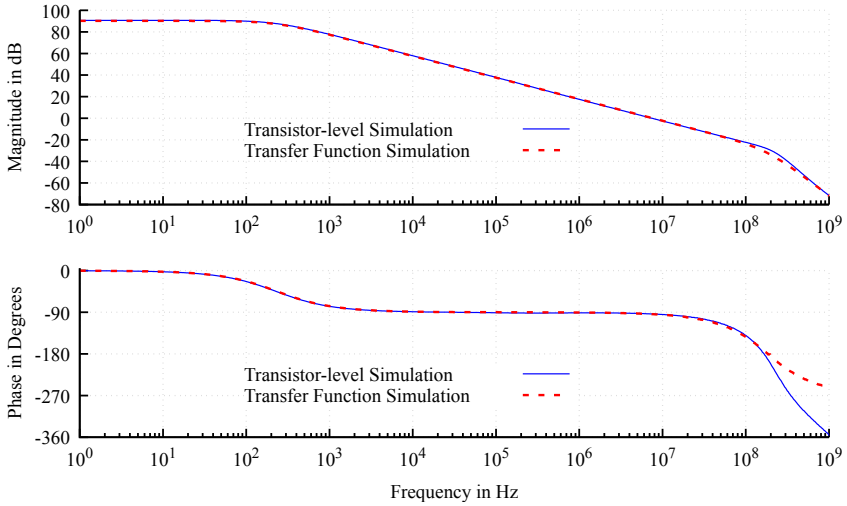


Figure 6. AC response of proposed frequency compensation with transfer function and transistors.

Referring to Figure 7, the AC response of the proposed compensation scheme is compared with NMC, NMCNR and RNMC compensation schemes. Observe that the response of the proposed scheme almost overlaps with the RNMC scheme, with the difference that the proposed compensation moves high-frequency poles to a much higher frequency. It is clear that the stability of the other compensation scheme is conditioned to maintain a good separation between their high frequency poles set by compensation capacitors, and the high frequency poles set by parasitic capacitances. This limits the highest achievable GBW with relatively good stability, whereas in the proposed compensation scheme, the design can operate with the highest GBW with relatively good stability as no high frequency poles are added. The only limitation is by the increment of parasitic capacitors obtained by growing the output stage transistors. Referring to Figure 7, the high-frequency improvement achieved by this compensation scheme increased the phase and gain margin showing better stability parameters with respect to the other compensation scheme used to compare the performance of the proposed compensation scheme.

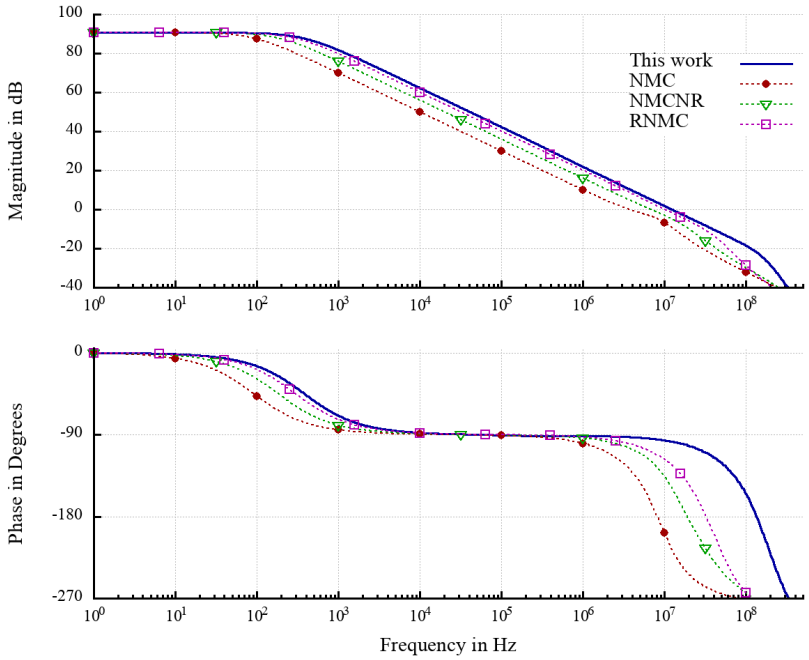


Figure 7. AC response of proposed frequency compensation compared with nested Miller compensation.

The settling time improvement is validated with large-signal and small-signal step response stimulus at different rise and fall times. For large-signal settling response, a 500 mV pulse with a rise and fall time of 300 ns is applied with a DC offset of 0.9 V to all amplifiers with different compensations, and the response is shown in Figure 8. Since NMC amplifier has a lower GBW and not good gain margin, some oscillations can be observed in its output signal. NMCNR, RNMC and the proposed compensation showed higher GBW with better phase margin and gain margin, and no oscillations are observed. An intentional large offset is added to the figures for readability.

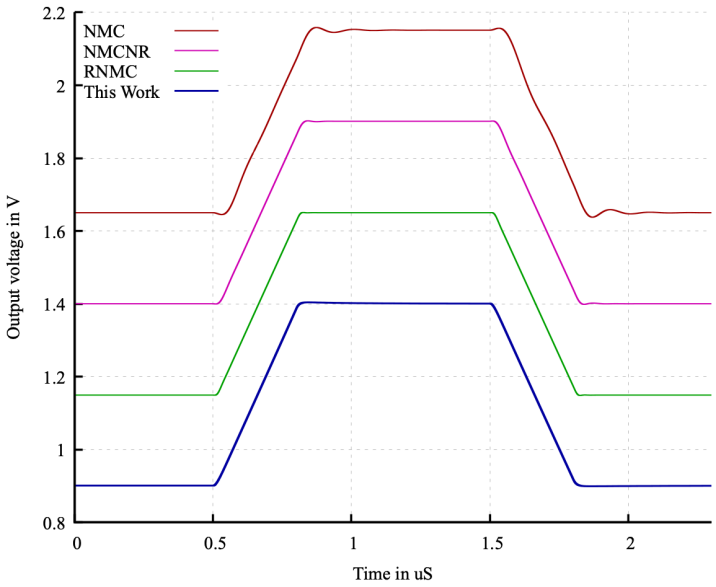


Figure 8. Large signal settling of proposed and nested Miller compensation with 300 ns rise and fall time. An intentional offset is added to the figure to distinguish the signals.

Small-signal settling is validated by applying 50 mV pulse with a rise and fall time of 50 ns as shown in Figure 9a. Observe that the proposed compensation does not show any voltage ring or peaking due to increased phase margin. Additionally, a large signal settling of 500 mV with a rise and fall time of 50 ns representing the slewing condition is shown in Figure 9b. Observe that the NMC shows a degraded response and higher fall settling time, whereas the proposed compensation scheme has no degradation during slewing condition. Similar responses are seen in NMCNR and RNMC. RNMC shows reduced fall settling degradation and this can be attributed to the fact that in order to design a stable amplifier, the trasconductance of second stage must be increased, which increases the slew rate and power consumption.

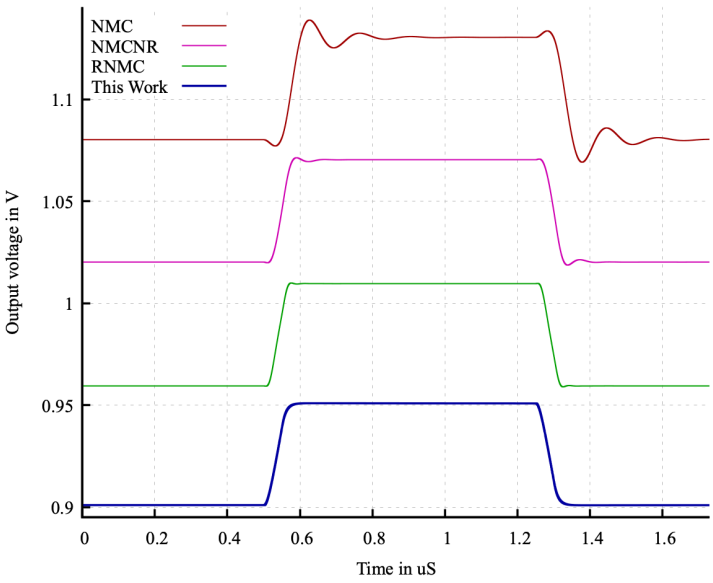
The total compensation capacitance required is reduced from 12 pF with NMC, 5.5 pF with NMCNR, 3.5 pF with RNMC to 2 pF and no nulling resistor. The phase margin is improved from 53 deg to 82.5 deg and the gain margin from 4.71 dB to 21.9 dB when compared with NMC as the proposed compensation scheme do not add high-frequency poles. Moreover, a significant improvement in the slew rate is observed with the proposed compensation. The proposed compensation is compared with the literature and is shown in Table 2, where unity gain frequency (UGF), DC gain (A_0), phase margin (PM), gain margin (GM), total compensation capacitance (C_C), total compensation resistance (R_C), load capacitance (C_L), average slew rate (SR), power consumption (P), and figure of merits (FOM) are given. Observe that the proposed scheme slew rate is 146% higher than NMC and 60% higher than NMCNR. RNMC has similar slew rate but consumes high power. Three different figures of merit (FOMs) are used to compare the performance of the proposed compensation scheme and are shown below. A FOM proposed in [14], FOM_R considers GBW, total sum of all transconductances and compensation capacitances. Observe that the proposed compensation scheme has higher FOM_S, FOM_L, FOM_{IS}, FOM_{IL}, and FOM_R.

A summary of stability and settling time results is the proposed compensation are shown in Table 3.

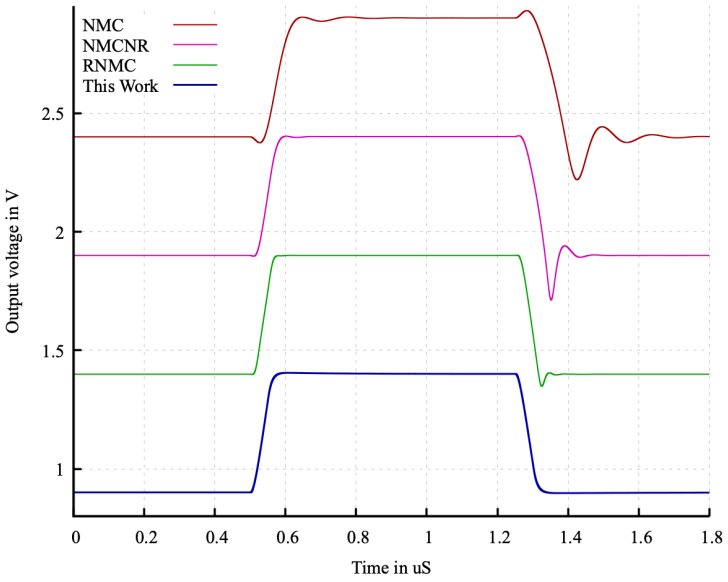
$$FOM_S = \frac{GBW_{Hz} \cdot C_L}{VDD \cdot I_{DD}} \qquad (MHz \cdot pF/mW) \tag{12}$$

$$FOM_L = \frac{SR \cdot C_L}{V_{DD} \cdot I_{DD}} \qquad (V/\mu s \cdot pF/mW) \tag{13}$$

$$FOM_R = \frac{\omega_{GBW} \cdot C_L}{g_{m1} + g_{m2} + g_{m3} + g_{mCOMP}} \tag{14}$$



(**a**) Small signal with 50 ns rise and fall time.



(**b**) Large signal with 50 ns rise and fall time.

Figure 9. Output voltage signal settling of proposed and nested Miller compensation. An intentional offset is added to the figure to distinguish the signals.

Table 2. Results comparison.

Type	Proposed	NMC	NMCNR	RNMC	[20] DPZC	[10] MNMC	[16] NGCC	[21] NMCFNR	[7] DFCFC
Process (μm)	**0.18**	0.18	0.18	0.18	0.35	0.35	0.35	0.35	0.35
UGF (MHz)	**12.31**	3.2	6.76	10.2	0.4	0.54	0.25	0.8	0.96
$C_C(pF)$	**2**	12	5.5	3.5	49.5	141	94	28.7	35
R_C (kΩ)	**0**	0	6	0	-	-	-	-	-
$C_L(pF)$	**10**	10	10	10	100	100	100	100	100
SR ($V/\mu s$)	**16**	6.5	10	15	0.375	0.4	0.27	0.75	0.78
P (μW)	**495**	450	450	675	345	431	365	345	372
FOM_S	**249**	71	150	151	116	125	68	232	256
FOM_L	**323**	144	222	222	109	93	101	217	208
FOM_{IS}	**447**	128	270	272	232	250	136	472	512
FOM_{IL}	**581**	0.18	0.35	0.36	218	186	202	434	416
FOM_R	**0.625**	0.18	0.35	0.36	0.24	0.21	0.13	0.39	0.56

Table 3. Stability and settling time results.

Type	Proposed	NMC	NMCNR	RNMC
UGF (MHz)	**12.31**	3.2	6.76	10.2
A_0 (dB)	**90.7**	90.7	90.7	90.7
PM (deg)	**82.5**	53	61	62
GM (dB)	**22**	4.71	9.5	10.8
t_{r1}/t_{f1} (ns) V_S = 50 mV, $t_{r,f}$ = 50 ns	**77/93**	286/289	78/126	67/63
t_{r2}/t_{f2} (ns) V_S = 0.5 V, $t_{r,f}$ = 50 ns	**297/297**	338/374	307/310	300/300
t_{r2}/t_{f2} (ns) V_S = 0.5 V, $t_{r,f}$ = 300 ns	**65/72**	213/414	78/235	65/125

The process corner simulation results at different temperatures are shown in Table 4. Observe that the phase margin and gain margin are maintained greater than 81° and 22 dB, respectively. A maximum deviation of 3.9 MHz is observed for unity-gain frequency from typical process and room temperature. Despite the process variation, the proposed compensation scheme maintained good stability for a temperature range from −40° to 125°.

Table 4. Process corners at different temperatures.

Temperature −40 °C					
Corner	TT	SS	FF	SF	FS
UGF (MHz)	15.48	14.77	16.48	14.93	16.23
Phase Margin (deg)	83	83	82.7	83.45	82.35
Gain Margin (dB)	23.72	23.77	23.6	24.25	23.11
Temperature 27 °C					
Corner	TT	SS	FF	SF	FS
UGF (MHz)	12.3	11.6	13.1	11.76	12.86
Phase Margin (deg)	82.5	86.53	83.1	83.87	82.74
Gain Margin (dB)	22	24.37	24	24.63	23.57
Temperature 125 °C					
Corner	TT	SS	FF	SF	FS
UGF (MHz)	9.29	8.75	10	8.96	9.83
Phase Margin (deg)	84	84.26	83.7	84.5	83.4
Gain Margin (dB)	25.12	25.32	24.75	25.66	24.4

5. Conclusions

The proposed compensation scheme for a three-stage amplifier uses lower compensation capacitance to achieve dynamic response superior to NMC and NMCNR, and is similar to RNMC without consuming higher power nor using a nulling resistor. The proposed compensation allows the amplifier to operate with the highest GBW with relatively good stability as no high frequency compensation poles are added. The slew-rate degradation observed in NMC is solved with the proposed compensation scheme, where the intended compensation remains connected in the original configuration during slewing condition. The proposed compensation can be used for improved load transient response in LDOs.

Author Contributions: The research problem is identified, executed, and solved by A.R.L. conducted a feasibility study through simulation, and transfer function calculations. A.V. conducted the literature review and advised on the architecture and wrote the initial draft manuscript. L.A.F.O., L.A.C.M., and D.M.F. supervised research that includes and is not limited to project administration, design and simulation results review, manuscript review, and corrections. All authors have read and agreed to the published version of the manuscript.

Funding: This research received no external funding.

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Acknowledgments: This work has been supported by PRODEP program from SEP (Secretariat of Public Education, Mexico) and Universidad Autonoma de Aguascalientes, Aguascalientes, Mexico.

Conflicts of Interest: The authors declare no conflict of interest.

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