

Article

An Approach for a Wide Dynamic Range Low-Noise Current Readout Circuit

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Abstract: Designing low-noise current readout circuits at high speed is challenging. There is a need for preamplification stages to amplify weak input currents before being processed by conventional integrator based readout. However, the high current gain preamplification stage usually limits the dynamic range. This article presents a 140 dB input dynamic range low-noise current readout circuit with a noise floor of $10 \sqrt{f A_{rms}} / \sqrt{q} (Hz)$. The architecture uses a programmable bidirectional input current gain stage followed by an integrator-based analog-to-pulse conversion stage. The programmable current gains setting enables one to achieve higher overall input dynamic range. The readout circuit is designed and in $0.18 \mu m$ CMOS and consumes 10.3 mW power from a 1.8 V supply. The circuit has been verified using post-layout simulations.

Keywords: dynamic range; low-noise current amplification; programmable gain

1. Introduction

There is a growing need to sense very low levels of current in many biosensors and diagnostics applications [1–3]. Current levels in such applications can be as low as picoamperes (pA) which are harder to detect using CMOS circuitry due to circuit noise. Several readout circuits have been developed for low current sensing. For example, an integrator or a transimpedance amplifier (TIA) has been employed to convert the current signal into a voltage signal, followed by quantization of the converted voltage signal. However, with the current in the pA range, if the integration method is adopted, it would take a long time to accumulate the small current into measurable voltage signal [4]. If a TIA is employed, the feedback resistance must be large enough (i.e., gigaohms range) to obtain high gain and there is a trade-off between achieving high dynamic range and achieving low input-referred current noise. Moreover, such a large feedback resistor cannot be reliably realized on-chip and must be externally connected. A high-value active pseudo resistor made using off-state transistors have been widely used for small current sensing [5–8]. However, the resistance is inversely proportional to the input current, which leads to a variable current gain and bandwidth applications [9].

In most applications, the small current signal needs to be amplified at high speed in bandwidths excess of 1 MHz. One such application is for nanopore sensing where the transient activity is in microseconds with Femto ampere current levels. A current conveyor is commonly employed for current amplification; however, the conventional current conveyor is not suitable for the small current amplification since the bias current of the conveyor leads to large input-referred current noise [10,11]. No-bias current conveyor has been adopted for low-noise current sensing [12]. The noise levels achieved may still be prohibitive for low current sensing. A current preamplifier was presented, featuring a matched double-MOS architecture around an amplifier to obtain current amplification in [13]. Capacitors with the same current ratio are needed to increase the bandwidth. The fixed current amplification gain leads to a smaller dynamic range. In this paper, a current preamplifier with

a programmable gain is proposed to obtain bidirectional current amplification. The programmable current gains setting enables one to achieve a higher overall input dynamic range. Higher gain allows for faster operation for small input currents while lower gain avoids saturation of the integrator stage for large input currents. Thus, the variable current gain enables a wider input dynamic range. Note the input dynamic range is defined as the ratio of the largest to the smallest input signal that the circuitry can process. For a programmable gain amplifier, the dynamic range will be measured as a ratio of highest input signal level (at lowest gain setting) and the largest referred input noise ever measured for any of the gain settings. A pulse width modulation output stage provides a digital output without the need for clock. The circuit is designed in a 0.18 μm CMOS process and validated using post-layout simulations.

2. Low-Noise Current Readout Architecture

2.1. Current Amplification

Floating current mirror is utilized to realize high current gain for amplifying weak current levels [13]. In Figure 1, transistor M_{N1} and M_{P1} are connected across the feedback loop of the amplifier. Transistor M_{N2} and M_{P2} are connected to the output node V_x . The node V_{out} connects to the negative input node of a following TIA or integrator stage which keeps V_{out} at the exact same voltage potential as node V_{in} or V_{cm} . Therefore, transistors $M_{N(P)1}$ and $M_{N(P)2}$ have the same V_{gs} and V_{ds} . The input current flows in or out through M_{N1} or M_{P1} , depending on the polarity of the current signal. Transistors M_{N2} and M_{P2} are sized N times as M_{N1} and M_{P1} , respectively. Therefore, the current through M_{N2} or M_{P2} is N times the input current signal. The capacitor C_1 and C_2 have the same ratio of N for high frequency current amplification as in Equation (1).

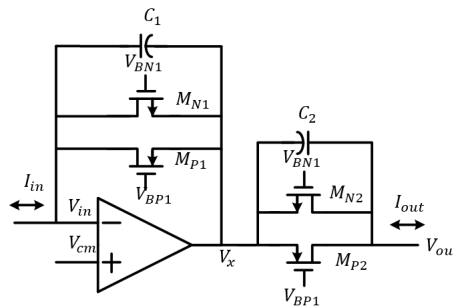


Figure 1. Bidirectional current amplification.

$$\frac{\left(\frac{W}{L}\right)_{M_{P2}}}{\left(\frac{W}{L}\right)_{M_{P1}}} = \frac{\left(\frac{W}{L}\right)_{M_{N2}}}{\left(\frac{W}{L}\right)_{M_{N1}}} = \frac{C_1}{C_2} = N \quad (1)$$

This architecture has the advantage that it provides high current gain so that the input-referred current noise at the input node from the following TIA or integrator is attenuated by the high current gain of this preamplification stage. However, this fixed high current gain would saturate the following TIA or integrator stage when the input current signal is large. The maximum input current is limited to the tens of nA range. In this paper, we design a programmable current preamplification stage to extend the input current signal range. This allows one to trade-off noise performance with a high dynamic range.

2.2. Programmable Gain Current Amplifier Stage

To allow processing of wide range (100 fA – 1 μA) current signals, the gain of the current amplifier is designed to be programmable, and the gate control voltage of transistor $M_{N(P)1}$ and $M_{N(P)2}$ can be externally tuned to adjust to the different range of input currents. Two cascade current gain stages are

implemented for a maximum of $1000\times$. This is designed to amplify currents as low as 100 fA. The first stage offers a maximum current gain of 50, while the second stage provides a maximum current gain of 20. The effective capacitor ratio and the effective transistor ratio are programmable to achieve different current gain for a high dynamic input current range as in Table 1.

Table 1. Current gain in each stage.

Total Gain	First Stage Gain	Second Stage Gain
$1000\times$	$50\times$	$20\times$
$100\times$	$50\times$	$2\times$
$10\times$	$10\times$	$1\times$
$1\times$	$1\times$	$1\times$

2.3. Low-Frequency Gain Setting

The programmable low-frequency current amplification ratio is achieved by turning on or off the mirroring transistors M_{N2} and M_{P2} in Figure 2. For the first current gain stage, there are a total of 50 sets of transistors-based current mirrors for low-frequency current signal amplification. Let us consider one example. For a gain of 10, the gates of the 10 NMOS transistors M_{N2} connect to V_{BN1} , while the gates of the remaining 40 NMOS transistors M_{N2} connect to Gnd ; the gates of the 10 PMOS transistors M_{P2} connect to V_{PN1} , while the gates of the remaining 40 PMOS transistors M_{P2} connect to Vdd .

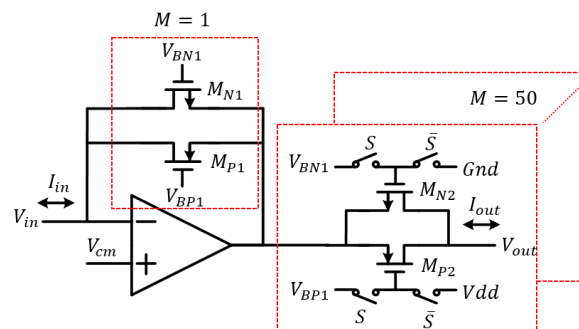


Figure 2. Programmable low-frequency current gain stage.

2.4. High-Frequency Gain Setting

The high-frequency programmable gain is obtained by setting the feedback capacitor units. For the first current amplification stage, there are a total of 50 cells of feedback capacitors controlled by the switches in the feedback loop as in Figure 3. The switches are large to reduce the on-resistance. However, the large size switch increases the parasitic capacitance that reduces the accuracy of the high-frequency gain. For example, if a gain of 10 is selected, then the first stage enables 10 capacitors by turning on the 10 switches coupling to the capacitors. The remaining 40 switches are turned off. However, the switches from the disabled paths will still add to the parasitic capacitance in parallel with the feedback capacitors, which provide a signal path for the high-frequency signal as in Figure 4. Consequently, this will influence the gain at high frequency. The problem is exaggerated when two gain stages are cascaded.

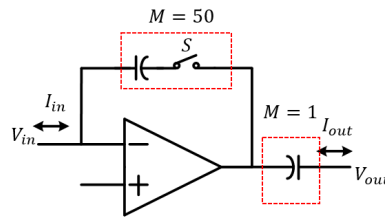


Figure 3. Conventional series switch based high frequency current gain stage.

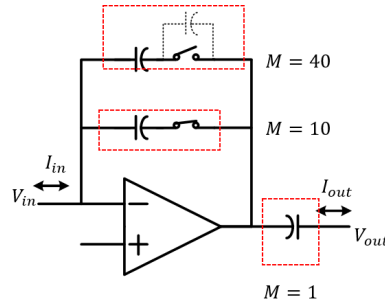


Figure 4. Shows a realization of a gain of 10. Off-switches will still contribute to parasitic capacitance affecting the overall gain and stability.

To solve this problem, we realize a T-network using two capacitors connecting in series as the feedback capacitor and move the switch between their intermediate node V_c and ground as in Figure 5. When the feedback path is enabled, the switch is off, presenting a high impedance node at V_c , the high-frequency signal can go through the feedback path. The two feedback capacitors connecting in series form equivalent feedback C as in Figure 6. When the feedback path is disabled, the switch is on presenting a low impedance node at V_c , the high-frequency signal has a path to ground, without passing through the feedback path as in Figure 7. This implementation is more stable (better phase margin) compared to conventional implementation as in Figure 4. Note that the NMOS switch is not in the high-frequency signal path when the high-frequency signal gain is enabled, therefore, the size of the NMOS switch can be designed with small size introducing minimal parasitic capacitance. There is also no issue of parasitic capacitance when certain feedback paths are disabled. A dummy disabled NMOS switch is connected at node V_D for matching. The programmable low-frequency and high-frequency current gain provide an accurate amplification over a large input current dynamic range and over a large bandwidth.

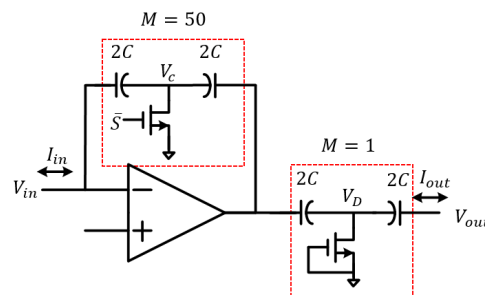


Figure 5. Proposed programmable high-gain stage using a T-network.

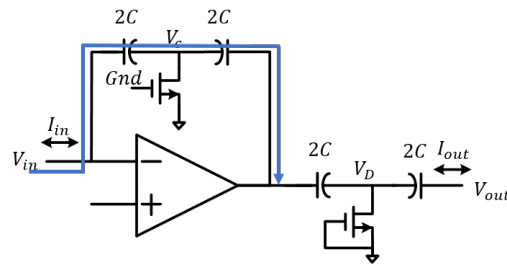


Figure 6. Current follows through the two feedback capacitor during amplification state.

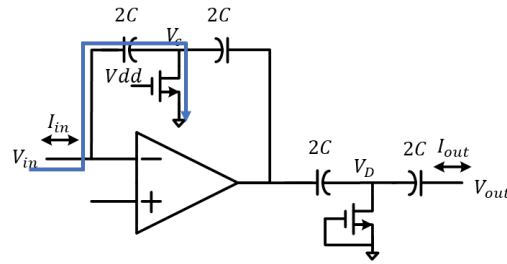


Figure 7. Current follows through the ground during off state.

2.5. System Architecture

The readout system is composed of two current amplification stages, an integrator stage, and a pulse width modulation stage as shown in Figure 8. Two current amplification stages are cascaded to reduce the number of current mirrors. The amplified current flows into a first-order clock-less sigma-delta modulator. This works similarly to the self-resetting integrator stage that generates an output pulse width and frequency-dependent on the value of the input current [14]. If the control bit C is 1, then the current reference at the upper side is on, and the current reference at the lower side is off. The total current flowing into the integrator is $1000I_{in} + I_{REF}$. If the control bit C is 0, then the current reference at the upper side is off, and the current reference at the lower side is on. The total current flowing into the integrator is $1000I_{in} - I_{REF}$. The voltage V_P at the output node of the integrator compares with the reference voltage V_{REFP} and V_{REFN} . Once V_P crosses the voltage window ($V_{REFN} \leq V_P \leq V_{REFP}$), the control bit signal C changes its polarity, which alters the direction of the reference current.

$$V_{Threshold}C_{INT} = T_1(1000I_{IN} + I_{REF}) \quad (2)$$

$$V_{Threshold}C_{INT} = T_2(1000I_{IN} - I_{REF}) \quad (3)$$

$$I_{in} = \frac{I_{REF}(T_1 + T_2)}{1000(T_2 - T_1)} \quad (4)$$

From Equations (2)–(4), utilizing charge conservation, one can show that the input current can be obtained from the pulse width of the control signal C .

The programmable low-frequency current amplification ratio is achieved by turning on or off the mirroring transistors M_{N2} and M_{P2} . For the first current gain stage, there are a total of 50 sets of the transistors-based current mirrors for low-frequency current signal amplification and 50 sets of capacitors for high-frequency current signal amplification, respectively as in Figure 8. When the gain of 10 of the first stage is selected, for example, the gates of the 10 NMOS transistors M_{N2} connect to V_{BN1} , while the gates of the remaining 40 NMOS transistors M_{N2} connect to Gnd ; the gates of the 10 PMOS transistors M_{P2} connect to V_{BP1} , while the gates of the remaining 40 PMOS transistors V_{BP2}

connect to V_{dd} . For the high-frequency gain, 10 sets of NMOS switches of the capacitor in the red box connect to Gnd , and the remaining 40 sets of the NMOS switches of the capacitor connected to V_{dd} .

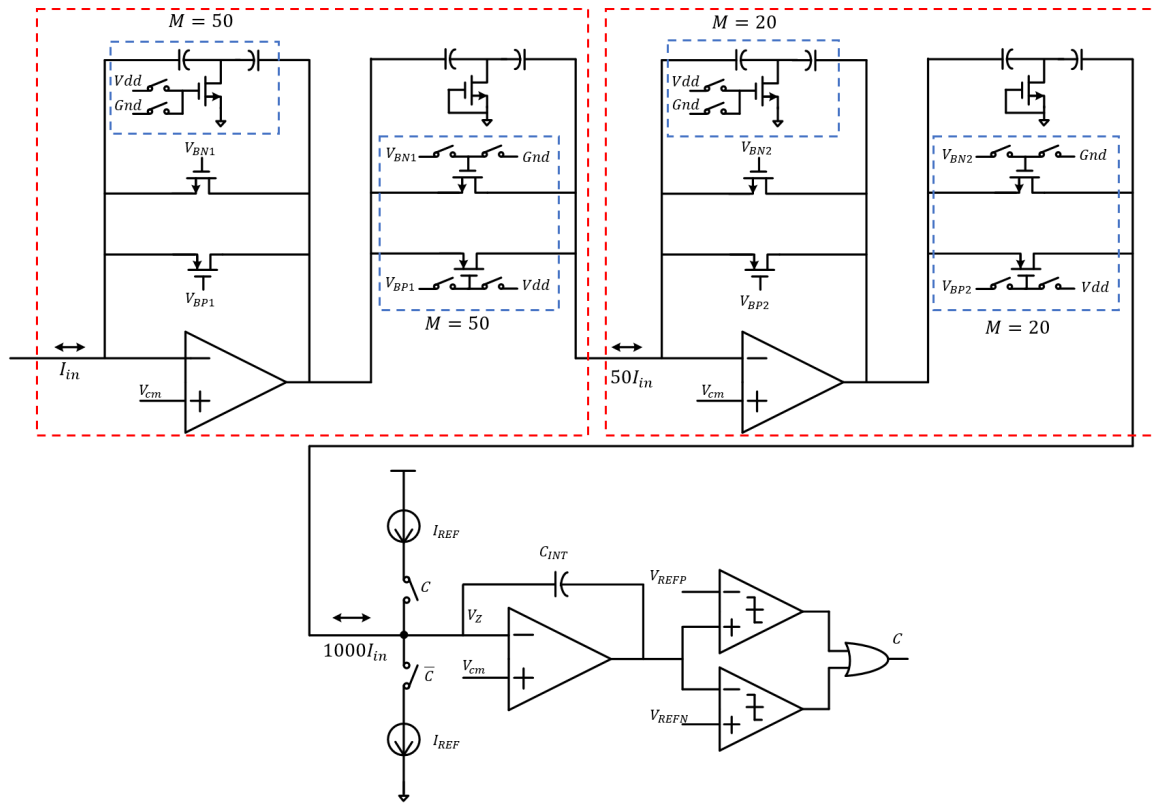


Figure 8. Top architecture of the wide dynamic range current readout circuit.

2.6. Programmable Reference Current Stage

To allow for a wide dynamic range at the input, the reference current feeds the clockless delta-sigma modulator (aka pulse width modulation stage). The reference current stage provides a selection of reference currents to the wide range input current signal. The tiny reference current is obtained by the current splitter architecture as in Figure 9 [15]. The attenuation gain is 10 in this design. The R2R topology provides the same V_{gs} voltage, so the current flowing in or out of this circuit will be linearly divided into two parts, according to the transistor size. Different scaled currents can be obtained from different transistor size ratios as in Table 2.

We use a simple divide-by-2 circuit to explain the operation of this circuit as in Figure 10. For a long-channel transistor, the drain current is proportional to the channel size W/L . Based on this statement, in Figure 10a, the transistor M_0 with size W/L is equivalent to the four identical transistors M_{01} , M_{02} , M_{03} , and M_{04} , with same size W/L in a series-parallel configuration. The current I splits equally through each of the four transistors. Transistor M_{01} and M_{02} can be simplified as an equivalent transistor M_{012} with a size of $2W/L$. Therefore, in Figure 10b, the transistor-based current split architecture by a factor of 2 is shown.

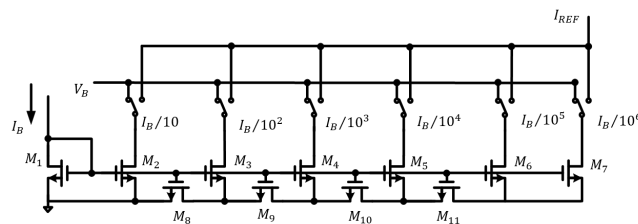


Figure 9. Current splitter for programmable reference current generation.

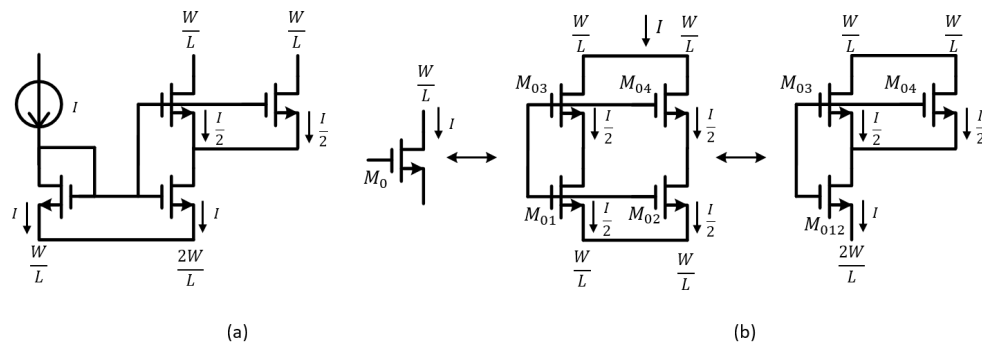


Figure 10. Half Current splitting circuit shown in (a) based on the splitting equivalent representation of a single transistor in (b).

Table 2. Table of comparison with relevant architecture.

Parameter	Value
$(W/L)_{1-6}$	$N - 1$
$(W/L)_7$	$(N - 1)/N$
$(W/L)_{8-11}$	$(N - 1)/N$

2.7. Amplifier

The low-noise amplifier composes of a low gain pre-amplification stage and a miller compensation amplifier stage as in Figure 11. The pre-amplification stage provides a gain of 4 with 13 MHz 3-dB bandwidth to reduce the noise and offset from the subsequent stage. The open-loop DC gain is 95 dB, unity gain bandwidth is 47 MHz, and the phase margin is 74° .

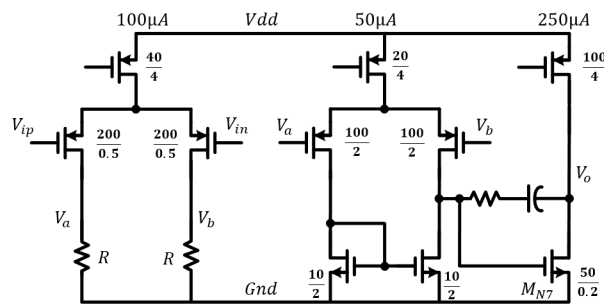


Figure 11. Low-noise amplifier.

2.8. Comparator

The comparator is a continuous-time circuit as shown in Figure 12 [16]. The internal positive feedback loop should be larger enough to enable the hysteresis performance. The hysteresis is 40 mV. The reference voltage V_{REFP} and V_{REFN} can be adjusted to select the integration voltage window.

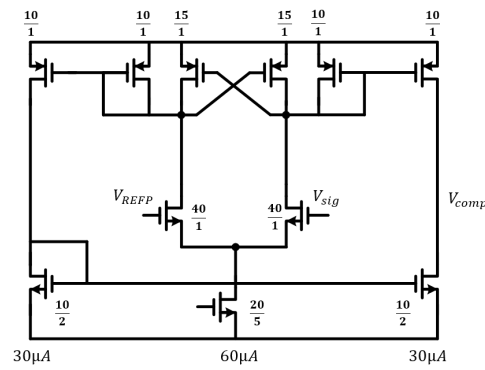


Figure 12. Hysteresis comparator.

2.9. Layout

The entire design is implemented in 0.18 μm CMOS technology, and the total layout area is $1410 \mu\text{m} \times 720 \mu\text{m}$. The transistors and the capacitors of the current amplification stage consume most of the layout area in Figure 13.

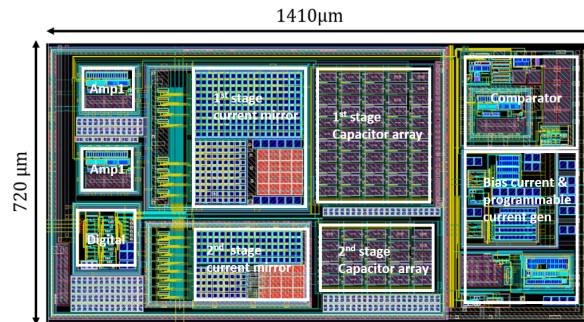
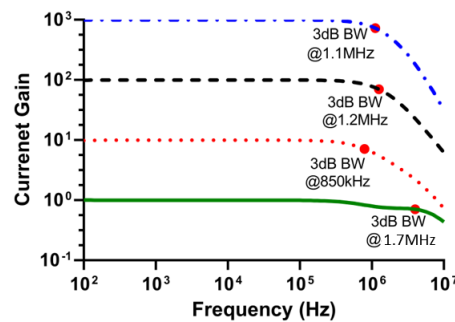


Figure 13. Current reader layout.

3. Simulation Result

The circuit was simulated with post-layout extraction. This captures the RC parasitic effects in addition to any coupling capacitance. The current gain for wide dynamic range input current and the noise performance are simulated. By controlling the digital codes, the current gain can be programmed to be $1000\times$, $100\times$, $10\times$, and $1\times$ as in Figure 14. The proposed switch connections enable the flat current gain in various current gain settings.

Figure 14. Current gains of $1000\times$, $100\times$, $10\times$, and $1\times$.

With high current pre-amplification, the input-referred current noise at the input is given by Equation (5). Note that the noise from the integration stage has been attenuated by the current-amplification gain. The feedback transistors and the input stage amplifier dominate the

input reference current noise contribution. qI_{in} is the shot noise from $M_{P(N)1}$ in Figure 8 operating in the subthreshold region. The voltage noise e_n^2 from the op-amp over the input capacitance C_{in} sets the minimal noise of the circuit when the input current I_{in} is small.

$$i_{eq}^2 = qI_{in} + (2\pi f C_{in})^2 (e_n)^2. \quad (5)$$

The equivalent input voltage noise from the front-end amplifier is shown in Equation (6). The pre-amplification stage from Figure 10 has a dominant noise contribution. k is Boltzmann constant, and K is a process related constant which influences the flicker noise.

$$e_n^2 = \frac{16kT}{3gm_{M_{P1}}} + \frac{2K}{WLC_{ox}f} + \frac{8kT}{(gm_{M_{P1}})^2 R}. \quad (6)$$

The noise density and integrated noise simulation are shown in Figures 15 and 16, respectively.

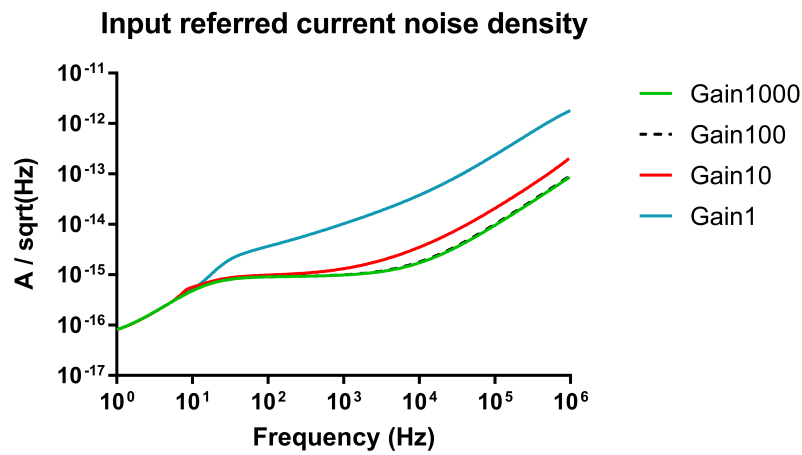


Figure 15. Input referred noise density of the current reader with the gain of 1000×, 100×, 10× and 1×.

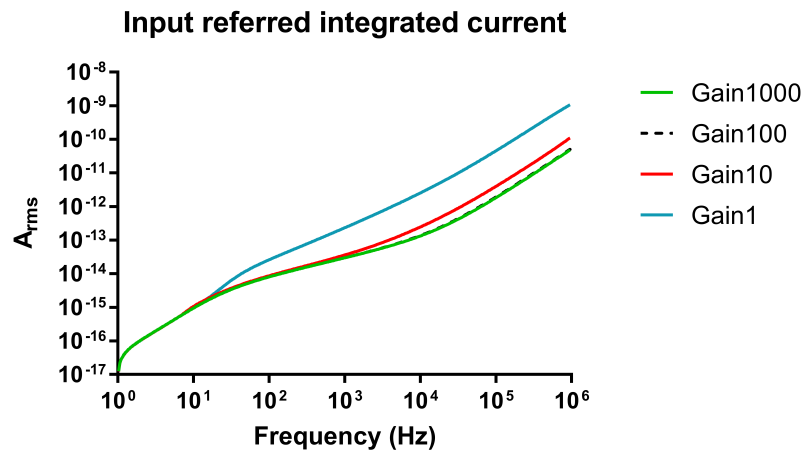


Figure 16. Input-referred integrated noise of the current reader with the gain of 1000×, 100×, 10× and 1×.

Table 3 lists the integrated noise (rms) with the signal bandwidth of 100 Hz, 10 KHz, and 1 MHz, and with the current gain of 1000×, 100×, 10×, and 1×, respectively. One can choose a fast operation mode for the small input current with some trade-off with the bandwidth, or one can process high bandwidth signal with a slower operation.

Table 3. Input referred integrated current noise (rms).

	Gain 1000×	Gain 100×	Gain 10×	Gain 1×
100 Hz	8 fA	8 fA	9 fA	26 fA
10 KHz	0.13 pA	0.13 pA	0.25 pA	2.53 pA
1 MHz	0.051 nA	0.054 nA	0.118 nA	1.113 nA

In Figure 17, sinusoidal signals of the amplitude of 100 fA (10 Hz), 1 nA (1 KHz), and 1 μ A (1 MHz) are used as the input signal, respectively, and results show that recovered signal matches well with the input signal [14].

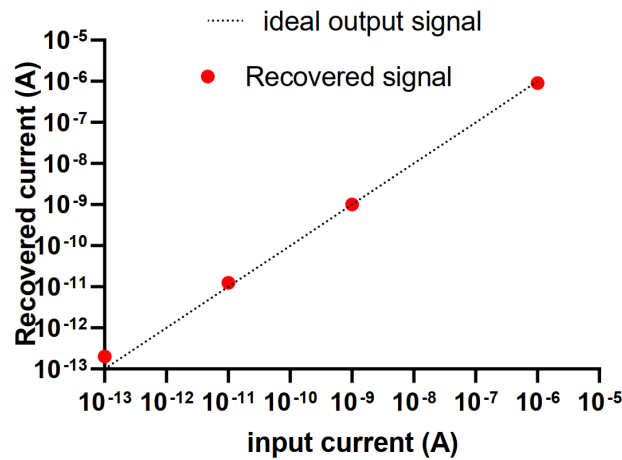
**Figure 17.** Recovered input current.

Table 4 lists the proposed readout circuit performance and compares it with other recent state-of-the-art demonstrations. We added a new metric to the table; “Speed improvement factor”. It is defined as the improvement in output data rate from the use of variable gain settings. This can be estimated as follows. $V_{Threshold}$ is the threshold voltage of the comparator, and C_{INT} is the integration capacitor. I is the integration current and T_x is the integration time for the 1× current gain setting; 1000 I is the integration current and T_y is the integration time for the 1000× current gain setting. We can write Equations (7) and (8) for these two settings.

$$IT_x = V_{Threshold}C_{INT} \quad (7)$$

$$1000IT_y = V_{Threshold}C_{INT} \quad (8)$$

$$T_y = \frac{T_x}{1000} \quad (9)$$

Equation (9) implies that the circuit can generate the output pulse at a rate 1000 times using the 1000× current gain setting.

Table 4. Table of comparison with relevant architecture.

	[4]	[5]	[17]	[18]	[19]	This Work *
Technology (μm)	0.18	0.35	0.35/0.5	0.18	0.18	0.18
Power supply (V)	1.8	3	3	1.8	3.3	1.8
3 dB Signal bandwidth (MHz)	1.4	4	0.1	1.25	0.0039	0.85
Dynamic range (dB)	155.1	95.9	80	160	74	140
Area (mm^2)	0.091	0.34	0.6	0.2	0.5	1.015
Power consumption (mW)	9.4	13.5	7	0.3	23	10.3
Speed improvement factor	1 $\times$	1 $\times$	1 $\times$ 1	1 $\times$	1 $\times$	1000 $\times$

* Simulation result.

4. Conclusions

This paper presents a low-noise current readout circuit using programmable gain setting switches to process a wide input range of currents of 140 dB. The switch arrangement for choosing the programmable gain has been proposed that introduces no phase distortion and it offers flat high-frequency gain. The programmable amplification current stage offers a fast operation of the small current signal and provides a large input dynamic range. The one-bit clockless delta-sigma modulator produces digital output, the input signal is calculated directly from the duty cycle of the pulse output signal. The current amplification enables a higher output data rate for smaller currents. Simulation results in a 0.18 μm CMOS process to validate the performance.

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