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Accurate Analysis and Design of Integrated Single Input Schmitt Trigger Circuits

Mohamed R. Elmezayen [1,2,*], Wei Hu [1], Amr M. Maghraby [2], Islam T. Abougindia [2] and Suat U. Ay [1]

[1] Department of Electrical and Computer Engineering, University of Idaho, Moscow, ID 83844, USA; hu2144@vandals.uidaho.edu (W.H.); suatay@uidaho.edu (S.U.A.)
[2] Electronic Engineering Department, Military Technical Collage, Cairo 11838, Egypt; amr.maghraby@mtc.edu.eg (A.M.M.); iabougindia@mtc.edu.eg (I.T.A.)
* Correspondence: moha1586@vandals.uidaho.edu

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Abstract: Schmitt trigger (ST) circuits are widely used integrated circuit (IC) blocks with hysteretic input/output (I/O) characteristics. Like the I/O characteristics of a living neuron, STs reject noise and provide stability to systems that they are deployed in. Indeed, single-input/single-output (SISO) STs are likely candidates to be the core unit element in artificial neural networks (ANNs) due not only to their similar I/O characteristics but also to their low power consumption and small silicon footprints. This paper presents an accurate and detailed analysis and design of six widely used complementary metal-oxide-semiconductor (CMOS) SISO ST circuits. The hysteresis characteristics of these ST circuits were derived for hand calculations and compared to original design equations and simulation results. Simulations were carried out in a well-established, 0.35 µm/3.3 V, analog/mixed-signal CMOS process. Additionally, simulations were performed using a wide range of supplies and process variations, but only 3.3 V supply results are presented. Most of the new design equations provide better accuracy and insights, as broad assumptions of original derivations were avoided.

Keywords: schmitt trigger; artificial neural networks; hysteresis circuits

1. Introduction

Artificial neural networks (ANNs) are the core of artificial intelligence (AI) in next generation systems that mimic the parallel processing capabilities of the human brain. One important characteristic of the distributed processing element of the brain, the neuron, is to deal with chaos through its hysteretic I/O response [1]. It is shown that this characteristic of a neuron makes ANNs stable [2] and converge more rapidly [3]. Additionally, the artificial neuron has to be small and consume minimal power to be able to be integrated into mass numbers [4].

The Schmitt trigger (ST) has been used in both analog and digital domains to improve the noise immunity of circuits, thanks to its programmable or hard-wired hysteresis characteristics [5–11]. This characteristic has been utilized in many CMOS circuit blocks including oscillators [12–15], input/output pads of integrated circuits [16,17], image sensors [18–24], triangular carrier-based PWM modulators [25], subthreshold SRAMs [26–29], CMOS transceivers [30–34], impedance-to-frequency converters [35], digital to analog converters (DACs) [36], neuron-based analog to digital converters (ADCs) [37–39], powerline communication systems [40], binary logic circuits (i.e., adders [41] and gates [42]), and sensors [43,44].

CMOS STs can be categorized based on their mode of operation (voltage or current), inputs (single or differential input), outputs (inverting or noninverting), and hysteresis controls (fixed or programmable). The simplest and most compact STs are the ones with fixed hysteresis, and single voltage input and

single voltage output types. Six well known single input/single output ST topologies are investigated in this paper: Dokic [5] (three types: N, P, and CMOS), Steyaert [6], Pedroni [7], and Al-Sarawi [8]. In this paper, we show how to derive the hysteresis voltages accurately for these STs, and determine their design limitations and sensitivities to process variations. For the analysis and design of an ST circuit, three fundamental input-output (I/O) parameters are considered: high-to-low switching voltage (V_{HL}), low-to-high switching voltage (V_{LH}), and hysteresis voltage ($\Delta V_H = V_{HL} - V_{LH}$), as shown in Figure 1. The hysteresis offset (V_{HO}) in Figure 1 can be calculated as ($V_{HO} = V_{LH} + \Delta V_H/2$).

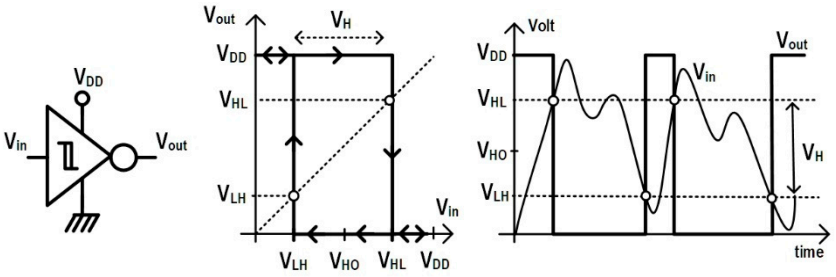


Figure 1. I/O characteristics of a voltage mode, inverting ST circuit.

Detailed analysis and the hand calculation equations of each topology are presented in Section 2. Each topology is extensively simulated at different corners of the selected CMOS process. The simulation results are presented in Section 3, as are the comparisons between hand calculations and the simulation results of each topology, in addition to the comparisons between the six topologies. The conclusion is presented in Section 4.

2. Analysis of Schmitt Trigger (ST) Circuits

Six well known single input and single output ST topologies and their variants are analyzed in this section, providing transistor level and more accurate and intuitive design equations. They are Dokic [5] (three types), Steyaert [6], Pedroni [7], and Al-Sarawi [8] STs. We used long-channel MOSFET models and high supply voltage process in this section. Equations (1) and (2) are the quadratic MOSFET transistor model equations that were used for the analysis in saturation (SAT) and linear/triode (LIN) regions, respectively [45]. The threshold voltage equation was modified slightly, linearizing bulk-to-source voltage dependency as $V_{thx} = V_{th0} + \psi \cdot V_{SB}$. Here, ψ is defined as $\psi = n \cdot GAMMA \cdot PHI$, where $GAMMA$ is the back-gate effect parameter, PHI is the surface potential, and n is a fitting parameter ($0.3 < n < 0.5$) which is determined through the simulation.

$$I_{DS} = \beta(V_{GS} - V_{TH})^2 \quad \text{for} \quad V_{DS} \geq V_{GS} - V_{TH} \quad \text{(Saturation)} \tag{1}$$

$$I_{DS} = \beta\left(2(V_{GS} - V_{TH})V_{DS} - V_{DS}^2\right) \quad \text{for} \quad V_{DS} < V_{GS} - V_{TH} \quad \text{(Linear)} \tag{2}$$

where

$$\beta = \frac{1}{2} KP\left(\frac{W}{L}\right) \tag{3}$$

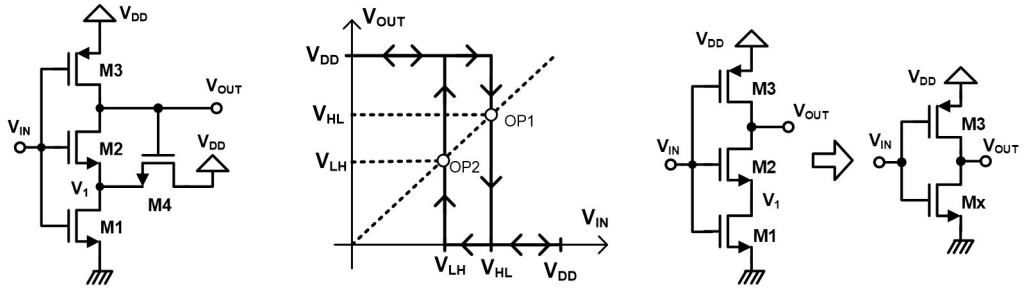
2.1. Dokic Schmitt Trigger Circuits

Dokic proposed three ST topologies in [5]: N-type, P-type, and CMOS-type. These topologies are investigated and detailed, and more accurate design equations for V_{HL}, V_{LH}, and ΔV_H are derived.

2.1.1. N-Type ST by Dokic

Figure 2a shows the N-type Dokic ST [5]. It is composed of four transistors and its hysteresis is shown in Figure 2b. Depending on how the input signal changes, two I/O characteristics can be observed. If the input goes from low (0) to high (V_{DD}), the output changes from high to low at V_{HL}.

If the input goes from high (V_{DD}) to low (0), the output changes from low (0) to high (V_{DD}) at V_{LH}. The V_{HL} and V_{LH} can be found when the input and output voltages are equal to each other at operating points OP1 and OP2, respectively, as marked in Figure 2b.



(**a**) (**b**) (**c**)

Figure 2. N-type Dokic ST: (**a**) circuit diagram, (**b**) input–output characteristics, and (**c**) modeled equivalent circuit when M4 is OFF.

V_{HL} Voltage

From Figure 2a, in the steady-state and when input is 0 V, the transistors M1 and M2 are OFF, M3 is in the deep LIN region where V_{ds3} is close to 0 V, and M4 can be considered in the subthreshold region, where $V_{gs4} < V_{thn4}$ while the output is V_{DD}. The node voltage V_1 would be ($V_{DD} - V_{thn4}$) and rising. When the input is increased and greater than V_{thn0}, M1 turns ON, discharging V_1 to a switching point. Since $V_{sb2} = V_{sb4} > V_{thn0}$, M2 is still OFF and M4 is in SAT. M2 turns ON only when V_{in} is V_{thn0} above the V_1 voltage. Before M2 turns on, the V_1 can be found by equating the drain currents of transistors M1 and M4. The general V_1 equation, including body-effect where $V_{thn4} \approx V_{thn0} + \psi \cdot V_1$, is:

$$V_1 = \frac{V_{DD} - V_{thn0} \cdot (1 - \alpha_{1n}) - \alpha_{1n} V_{in}}{(1 + \Psi)} \tag{4}$$

where

$$\alpha_{1n} = \sqrt{\frac{\beta_1}{\beta_4}} \tag{5}$$

When V_{in} further increases, V_1 drops further, and finally, M2 turns ON. Then, the output node starts discharging, first turning M4 OFF and then turning M3 ON during this high to low transition. M2 turns ON when $V_{in(min)} > V_1 + V_{thn2}$. $V_{in(min)}$ could be considered as the threshold voltage of the series combination of M1 and M2, or V_{thnx}. Using (4), it can be found as follows:

$$V_{in(min)} \geq V_1 + V_{thn2} = V_1 + V_{thn0} + \Psi \cdot V_1 = V_{DD} + \alpha_{1n} V_{thn0} - \alpha_{1n} V_{in(min)} \tag{6}$$

$$V_{thnx} = V_{in(min)} \geq \frac{V_{DD} + \alpha_{1n} \cdot V_{thn0}}{(1 + \alpha_{1n})} \tag{7}$$

When $V_{in} = V_{HL}$, Dokic [5] assumes that M1 works in LIN, and M2 and M3 are in SAT regions, while M4 is OFF. However, series transistors M1 and M2 (Figure 2c) work in two different operation regions (M1 in LIN, M2 in SAT) that could be simplified into a single NMOS (M_x) transistor working in SAT with an equivalent threshold voltage of V_{thnx}, and $\beta = \beta_{xn}$, as follows:

$$I_{ds1} = \beta_1 \cdot \left(2 \cdot (V_{in} - V_{thn0}) \cdot V_1 - V_1^2\right) \tag{8}$$

$$V_1 = +(V_{in} - V_{thn0}) \pm \sqrt{(V_{in} - V_{thn0})^2 - \frac{I_{ds1}}{\beta_1}} \tag{9}$$

$$I_{ds2} = \frac{1}{2} KP_n \left(\frac{W}{L}\right)_2 (V_{in} - V_1 - V_{thn2})^2 = \beta_2 (V_{in} - V_1 - V_{thn0} - \Psi \cdot V_1)^2 \tag{10}$$

using (9) in (10):

$$I_{ds2} = \beta_2 \cdot \left(V_{in} - (1 + \Psi) \cdot \left[+ (V_{in} - V_{thn0}) \pm \sqrt{(V_{in} - V_{thn0})^2 - \frac{I_{ds1}}{\beta_1}} \right] - V_{thn0} \right)^2 \tag{11}$$

and assuming that $V_{thn1} \cong V_{thn2} = V_{thn0}$, where $\psi = 0$, and $I_{ds1} = I_{ds2} = I_{dsx}$, Equation (11) becomes,

$$I_{dsx} = \beta_2 \cdot \left[(V_{in} - V_{thn0})^2 - \frac{I_{dsx}}{\beta_1} \right] \tag{12}$$

$$I_{ds1} = I_{ds2} = I_{dsx} = \left[\frac{\beta_1 \cdot \beta_2}{\beta_1 + \beta_2} \right] (V_{in} - V_{thn0})^2 = \beta_{xn} \cdot (V_{in} - V_{thn0})^2 \tag{13}$$

where

$$\beta_{xn} = \left[\frac{\beta_1 \cdot \beta_2}{\beta_1 + \beta_2} \right] \tag{14}$$

The V_{HL} of the N-type Dokic ST can now be found by equating the drain currents of the transistors M3 and Mx shown in Figure 2c, assuming that both are working in SAT region at OP1:

$$V_{HL} = \frac{V_{DD} - |V_{thp0}| + \alpha_{2n} \cdot V_{thn0}}{(1 + \alpha_{2n})} + \frac{\alpha_{2n} \cdot (V_{DD} - V_{thn0})}{(1 + \alpha_{1n})(1 + \alpha_{2n})} \tag{15}$$

$$\text{where, } \alpha_{1n} = \sqrt{\frac{\beta_1}{\beta_4}} \text{ and } \alpha_{2n} = \sqrt{\frac{\beta_{xn}}{\beta_3}} \tag{16}$$

V_{LH} Voltage

The V_{LH} can be found by considering M4 as being OFF right before the output transition from low to high which occurs at OP2 ($V_{in} = V_{out} = V_{LH}$), and by equating the drain current of M3 to that of M_x, which both work in SAT. It is important to note here that the current of M_x is equal to that of M2 (as in (13)) in which β_{xn}, V_{thn0}, and α_{1n}, and α_{2n} from Equation (16) are used.

$$V_{LH} = \frac{V_{DD} - |V_{thp0}| + \alpha_{2n} \cdot V_{thn0}}{(1 + \alpha_{2n})} \tag{17}$$

Hysteresis Voltage

The hysteresis voltage of the N-type Dokic ST can then be derived by using (15) and (17) as:

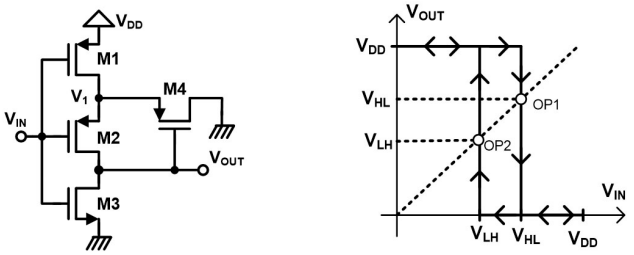
$$\Delta V_H = V_{HL} - V_{LH} = \frac{\alpha_{2n} \cdot (V_{DD} - V_{thn0})}{(1 + \alpha_{1n})(1 + \alpha_{2n})} \tag{18}$$

Compared to Dokic's original hysteresis equation (Equation (7) in [5]), (18) provides a transistor-level design strategy, that the hysteresis voltage could be maximized by minimizing α_{1n} and by maximizing α_{2n} parameters while ensuring that the individual transistor parameters satisfy $\beta_4 > \beta_1$ and $\beta_3 < \beta_{xn}$.

2.1.2. P-Type ST by Dokic

Figure 3 shows the P-type Dokic ST [5]. It is the complementary version of the N-type and has the same hysteresis characteristics. Transistors are numbered the same as the N-type as shown in Figure 2 and the analysis is carried out following the same process presented in the previous section. The V_{HL}

and V_{LH} of the P-type Dokic ST can be found when input and output voltages are equal at operating points OP1 and OP2 as shown in Figure 3.



(**a**) (**b**)

Figure 3. P-type Dokic ST [5]. (**a**) Circuit diagram and (**b**) input-output characteristics.

The design equations and parameters for the P-type Dokic ST can be derived as:

$$V_{LH} = \frac{\alpha_{2p} \cdot V_{thn0}}{\left(1+\alpha_{2p}\right)} + \frac{\alpha_{1p} \cdot \left(V_{DD} - \left|V_{thp0}\right|\right)}{\left(1+\alpha_{1p}\right)\left(1+\alpha_{2p}\right)} \tag{19}$$

$$V_{HL} = \frac{V_{DD} - \left|V_{thp0}\right| + \alpha_{2p} \cdot V_{thn0}}{\left(1+\alpha_{2p}\right)} \tag{20}$$

and the hysteresis voltage:

$$\Delta V_H = V_{HL} - V_{LH} = \frac{\left(V_{DD} - \left|V_{thp0}\right|\right)}{\left(1+\alpha_{1p}\right)\left(1+\alpha_{2p}\right)} \tag{21}$$

where

$$\alpha_{1p} = \sqrt{\frac{\beta_1}{\beta_4}}\,,\ \alpha_{2p} = \sqrt{\frac{\beta_3}{\beta_{xp}}},\ \beta_{xp} = \left[\frac{\beta_1 \cdot \beta_2}{\beta_1 + \beta_2}\right],\ \text{and}\ \left|V_{thpx}\right| = V_{DD} - \frac{\alpha_{1p} \cdot \left(V_{DD} - \left|V_{thp0}\right|\right)}{\left(1+\alpha_{1p}\right)} \tag{22}$$

Compared to Dokic's original hysteresis equation (Equation (13) in [5]), (21) provides a transistor-level design strategy, that the hysteresis voltage could be maximized by minimizing both α_{1p} and α_{2p} parameters while ensuring the individual transistor parameters satisfies $\beta_4 > \beta_1$ and $\beta_{xp} < \beta_3$ conditions.

2.1.3. CMOS-Type ST by Dokic

Figure 4 shows the CMOS type Dokic ST circuit [5]. It is composed of six transistors and its hysteresis is shown in Figure 4b. Depending on how the input signal changes, two I/O characteristics can be observed. If the input goes from low (0) to high (V_{DD}) voltage level, the output state is changed at V_{HL} where the output goes from high (V_{DD}) to low (0) and vice versa, it switches from low (0) to high (V_{DD}) at V_{LH}. The V_{HL} and V_{LH} can be found when the input and output voltages are equal at operating points OP1 and OP2, as shown in Figure 4b.

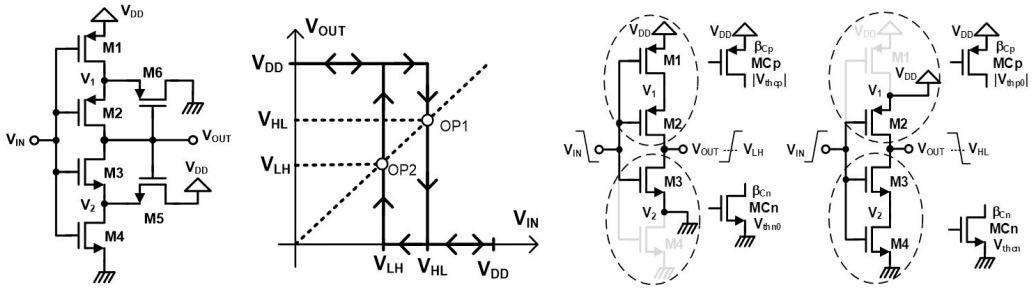


Figure 4. CMOS type Schmitt trigger circuit by Dokic [5]. (**a**) Circuit diagram, (**b**) input-output characteristics, (**c**) equivalent circuit for V_{LH} transition, and (**d**) equivalent circuit for V_{HL} transition.

V_{LH} Voltage

When the input is V_{DD}, the output is close to 0 V and M1, M2, and M5 are OFF, while M6 operates in the subthreshold region. M3 and M4 are in the deep LIN region where $V_{ds3,4} \approx 0$, and $I_{ds3,4} \approx 0$. V_1 approaches but remains below $|V_{thp6}|$ and is continuously discharged by the subthreshold current of M6. When V_{in} drops a $|V_{thcp}|$ below V_{DD}, the series combination of M1 and M2 (MCp) turns ON and works in the SAT region. During this time, M3 still works in SAT, while M5 is OFF and M4 is in LIN, which keeps V_2 voltage close to 0 V. Thus, the V_{LH} voltage could be determined by equating the SAT current of the transistor MCp to that of MCn formed by the series combination of M3 and M4, while assuming $V_2 = 0$. This means that MCn will have V_{thn0} as the threshold voltage, while the threshold voltage of MCp will be $|V_{thcp}|$, the same as $|V_{thpx}|$ in Equation (22). Thus, the V_{LH} can be derived as:

$$V_{LH} = \frac{\alpha_2 \cdot V_{thn0}}{(1+\alpha_2)} + \frac{\alpha_1 \cdot \left(V_{DD} - \left|V_{thp0}\right|\right)}{(1+\alpha_1)(1+\alpha_2)} \tag{23}$$

where

$$\alpha_1 = \sqrt{\frac{\beta_1}{\beta_6}},\ \alpha_2 = \sqrt{\frac{\beta_{cn}}{\beta_{cp}}},\ \ \beta_{cp} = \left[\frac{\beta_1 \cdot \beta_2}{\beta_1 + \beta_2}\right], \text{and}\ \ \beta_{cn} = \left[\frac{\beta_3 \cdot \beta_4}{\beta_3 + \beta_4}\right] \tag{24}$$

V_{HL} Voltage

When the input is 0 V, the output is close to V_{DD} and transistors M3, M4, and M6 are OFF, while M5 operates in the subthreshold region. Transistors M1 and M2 are in the deep LIN region where $V_{sd1,2} \approx 0$, and $I_{sd1,2} \approx 0$. V_2 approaches but remains below V_{DD} and is continuously charged by the subthreshold current of M5. When V_{in} increases a V_{thcn} above 0 V, the series combination of M3 and M4 (MCn) turns ON and into the SAT region. During this time, M2 still works in SAT, while M6 is OFF and M1 is in the LIN region, which keeps V_1 voltage close to V_{DD}. Thus, the V_{HL} voltage could be determined by equating the SAT current of transistor MCn to that of MCp formed by the series combination of M1 and M2, while assuming $V_1 = V_{DD}$. This means that MCp will have $|V_{thp0}|$ as threshold voltage, while the threshold voltage of MCn will be V_{thcn}, the same as V_{thnx} in Equation (7). Thus, V_{HL} can be derived as:

$$V_{HL} = \frac{V_{DD} - \left|V_{thp0}\right| + \alpha_2 \cdot V_{thn0}}{(1+\alpha_2)} + \frac{\alpha_2 \cdot (V_{DD} - V_{thn0})}{(1+\alpha_2)(1+\alpha_3)} \tag{25}$$

where

$$\alpha_3 = \sqrt{\frac{\beta_4}{\beta_5}} \text{ and } V_{thcn} = \frac{V_{DD} + \alpha_3 \cdot V_{thn0}}{(1+\alpha_3)} \tag{26}$$

Hysteresis Voltage

The hysteresis voltage can then be derived by using Equations (23) and (25), as follows:

$$\Delta V_H = \frac{1}{(1+\alpha_2)}\left(\frac{\alpha_2 \cdot (V_{DD} - V_{thn0})}{(1+\alpha_3)} + \frac{V_{DD} - |V_{thp0}|}{(1+\alpha_1)}\right) \tag{27}$$

Compared to Dokic's original hysteresis equation (Equation (16) in [5]), (27) provides a transistor-level design strategy, that hysteresis voltage could be adjusted accordingly. The design parameters sensitivity (V_{HL}, V_{LH}, and ΔV_H) in terms of the individual transistor parameters (α_1, α_2, α_3) can also be determined by using the new design Equations (23), (25) and (27), which provides better insight for the design of CMOS-type Dokic ST.

The new design equations for N-, P-, and CMOS-type Dokic ST presented in this section also provides better hand calculation accuracy in the wide process, supply, and device parameters variation as presented in the next section.

2.2. CMOS-Type Schmitt Trigger by Steyaert

Figure 5a shows the CMOS type ST circuit by Steyaert [6]. It is composed of five transistors and has the hysteresis that is shown in Figure 5b. Depending on how the input signal changes, two I/O characteristics can be observed. If the input goes from low (0) to high (V_{DD}), the output state changes at V_{LH}, where the output goes from low (0) to high (V_{DD}) supply voltage. If the input goes from high (V_{DD}) to (0) low, in this case, the output changes its value at V_{HL}, where the output value goes from high (V_{DD}) to (0) low. The V_{HL} and V_{LH} can be found when input and output voltages are equal at the operating points OP1 and OP2, as shown in Figure 5b. During the analysis, we will assume that, without M5, the switching voltages of the two inverters are the same. Thus, the device sizes of M1 and M3 and M1 and M3 are the same. We also assume that there is a slight delay between voltages V_{in} and V_{out} due to the loading at the V_1 and output nodes.

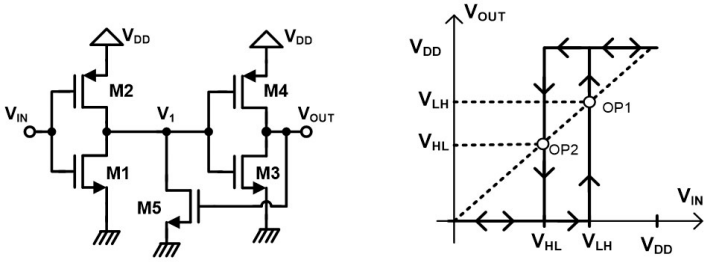


Figure 5. CMOS-type ST by Steyaert [6]. (**a**) Circuit diagram and (**b**) input-output characteristics.

2.2.1. V_{LH} Voltage

When the input is low (0 V), V_1 is high (V_{DD}). Transistors M2 and M3 are ON while M1, M4, and M5 are OFF. At OP1, the V_{LH} voltage is determined by equating the SAT currents of M1 and M2, like a regular CMOS inverter. Thus, the V_{LH} can be derived as:

$$V_{LH} = \frac{\alpha_1 \cdot \left(V_{DD} - |V_{thp0}|\right) + V_{thn0}}{(1+\alpha_1)} \tag{28}$$

where

$$\alpha_1 = \sqrt{\frac{\beta_2}{\beta_1}} \tag{29}$$

This formulation is the same as the one presented by Steyaert as Equation (1) in [6].

2.2.2. V_{HL} Voltage

When the input is high (V_{DD}), V_1 is low (0 V). Transistors M2 and M3 are OFF while M1, M4, and M5 are ON. At OP2, M2 turns ON, and the V_{HL} voltage could be determined by equating the SAT currents of M1, M2, and M5 while ignoring the channel-length modulation parameter (λ) of the transistors as follows:

$$V_{HL} = V_{HLA}\left(1 + \sqrt{1 - \frac{V_{HLB}}{V_{HLA}}}\right) \tag{30}$$

where

$$\alpha_2 = \sqrt{\frac{\beta_5}{\beta_1}} \tag{31}$$

and

$$V_{HLA} = \frac{\alpha_1^2 \cdot \left(V_{DD} - \left|V_{thp0}\right|\right) - V_{thn0}}{\left(\alpha_1^2 - 1\right)} \quad V_{HLB} = \frac{\alpha_1^2\left(V_{DD} - \left|V_{thp0}\right|\right)^2 - V_{thn0}^2 - \alpha_2^2(V_{DD} - V_{thn0})^2}{\left(\alpha_1^2 - 1\right)} \tag{32}$$

The formulation presented by Steyaert (Equation (2) in [6]) is given below, which is much simpler than Equation (30) above, but inaccurate for hand calculations as discussed in the next section.

$$V_{HL} = V_{LH} - \frac{\alpha_2 \cdot (V_{DD} - V_{thn0})}{2 \cdot (1 + \alpha_1)} \tag{33}$$

2.2.3. Hysteresis Voltage

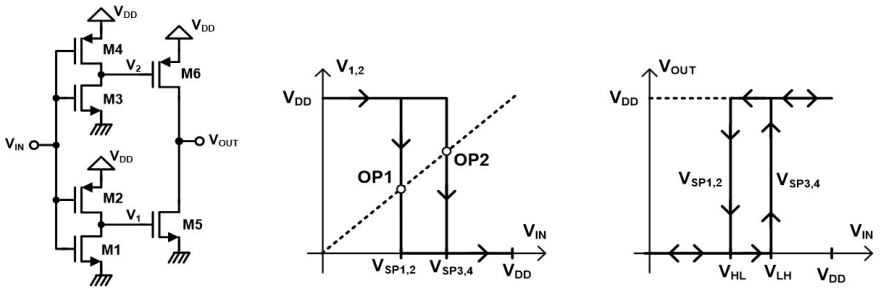
The hysteresis voltage can then be derived by using Equations (28) and (30) as:

$$\Delta V_H = V_{HL} - V_{LH} = V_{HLA}\left(1 + \sqrt{1 - \frac{V_{HLB}}{V_{HLA}}}\right) - \frac{\alpha_1 \cdot \left(V_{DD} - \left|V_{thp0}\right|\right) + V_{thn0}}{(1 + \alpha_1)} \tag{34}$$

Compared with the Steyaert's formula, Equation (34) is more accurate, but less intuitive in designing the ST circuit. More accurate hysteresis voltage could be derived if we include the channel-length modulation mechanism, but the equation becomes more complicated and less intuitive.

2.3. Non-Inverting Schmitt Trigger by Pedroni

Figure 6 shows the non-inverting ST by Pedroni [7]. It is composed of six transistors and its hysteresis is shown in Figure 6a. When the input goes from low (0) to high (V_{DD}) voltage level, the output state changes at V_{LH} where the output goes from low (0) to high (V_{DD}). If the input goes from high (V_{DD}) to (0) low, the output changes at V_{HL}, where the output goes from high (V_{DD}) to (0) low. The V_{HL} is defined by the switching point of the inverter composed of M1 and M2 and the V_{LH} is set by the inverter transistors M3 and M4, as shown in Figure 6b. Besides, the hysteresis exists only if $V_{SP3,4} > V_{SP1,2}$.



(**a**) (**b**) (**c**)

Figure 6. The non-inverting ST by Pedroni [7]. (**a**) Circuit diagram, (**b**) input-output characteristics of each input inverter, and (**c**) overall characteristics of the ST.

Hysteresis Voltages

When the input is low (0 V), V_1 and V_2 are high (V_{DD}). M2, M4, and M5 are ON while M1, M3, and M6 transistors are OFF, and the output is 0 V. At OP1, V_1 becomes 0 V which turns off M5, and then the output floats maintaining its last state which is 0 V. The output only changes when V_2 becomes 0 V at OP2 where M6 turns ON and charges the output to V_{DD}. Thus, VLH occurs at the switching point (V_{SP}) of the upper inverter composed of transistors M3 and M4. Thus, $V_{LH} = V_{SP3,4}$ can be derived as follows:

$$V_{HL} = \frac{\alpha_1 \cdot \left(V_{DD} - \left|V_{thp0}\right|\right) + V_{thn0}}{(1+\alpha_1)} \tag{35}$$

where

$$\alpha_1 = \sqrt{\frac{\beta_4}{\beta_3}} \tag{36}$$

Similarly, the V_{HL} can be found as:

$$V_{HL} = \frac{\alpha_2 \cdot \left(V_{DD} - \left|V_{thp0}\right|\right) + V_{thn0}}{(1+\alpha_2)} \tag{37}$$

where

$$\alpha_2 = \sqrt{\frac{\beta_2}{\beta_1}} \tag{38}$$

The hysteresis voltage could then be derived as:

$$\Delta V_H = V_{HL} - V_{LH} = -\frac{\left(V_{DD} - \left|V_{thp0}\right| + V_{thn0}\right)(\alpha_1 - \alpha_2)}{(1+\alpha_1)(1+\alpha_2)} \tag{39}$$

2.4. Low-Power CMOS-Type Schmitt Trigger by Al-Sarawi

Figure 7 shows the low-power CMOS-type ST by Al-Sarawi [8]. It is composed of six transistors and its hysteresis is shown in Figure 7d. Depending on how the input signal changes, two I/O characteristics can be observed: If the input goes from low (0) to high (V_{DD}) voltage level, the output state changes at V_{HL} where the output goes from high (V_{DD}) to low (0). If the input goes from high (V_{DD}) to low (0), in this case, the output changes at V_{LH}, where the output goes from low (0) to high (V_{DD}). The V_{HL} and V_{LH} can be found when the input and the output voltages are equal at the operating points OP1 and OP2, as shown in Figure 7b,c. For the analysis, the switching voltage of the two inverters is assumed to be the same. Thus, the device sizes of M1 and M3, and M2 and M4 are the same.

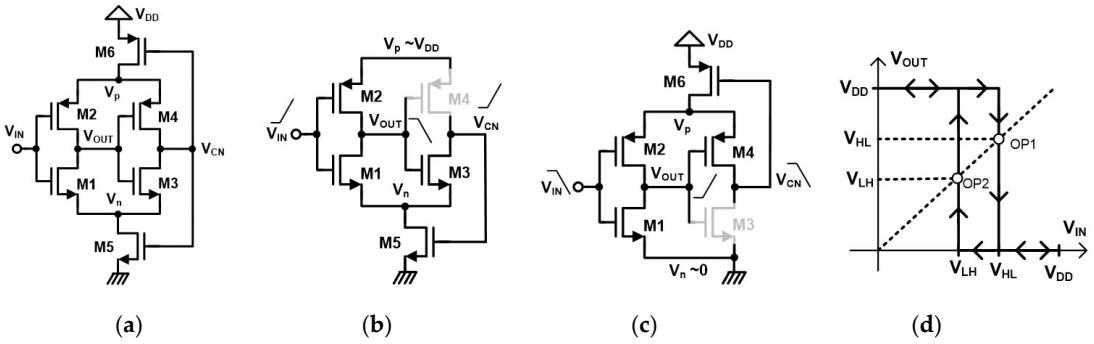


Figure 7. Low-power CMOS-type ST by Al-Sarawi [8]. (**a**) Circuit diagram, (**b**) equivalent circuit for V_{HL}, (**c**) equivalent circuit for V_{LH}, and (**d**) input-output characteristics.

2.4.1. V_{HL} Voltage

When the input is low (0 V), V_{out} is high (V_{DD}). Since V_{out} is a high impedance node and M1 is OFF, V_{CN} drifts towards low (0) potential through the diode-connected M5 that works in the subthreshold region. While M3 works in the deep LIN region that V_{DS3} is close to 0. As a result, M6 turns fully ON which pulls the node voltage V_P to V_{DD}. Thus, when input is low (0) at steady state, transistors M2, M6, and M3 are ON, M5 is in subthreshold and, other transistors are fully OFF. Assuming V_{HL} is larger than the threshold voltage of M1 at OP1, the V_{HL} switching voltage could be determined by equating the SAT currents of M1 and M2, like a regular CMOS inverter with finite V_n that keeps M5 on the edge of SAT and OFF regions.

$$V_{HL} = \frac{V_n + \alpha_1 \cdot \left(V_{DD} - \left|V_{thp0}\right|\right) + V_{thn0}}{(1 + \alpha_1)} \tag{40}$$

where

$$\alpha_1 = \sqrt{\frac{\beta_2}{\beta_1}} \tag{41}$$

V_n could be found by using the equivalent circuit shown in Figure 7b. Here, it is assumed that the V_{out} node voltage is close to V_{DD}, and M3 shorts V_{cn} to V_n effectively connecting the gate of M5 to its drain, which keeps it in the SAT region. Thus, using SAT currents of transistors M1 and M5, we can determine the V_n voltage as follows:

$$V_n = \frac{V_{in}}{(1 + \alpha_2)} + \frac{(\alpha_2 - 1) \cdot V_{thn0}}{(1 + \alpha_2)} \tag{42}$$

where

$$\alpha_2 = \sqrt{\frac{\beta_5}{\beta_1}} \tag{43}$$

Using (42) in (40) for $V_{in} = V_{HL}$, we can find the V_{HL} as follows.

$$V_{HL} = \frac{2 \cdot \alpha_2 \cdot V_{thn0} + \alpha_1 \cdot (1 + \alpha_2) \cdot \left(V_{DD} - \left|V_{thp0}\right|\right)}{\alpha_1 + \alpha_2 \cdot (1 + \alpha_1)} \tag{44}$$

Compared to Al-Sarawi's equation, Equations (42) and (44) are different than his V_n and V_{HL} equations (Equations (2) and (3) in [8]) due to his broad assumption of $V_{thn0} = |V_{thp0}| = V_{th}$.

2.4.2. V_{LH} Voltage

When the input is high (V_{DD}), V_{out} is low (0 V). As a result, M4 is ON shorting drain and gate of M6 that keeps M6 at the edge of SAT and OFF regions. Thus, when the input is high (V_{DD}), transistors M1,

M5, M4, and M6 are ON and the other transistors are OFF. At OP2, the V_{LH} voltage can be determined by equating the SAT currents of M1 and M2. Here, V_p could be considered as finite and less than V_{DD}, where M6 is on the edge of the SAT and OFF regions.

$$V_{LH} = \frac{\alpha_1 \cdot \left(V_p - \left|V_{thp0}\right|\right) + V_{thn0}}{(1+\alpha_1)} \tag{45}$$

V_p could be found by using the equivalent circuit as shown in Figure 7c. Here, it is assumed that the V_{out} node voltage is approximately equal to 0 V, and M4 shorts V_{cn} to V_p effectively connecting the gate of M6 to its drain, which keeps it in SAT region. Thus, using SAT currents of transistors M2 and M6, we can determine the V_p voltage as follows:

$$V_p = \frac{V_{in} + \alpha_3 \cdot V_{DD} + (1-\alpha_3)\left|V_{thp0}\right|}{(1+\alpha_3)} \tag{46}$$

where

$$\alpha_3 = \sqrt{\frac{\beta_6}{\beta_2}} \tag{47}$$

Using (46) in (45) for $V_{in} = V_{LH}$, we can derive the V_{LH} as follows:

$$V_{LH} = \frac{(1+\alpha_3) \cdot V_{thn0} + \alpha_1 \cdot \alpha_3 \cdot \left(V_{DD} - 2 \cdot \left|V_{thp0}\right|\right)}{1 + \alpha_3 \cdot (1+\alpha_1)} \tag{48}$$

Al-Sarawi derived the V_{LH} equation (Equation (4) in [8]) rather differently, which assumes $V_{LH} = V_{DD} - V_{HL}$ as well as $V_{thn0} = |V_{thp0}| = V_{th}$. This assumption results in a simple but inaccurate V_{LH} design equation. Additionally, his V_{LH} equation has a typographical error that causes gross calculation error larger than 200% of simulated values. The corrected equation that gives reasonable hand calculation error (<20% of simulated values) is given below. We used this corrected equation instead of Equation (4) in [8] to compare our new equation.

$$V_{LH} = V_{DD} \times \frac{(R+1)}{R_p(R+1)+1} - V_{th} \times \frac{R_p(2R-1)-1}{R_p(R+1)+1} \tag{49}$$

where

$$R = 1/\alpha_1, \text{ and } R_p = \alpha_3 \tag{50}$$

2.4.3. Hysteresis Voltages

Formulation provided by Al-Sarawi (Equations (2)–(4) in [8]) assumes that the threshold voltages of the NMOS and PMOS devices are the same and do not cover all design and process variations. Thus, the equations given in (44) and (48) are more detailed and useful for hand calculations and design for the hysteresis voltage ($\Delta V_H = V_{HL} - V_{LH}$).

3. Comparison of Simulation and Hand Calculations

Simulations of all ST circuits were performed using a well established, analog/mixed-signal, 0.35 µm CMOS, 3.3 V, CMOS process with BSIM3v3 Spice models. The process has device characteristics listed in Table 1. This process allows a fair comparison with literature that used long channel MOSFET models and high supply voltages. We used a minimum channel length (L_{min}) of 0.35 µm and changed widths of transistors to cover a wide range of design spaces. In addition, Monte-Carlo, corner/parameter, or both, sweep simulations were run to find hysteresis voltages (V_{LH} and V_{HL}) under various conditions.

Here, we only reported 3.3 V supply results at room temperature (T = 300 K), while similar trends were observed for other supply voltages.

Table 1. 0.35 µm CMOS process parameters for hand calculations.

Parameter	NMOS	PMOS
Transconductance (KP) (µA/V^2)	170	58
Threshold Voltage (V_{th0}) (V)	0.50	−0.65

3.1. Dokic ST Circuits

For the simulations of Dokic's circuits, transistor widths were changed between 2 L_{min} and 20 L_{min} with 2 L_{min} steps such that channel widths of transistors M1, M2, and M4 were set equal to each other and M3 varied separately for P-type and N-type ST circuits. For CMOS type ST, widths of M1, M2, M6 and widths of M3, M4, M5 were set equal, respectively. Since minimum channel length was used for all transistors, setting α_{1n}, α_{1p}, α_1, and α_3 to 1.0 for all ST types, while α_{2n} and α_{2p} were varied between 0.383 and 3.83 for N-type and P-type circuits. For CMOS ST, α_2 was changed between 0.54 and 5.4. The bulk of all NMOS transistors were connected to ground and the bulk of all PMOS transistors were connected to V_{DD}.

3.1.1. N-Type ST by Dokic

Figure 8 shows the simulation results for N-type Dokic ST. Hysteresis voltage (ΔV_H) as large as 1 V could be achieved for α_{2n} = 3.83. Moreover, smaller hysteresis voltages close to 0.1 V are also possible with N-type Dokic ST. Although they are not the same, Equations (15) and (17) result in the same V_{HL} and V_{LH} hand calculation values as the original Dokic equations (Equations (5) and (6) in [5]). Hand calculation accuracy compared to the simulation results are shown in Figure 9. Hand calculations result in lower than −13 and +5% errors for V_{HL} and V_{LH}, respectively. Wide hysteresis voltage can be achieved by choosing $(W/L)_{1,2,4}$ = 20 (α_{1n} = 1.0), and $(W/L)_3$ = 2 (α_{2n} = 3.83).

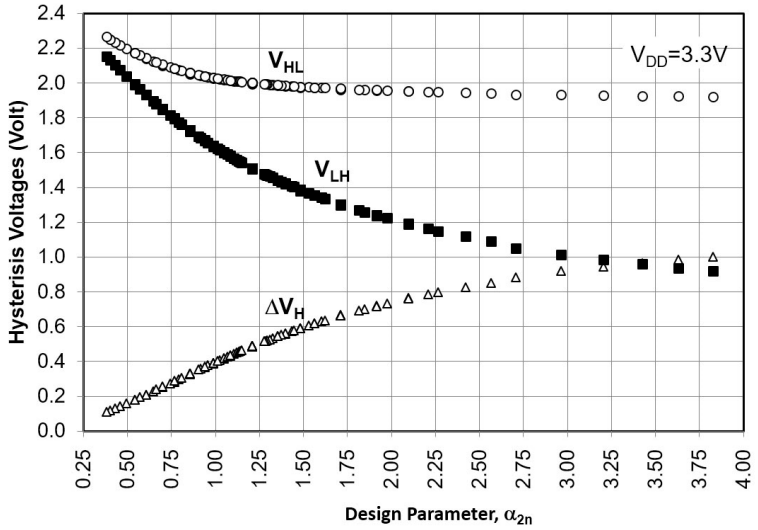


Figure 8. Simulated hysteresis voltages (V_{HL}, V_{LH}, ΔV_H) of N-type Dokic ST for different device sizes (0.383 < α_{2n} < 3.83) and V_{DD} = 3.3 V.

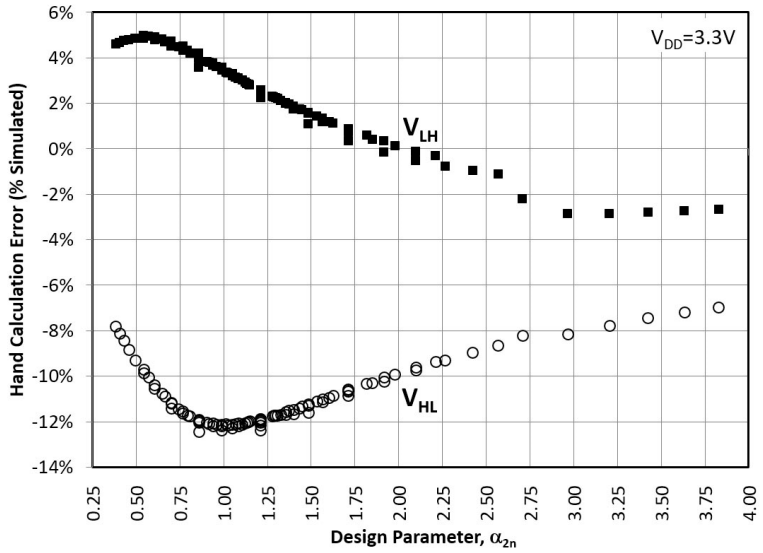


Figure 9. Hand calculation errors of hysteresis voltages using (15) and (17) for N-Type ST (or with Equations (5) and (6) in [5]) for V_{DD} = 3.3 V and different device sizes (0.383 < α_{2n} < 3.83).

3.1.2. P-Type ST by Dokic

For P-type Dokic ST, the channel length of M3 is set to 4 L_{min} and the bulk of M4 is connected to the node V_1 while the dimensions of other transistors and bulk connections are kept the same as N-type Dokic ST. Figure 10 shows the simulation results of P-type Dokic ST for 3.3 V supply voltage. Hysteresis voltage (ΔV_H) as large as 0.9 V could be achieved for α_{2p} = 0.383. Moreover, hysteresis voltages close to 0.1 V are also possible with P-type Dokic ST for larger α_{2p} values. The simulation results for the hysteresis voltages for different device sizes and supply voltages show that, typically, the V_{HL} voltage is widely controlled by the design parameters. Figure 11 shows the hand calculation errors of the hysteresis voltages for the design parameter α_{2p} using Equations (19) and (20) (or with Equations (8) and (12) in [5]). The error could be less than ±13%.

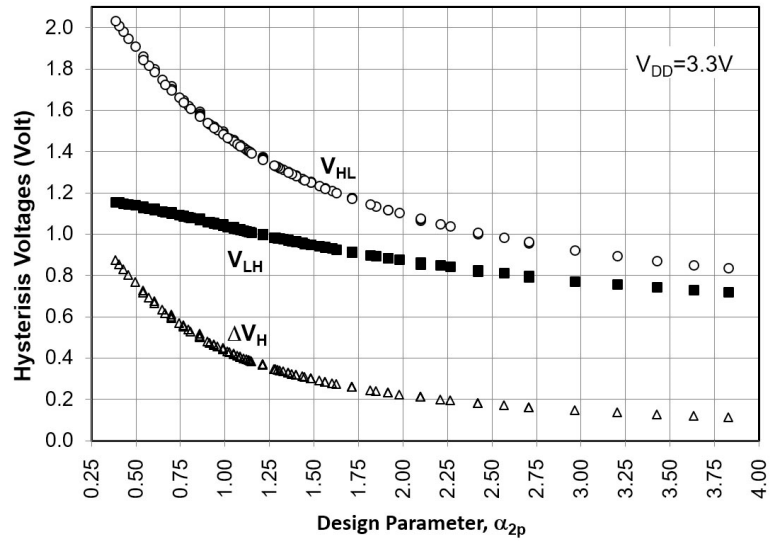


Figure 10. Simulated hysteresis voltages (V_{HL}, V_{LH}, ΔV_H) of P-type Dokic ST for different device sizes (0.383 < α_{2p} < 3.83) and V_{DD} = 3.3 V.

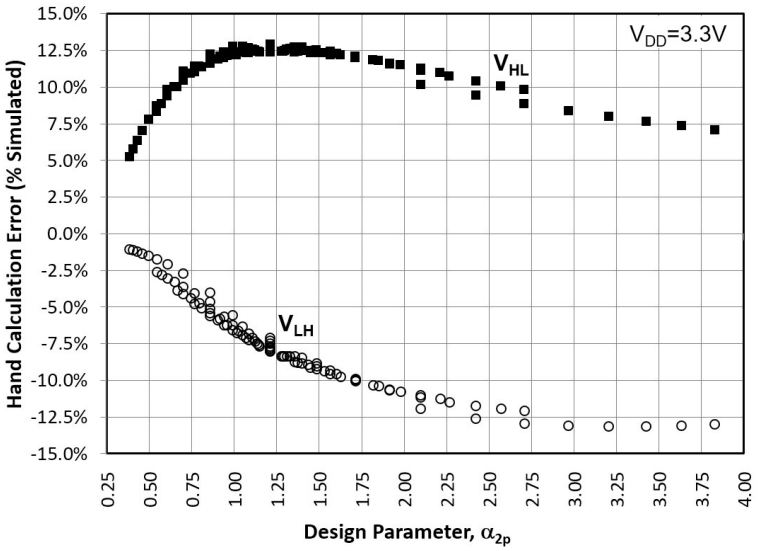


Figure 11. Hand calculation errors of hysteresis voltages using (19) and (20) for P-Type ST (or with Equations (8) and (12) in [5]) for different device sizes ($0.383 < \alpha_{2p} < 3.83$) and $V_{DD} = 3.3$ V.

3.1.3. CMOS-Type ST by Dokic

For CMOS-type Dokic ST circuit simulations, the bulk of M6 is connected to the node V_1. Figure 12 shows the simulation results for the 3.3 V supply voltage. Hysteresis voltage (ΔV_H) as large as 1.2 V could be achieved for $\alpha_2 = 0.54$. The simulation results show that a smaller hysteresis voltage is not possible. Additionally, hand calculation equations (Equations (23) and (25)) and original Dokic equations (Equations (14) and (15) in [5]) do not provide good approximations that result in up to ±50% error for V_{HL} and between +10% and −25% error for V_{LH}, as shown in Figure 13.

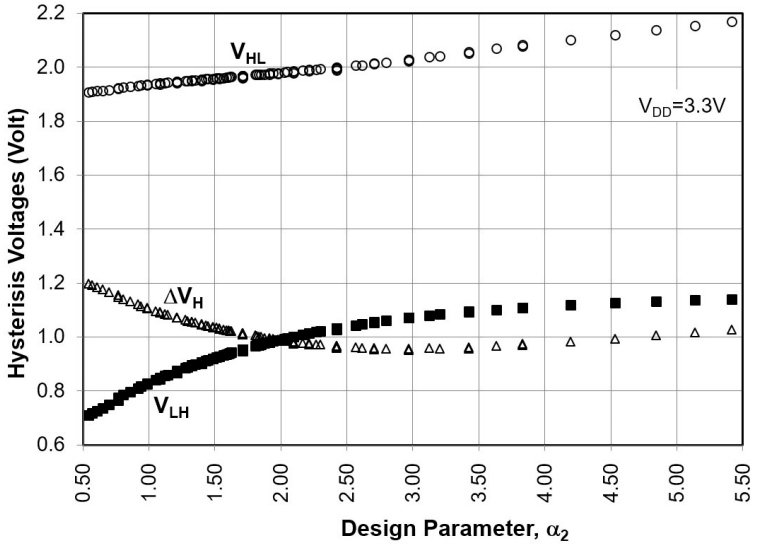


Figure 12. Simulated hysteresis voltages (V_{HL}, V_{LH}, ΔV_H) of CMOS-type Dokic ST for different device sizes ($0.54 < \alpha_2 < 5.4$) at $V_{DD} = 3.3$ V.

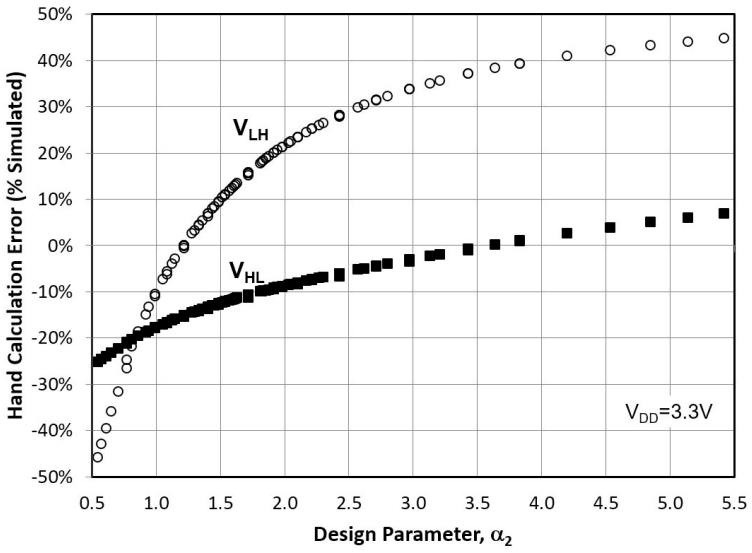
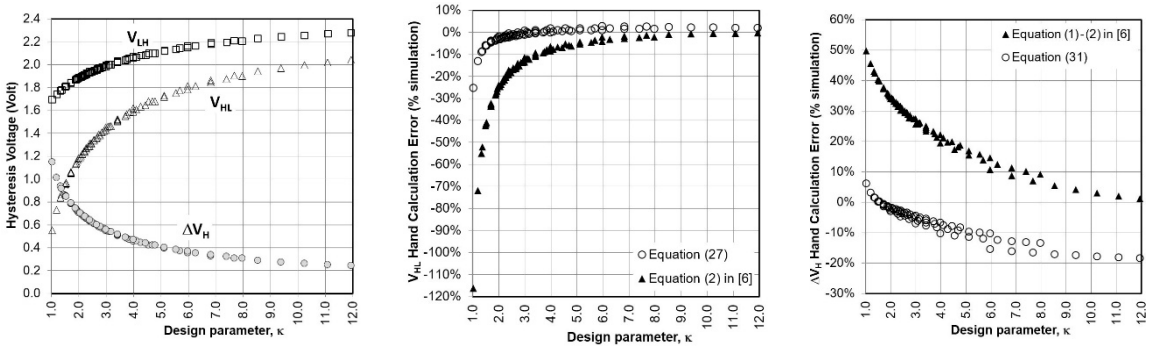


Figure 13. Hand calculation errors of hysteresis voltages using (23) and (25) for CMOS-type ST (or with Equations (14) and (15) in [5]) for different device sizes ($0.54 < \alpha_2 < 5.4$) at V_{DD} = 3.3 V.

3.2. CMOS-Type ST by Steyaert

Transistor widths were changed between 2 L_{min} and 10 L_{min} with L_{min} steps for transistors M1, M3, and M5, and between 7 L_{min} and 14 L_{min} with 4 L_{min} steps for transistors M2 and M4 during the simulation. The channel lengths of NMOS and PMOS transistors were set to 10 L_{min} and L_{min}, respectively. As a result, a wide design space was covered for simulations and calculations. A new design parameter, the transconductance factor ratio (κ) which is defined as the ratio between β_2 (M2) and β_1 + β_5 (M1 and M5 combination) represents the design space. κ was set between 1.0 and 12. This results in the V_{HL} voltage being between 0.55 and 2.04 V, the V_{LH} between 1.7 and 2.30 V, and the hysteresis voltage between 0.24 and 1.15 V for 3.3 V supply voltage, as shown in Figure 14a.



(**a**) (**b**) (**c**)

Figure 14. (**a**) Simulated hysteresis voltages of Steyaert ST, (**b**) hand calculation accuracy of V_{HL} using Equation (30) and Equation (1) in [6], and (**c**) hand calculation error of ΔV_H using Equation (34) and Equations (1) and (2) in [6].

Derived V_{LH} equation in this work, Equation (28), and the original Steyaert equation ((1) in [6]) are the same, resulting in a maximum −4% hand calculation error. Steyaert's V_{HL} equation ((2) in [6]), on the other hand, results in gross hand calculation errors up to −120% for smaller κ values, while Equation (30) presented in this work results in less than −25% as shown in Figure 14b. As a result, overall hand calculation error for the hysteresis voltage ΔV_H by Equation (34) is lower than that of the original Steyaert equation, (Equations (1) and (2) in [6]), as shown in Figure 14c.

3.3. Non-Inverting ST by Pedroni

The hysteresis voltages of Pedroni ST can be set by modifying the sizes of NMOS (M1, M3, M5) or PMOS (M2, M4, M6) transistors. For simulation, NMOS transistor widths were changed between 2 L_{min} and 10 L_{min} with 2 L_{min} steps. The multiplication factor (M) of M1 is set to M_x and M3 and M5 is to unity, respectively. Similar widths and steps used for the PMOS transistors while setting the multiplication factor of M4 to be Mx, and keeping the multiplication factor of M2 and M6 to be unity. The channel length of NMOS and PMOS transistors were set to L_{min} or 0.35 µm. Multiplication factor of transistor M1, M4, the M_x, varied from 2 to 6 while other Ms were kept constant at unity so that a wide range of V_{HL} and V_{LH} voltages were achieved.

Design parameter M_x, α_1, and α_2 can be used for setting hysteresis voltages (V_{HL}, V_{LH}, and ΔV_H) as shown in Figure 15. Hysteresis voltage as large as 1 V can be achieved by increasing all design parameters, however, this will result in a large silicon footprint. Equations (35) and (37) predict the hysteresis voltages, V_{HL}, and V_{LH} with +14% to −8% calculation errors as shown in Figure 16.

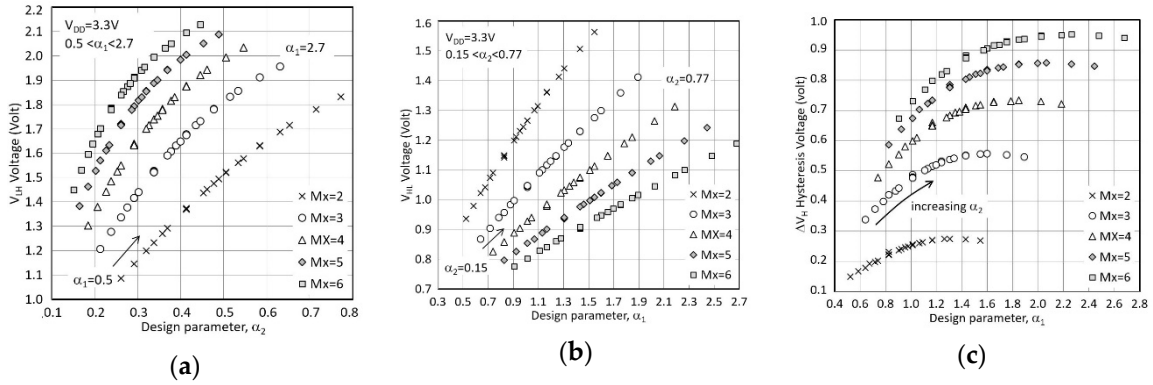


Figure 15. Simulated hysteresis voltages of Pedroni ST for different device sizes α_1, α_2, and Mx at V_{DD} = 3.3 V (**a**) V_{LH} vs. α_2, (**b**) V_{HL} vs. α_1, and (**c**) ΔV_H vs. α_1.

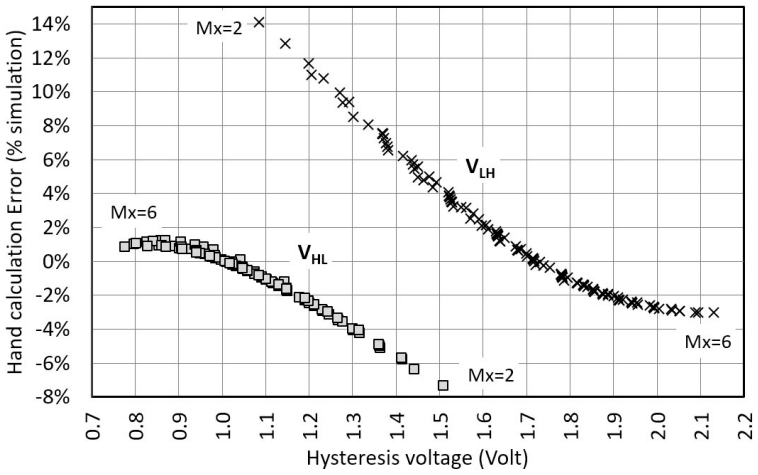
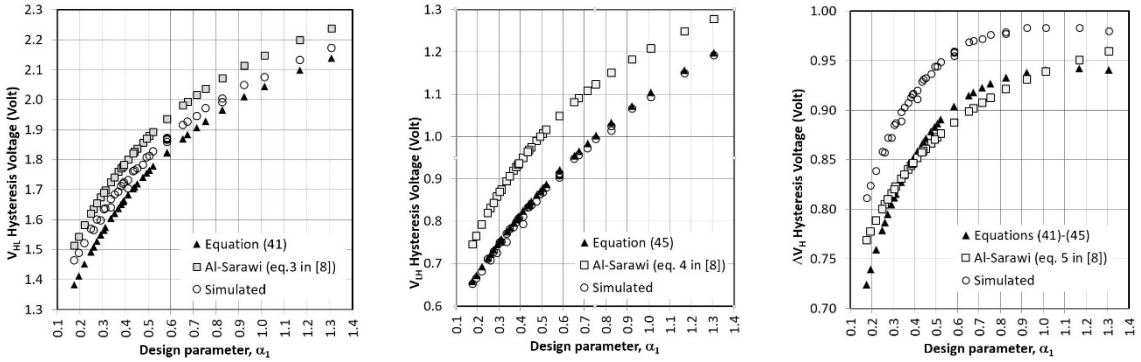


Figure 16. Hand calculation accuracy of hysteresis voltages V_{HL} and V_{LH} using Equations (35) and (37).

3.4. CMOS-Type ST by Al-Sarawi

The sensitivity of the V_{HL} to α_1 parameter, which can be derived from Equation (44), is much higher than the α_2 and α_3 parameters. Thus, for simulation and evaluation of the design equation accuracies, α_1 parameter varied from 0.15 to 1.3 while α_2 and α_3 were set to 1.41 and 2, respectively. We proposed new hysteresis design equations for the Al-Sarawi ST. Figure 17 shows the simulated and calculated values by using Al-Sarawi's original design equation and the proposed design Equation (44)

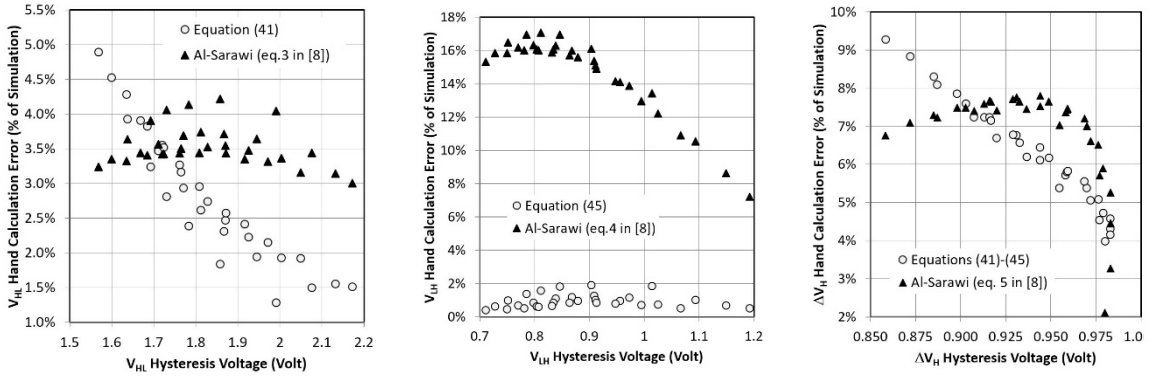
of the hysteresis voltages V_{HL}, V_{LH}, and ΔV_H versus α_1 parameter. The simulation results show that the ΔV_H reaches 0.98 V (Figure 17c), which is larger than Al-Sarawi's original design equation. However, it saturates around these values even if α_1 parameter is increased.



(**a**) (**b**) (**c**)

Figure 17. Comparison of design equations and simulated hysteresis voltages of Al-Sarawi's ST for 3.3 V supply voltage (**a**) V_{HL} vs. α_1, (**b**) V_{LH} vs. α_1, and (**c**) ΔV_H vs. α_1.

Figure 18 illustrates the hand calculation errors of proposed design equations in Section 2.4 as well as Al-Sarawi's original design equations related to the simulated values of V_{HL}, V_{LH}, and ΔV_H. It can be noticed from Figure 18b that V_{LH} hand calculation error of the proposed design Equation (48) is less than 2% while it could be as large as 17% for Al-Sarawi's original design equation. Additionally, hand calculation errors of V_{HL} and ΔV_H by the proposed design equations are always inversely proportional to V_{HL} and ΔV_H, respectively, and are lower than the calculation errors of Al-Sarawi's original design equations.



(**a**) (**b**) (**c**)

Figure 18. Comparison of hand calculation errors of hysteresis voltages of Al-Sarawi's ST for 3.3 V supply voltage. (**a**) error vs. V_{HL}, (**b**) error vs. V_{LH}, and (**c**) error vs. ΔV_H.

3.5. Comparison of All Circuits

Table 2 summarizes a comparison between Dokic [5], Steyaert [6], Pedroni [7], and Al-Sarawi [8] ST circuits in terms of total area, simulated power consumption, transition delays, and maximum hysteresis voltage based on the variation of device dimensions. There are tradeoffs among these parameters that the larger ΔV_H design may have the higher-power consumption or the larger footprint or the lower speed. By design, it is desirable to have larger ΔV_H, and smaller delay, area, and power

consumption. Thus, we propose a figure of merit (*FoM*) based on these parameters. *FoM* for ST circuits can be calculated using the following equation:

$$FoM = \frac{10000 \times \Delta V_H(V)}{Area(\mu m^2) \times Power\ consumtion(\mu W) \times Delays(ns)} \quad (51)$$

Table 2. Performance comparison of the six ST circuits.

ST Circuit	T_{rise} (ns)	T_{fall} (ns)	Area(μm)	Power (μW)	ΔV_H (V)	FoM
Dokic (N) [5]	1.636	0.109	7.60	58.51	1.110	1.43
Dokic (P) [5]	0.412	1.507	6.86	61.58	0.855	1.05
Dokic (CMOS) [5]	1.239	0.372	7.80	75.31	1.015	1.07
Steyaert [6]	1.308	3.043	38.20	186.48	1.150	0.04
Pedroni [7]	0.425	0.338	13.70	63.20	0.952	1.44
Al-Sarawi [8]	1.320	1.185	5.40	43.23	0.983	1.68

This equation is scaled by a multiplying factor of 10,000 for better number representation. Delay was measured at 50% of the supply voltage level when a 100 fF loading is added at the output of each ST design. The sum of rising (t_{rise}) and falling times (t_{fall}) was calculated as the delay.

From Table 2, if the large hysteresis voltage is the main requirement, the Steyaert ST circuit is the best, yet it has the lowest *FoM* due to large power consumption and area. Overall, Al-Sarawi's ST circuit offers the best *FoM*. However, it is slower than Pedroni's ST, which is the second-best choice among the investigated topologies.

4. Conclusions

In this paper, detailed reviews of Dokic [5], Steyaert [6], Pedroni [7], and Al-Sarawi [8] SISO ST circuits are presented. The paper starts with the detailed derivation of the hysteresis voltages (V_{HL}, V_{LH}, and ΔV_H) for each topology. Then, we propose some new design equations which result in a more intuitive, and accurate design through hand calculations. Simulations were run to verify that the derived and the original design equations are accurate. The simulations were carried out in a well-established 0.35 μm/3.3 V analog/mixed-signal CMOS process. For each ST circuit, hysteresis voltages (V_{HL}, V_{LH}, and ΔV_H) were calculated with respect to different device sizes, which cover wide design space at a process supply voltage of 3.3 V. The hand calculation results derived from both the original and the new design equations were presented for each ST circuit and are compared with simulation results. The comparisons show that the new design equations are better than the original ones in terms of accuracy and intuition. Finally, the proposed *FoM* in Equation (51) can work as a criterion to compare different ST circuits. It is found that Al-Sarawi's ST circuit offers the best *FoM* of the investigated topologies.

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