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Review

Advances in La-Based High-k Dielectrics for MOS Applications

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Abstract: This paper reviews the studies on La-based high-k dielectrics for metal-oxide-semiconductor (MOS) applications in recent years. According to the analyses of the physical and chemical characteristics of La_2O_3, its hygroscopicity and defects (oxygen vacancies, oxygen interstitials, interface states, and grain boundary states) are the main problems for high-performance devices. Reports show that post-deposition treatments (high temperature, laser), nitrogen incorporation and doping by other high-k material are capable of solving these problems. On the other hand, doping La into other high-k oxides can effectively passivate their oxygen vacancies and improve the threshold voltages of relevant MOS devices, thus improving the device performance. Investigations on MOS devices including non-volatile memory, MOS field-effect transistor, thin-film transistor, and novel devices (FinFET and nanowire-based transistor) suggest that La-based high-k dielectrics have high potential to fulfill the high-performance requirements in future MOS applications.

Keywords: lanthanum oxide; high-k dielectric; metal-oxide-semiconductor

1. Introduction

As the complementary metal-oxide-semiconductor (CMOS) technology is continually approaching the giga-scale in terms of integration level, the MOS devices have to be scaled to the nano-scale. According to the roadmap on the development of the semiconductor industry, the key geometric parameters for several technology nodes calculated by the technology rules are listed in Table 1 [1]. However, the minimum thickness of SiO_2 as a gate dielectric is ~0.7 nm because at least two layers of neighboring oxygen atoms are needed to prevent the gate/SiO_2 and SiO_2/Si interfaces from overlapping with each other [2]. However, practically, for SiO_2 dielectrics thinner than 3 nm, the gate leakage is too large for applications because direct tunneling of charge carriers occurs [3,4]. Figure 1a is an example of gate leakage increasing significantly with the decrease of dielectric thickness [5], where for a 1.5 nm oxide film, the unacceptable gate leakage exceeds 100 A/cm^2 at 2 V. Figure 1b shows the factors that contribute to the gate leakage current of MOS devices, including Fowler-Nordheim tunneling [6], Poole-Frenkel tunneling [7,8], trap-assisted tunneling [9,10], and direct tunneling [11]. Among them, direct tunneling has the closest relation with the thickness of the gate dielectric, and its current can be calculated as:

$$J_{DT} = J_0\left(1 - \frac{V_{ox}}{\Phi_B}\right)\exp\left\{-\frac{3}{4}\frac{\sqrt{2m^*q}}{h}\frac{T_{ox}{\Phi_B}^{3/2}}{V_{ox}}\left[1 - \left(1 - \frac{V_{ox}}{\Phi_B}\right)^{3/2}\right]\right\}, \quad (1)$$

where J_0 is a constant, V_{ox} is the voltage drop of the dielectric, Φ_B is the barrier height, m^* is the electron effective mass in the dielectric, $\hbar$ is the reduced Planck's constant, and T_{ox} is the dielectric thickness. Obviously, the direct tunneling current increases exponentially with the decrease of T_{ox}. Therefore, the replacement of SiO_2 by an alternative material with higher dielectric constant (k) allows the use of larger physical thickness for the same oxide capacitance, and so the tunneling current can be suppressed.

Table 1. Key geometric parameters for several technology nodes [1].

Gate Length (nm)	22	16	11	8
Dielectric thickness (nm)	0.8	0.6	0.4	0.3
Junction depth (nm)	11.0	8.0	5.5	4.0
Channel depletion thickness (nm)	11.0	8.0	5.5	4.0

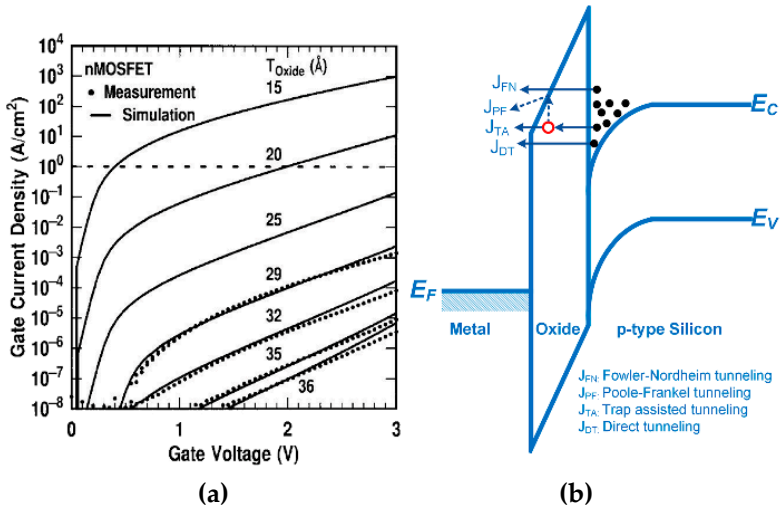

Figure 1. (**a**) Gate leakage current for nMOSFETs with different gate dielectric thicknesses [5], and (**b**) energy band diagram of an nMOS structure showing major tunneling mechanisms.

The first high-k material studied is silicon oxynitrde (SiO_xN_y). By annealing in NH_3 or other gases containing nitrogen (N), effective N incorporation is achieved in SiO_2 to improve its thermal and high-field reliability [12]. Besides, reports show that N doping is capable of reducing oxide charges and border traps [13]. However, SiO_xN_y could no longer meet the requirement of gate leakage during scaling down in the ITRS report in 2007, and so novel high-k materials as gate dielectrics had to be explored. According to Figure 2, that demonstrates the dielectric constants of promising candidates for MOS devices together with their band gaps and conduction-band offsets (CBO) with Si and GaAs [14,15], inverse trends in the variations of E_g and CBO with the k value can be found. Therefore, in order to reach a balance in this trade-off, apart from possessing a high k value, sufficiently large E_g (usually > 5 eV) and CBO with the substrate (usually > 1 eV) to minimize carrier injection should also be required. Besides, thermal stability is an additional criterion for choosing proper high-k dielectrics: large Gibbs free energy to inhibit the reaction with the Si substrate and small oxygen diffusion coefficient to suppress the formation of low-k SiO_x interfacial layer during high-temperature processing steps are essential [16,17].

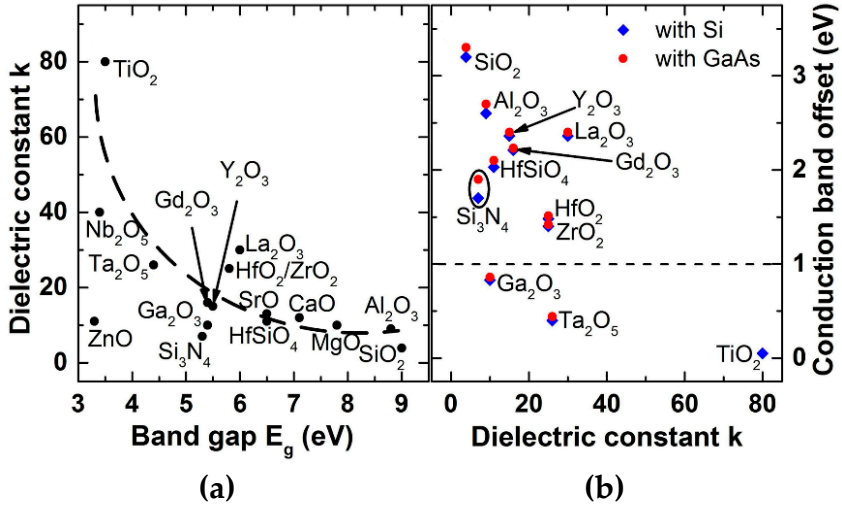

Figure 2. Dielectric constant vs. (**a**) band gap and (**b**) conduction band offsets with Si and GaAs for promising materials as gate dielectrics [14,15].

Through comprehensive consideration of the pertinent requirements for high-k gate dielectrics, following SiO_xN_y, hafnium (Hf)-based materials attracted much attention and were successfully introduced into production in 2007, with the TEM images of a PMOS transistor and its MOS gate stack shown in Figure 3 [18]. However, owing to lower thermal stability and lower interface quality with Si than SiO_2, HfO_2 is still far from being ideal. Therefore, measures including post-deposition annealing (PDA) and nitrogen incorporating and doping of Si, Al, La, etc. to form ternary oxides have been tried with good results achieved [19]. In the past decade, much efforts have been made to study novel high-k dielectrics in a variety of semiconductor devices, and hundreds of reports have shown the high potential of high-k gate dielectrics for application in the CMOS and VLSI technologies. For example, Al_2O_3, ZrO_2, Ta_2O_5, and Al-doped TiO_2 have been proved to be promising candidates for DRAM. Hf- and Zr-based ternary oxides have been widely used in MOSFET, FinFET, etc. [20]. Recently, flexible and stretchable electronics has become a hotspot for applications such as flexible displays, wearable sensors and electronic skins. Therefore, massive studies have been made on thin-film transistors (TFTs) with flexible/stretchable substrates. At the beginning, Al_2O_3 was proved to be an excellent gate dielectric for TFT [21]. However, its low k value limits its further applications. So, research interests moved to composite/stack layers involving materials with higher k values such as Ga_2O_3, Hf-/Zr-based ternary oxides/oxynitrides, rare-earth oxides, and perovskites [22]. Speaking of perovskites, their super-high k value (300~6000) makes them stand out in high-k dielectrics, among which $SrTiO_3$ and $BaTiO_3$ are the most representative dielectric perovskite oxides. However, the phase of perovskite is critical because most perovskite oxides are insulators in the cubic phase while variation in crystallinity induces metallic, superconducting, ferroelectric, and ferromagnetic properties [23]. Therefore, the deposition of perovskite oxides as dielectrics in MOS applications is the main issue. Then, the idea of using perovskite nanocrystals or nanocomposites has been proposed. Firstly, self-assembled $BaTiO_3$ and (Ba, Sr)TiO_3 nanocrystals have been tried on pentacene TFT with a mobility of 0.35 $cm^2 \cdot V^{-1} \cdot s^{-1}$ [24]. Synthesized $BaTiO_3$ has also been studied with a k value of 4000 achieved [25]. Moreover, a study on $BaTiO_3$/polypropylene nanocomposites showed a rubber shell of nano-scaled $BaTiO_3$ could promote the compatibility and dispersion of nano-particles in polypropylene matrix and also improve the dielectric and tensile properties of nanocomposites [26]. However, the uncertainty in the phase of perovskite oxide is still limiting the performance of relevant MOS devices.

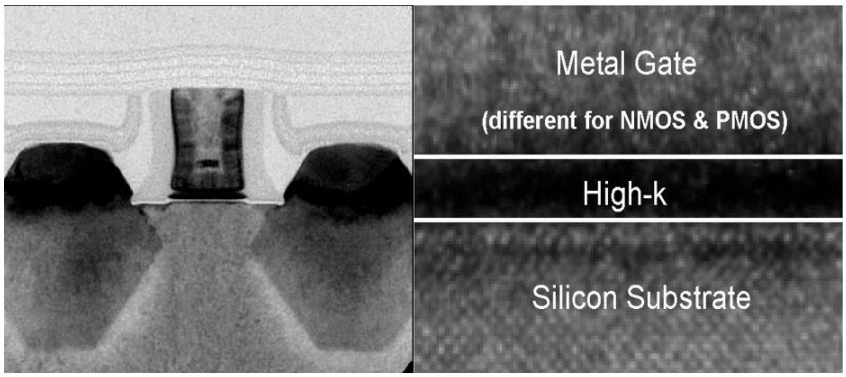

Figure 3. TEM images: (**a**) pMOS transistor and (**b**) MOS gate stack with Hf-based high-k gate dielectric [18].

Then, rare-earth oxide as a high-k dielectric has been studied, and La_2O_3 is a representative that has attracted much attention in recent years due to its high k value (~27) [27], large band gap (5.8~6.0 eV) [28], high breakdown field (> 13 MV/cm) [29], low leakage current for small effective oxide thickness (EOT) [30], good thermodynamic stability, and good high-field reliability on Si [30,31]. Based on the WKB approximation, the direct tunneling currents of ideal MOS structures with different dielectrics were modeled and simulated by H. Wu, et al., with results demonstrated in Figure 4 [32]. Significant gate leakage decrease is achieved by replacing SiO_2 with high-k materials, among which La_2O_3 has the lowest leakage current. Besides, unlike perovskites, high-quality La_2O_3 film can be easily deposited by sputtering, ALD, PVD, E-beam, etc. These make La-based high-k materials highly promising for MOS applications.

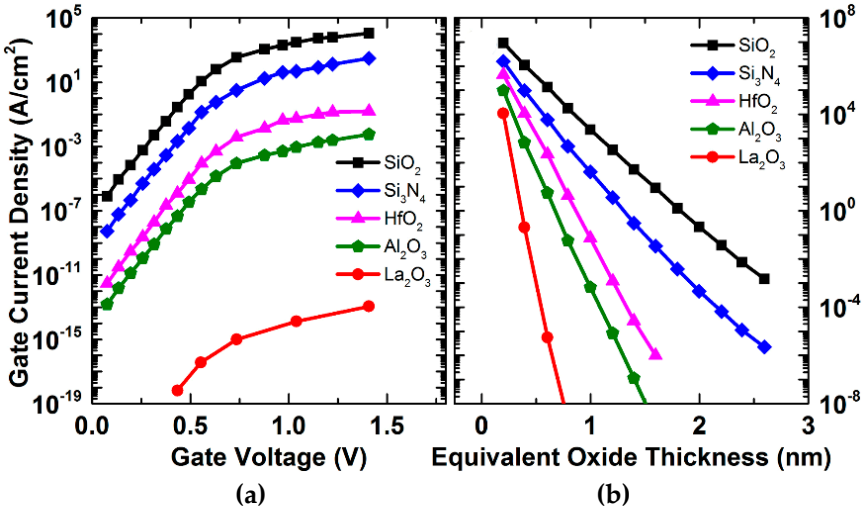

Figure 4. Gate leakage vs. (**a**) gate voltage and (**b**) equivalent oxide thickness for ideal MOS devices with different gate dielectrics [32].

However, besides the crystallization temperature (~500 °C) of La_2O_3 [19] not being high enough for high-temperature processing during fabrication, its hygroscopicity and defects [31,33] are the main concerns for MOS applications. Therefore, similar to HfO_2, treatments including nitrogen incorporation and metal doping are necessary for La_2O_3 to improve its oxide quality. So, based on the advantages of La_2O_3 over other high-k materials and with the motivation of providing guidelines for making good use of La-based high-k materials to improve the performance of MOS devices for meeting the requirements of the technology nodes in the future, this review focuses on the advances of La-based high-k dielectrics in MOS applications. To have a better understanding of the characteristics

of the La-based films; the basic theories for the main concerns of La_2O_3 as gate dielectric and the proposed solutions to these problems are discussed in Section 2, including the hygroscopicity of La_2O_3, the defects in La_2O_3, and the mechanisms for the effects of La in La-based ternary oxides. Then, the advances of the MOS applications with La-based high-k dielectrics are reviewed in Section 3 to provide a whole picture on the developments and advantages of La-based high-k dielectrics in MOS devices. The applications in Section 3 include non-volatile memory, MOSFET, TFT, Ge and III-V compound semiconductor devices, and novel MOS devices (e.g. FinFETs and nanowire FETs) because these are the main devices that need high-k dielectrics for high-performance MOS applications in the future. At last, a brief conclusion is made in Section 4 based on the discussions in Sections 2 and 3, and future studies are proposed to give directions to the developments of MOS devices with La-based high-k dielectrics.

2. Characteristics of La-Based High-k Dielectrics

2.1. Hygroscopicity of La_2O_3

As mentioned above, theoretically, the k value of La_2O_3 is ~27, but lower k values, even below 10, were found in early studies [34–36]. One important reason is the hygroscopic nature of La_2O_3, whose high ionicity leads to a direct reaction with H_2O:

$$La_2O_3 \rightarrow 2La^{3+} + 3O^{2-}, \quad (2)$$

$$H_2O + O^{2-} \rightarrow 2OH^{-}, \quad (3)$$

Experimental results [37] showed that after exposure to air for 12 h, the root-mean-squared (RMS) surface roughness of La_2O_3 increased from 0.5 to 2.4 nm (Figure 5a), which was probably caused by the non-uniform moisture absorption of the La_2O_3 film that led to a non-uniform volume expansion. Apart from the surface roughness, increases in physical thickness and thus capacitor equivalent thickness (CET) occurred as shown in Figure 5b which should be ascribed to the lower density of hexagonal $La(OH)_3$ (4.445 g/cm^3) than that of hexagonal La_2O_3 (6.565 g/cm^3). The obvious increase of CET resulted in a significant degradation in k value from 20 to 7 (Figure 5b). Besides, this moisture absorption further affected the electrical properties of MOS devices. Figure 5c demonstrates that the flat-band voltage (V_{fb}) shift and hysteresis of an MOS capacitor with La_2O_3 gate dielectric increase with exposure time, implying that negative charges and traps are induced near/at the La_2O_3/Si interface [38].

A lot of effort has been made to enhance the hygroscopic resistance of La_2O_3 so that its advantages as a gate dielectric can be made use of. The most widely used method is incorporating a second metal element to form a ternary oxide. The rate of the reaction between a metal oxide (M_xO_y) and moisture (H_2O) can be evaluated by the Gibbs free energy change (ΔG) [39]. A negative ΔG means the system energy decreases after the reaction, implying that the reaction has a high possibility to occur, and so a more positive ΔG is more promising for the corresponding high-k material to suppress the hygroscopicity of La_2O_3 [37,40]. For example, in Ref. [37], Y incorporation exhibited obvious improvement in the moisture resistance of La_2O_3, as shown in the inset of Figure 6, where for Y concentration higher than 40%, the degradation in k value after exposure in air is negligible. Apart from the materials in Figure 6, Ta and Nb have also been proved to be promising dopants to improve the hygroscopic resistance of La_2O_3 by surface morphology and XPS analysis, which showed that the La–OH peak significantly decreased with increasing Ta and Nb contents in TaLaO [41] and NbLaO [42], respectively.

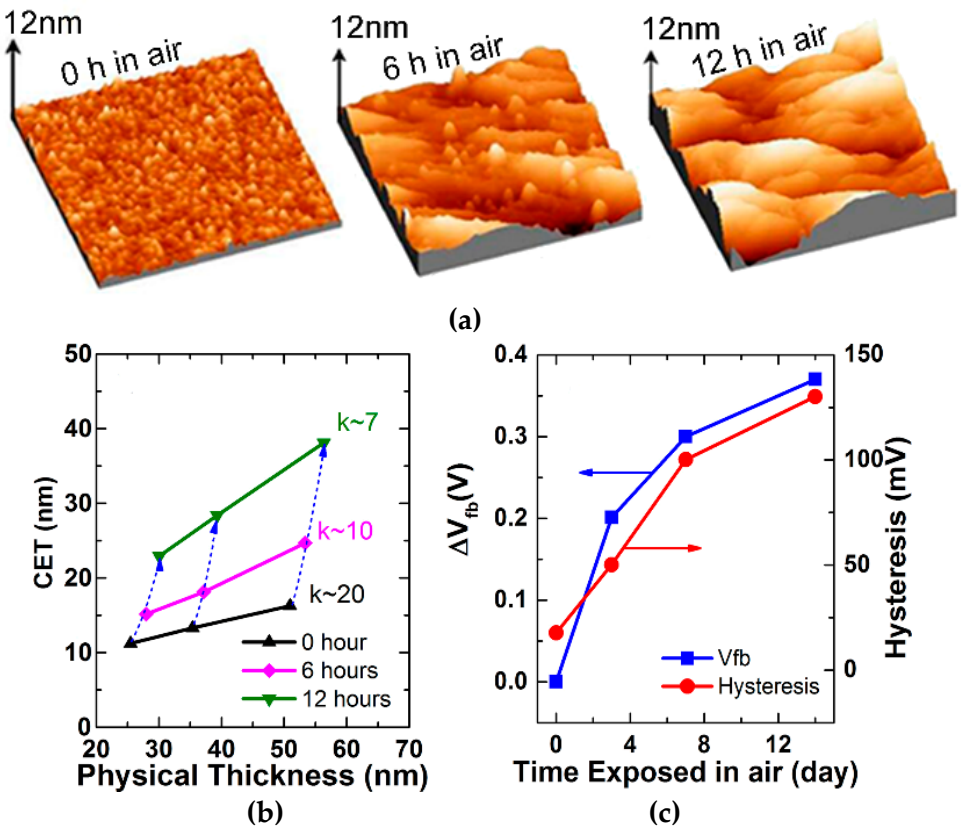

Figure 5. Impact of the hygroscopicity of La_2O_3 on (**a**) surface roughness, (**b**) film thickness and k value, and (**c**) V_{fb} and hysteresis of an MOS device [37].

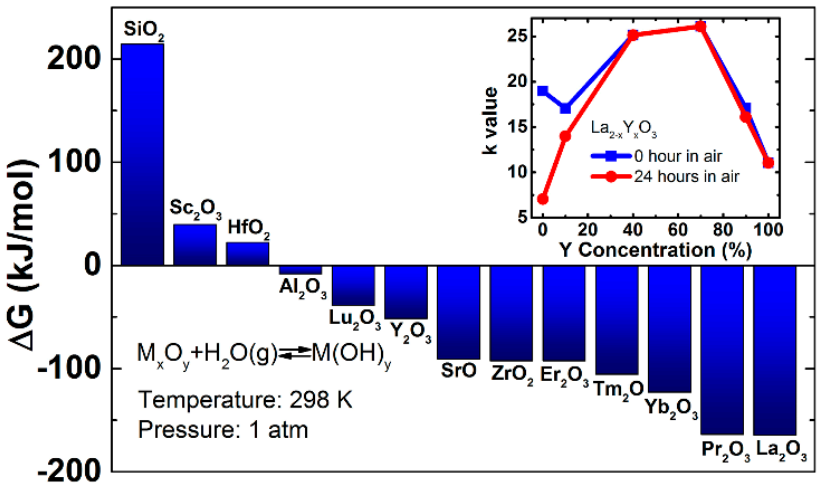

Figure 6. Gibbs free energy change of moisture reaction in high-k oxides under standard conditions [39].

Another method is post-deposition ultraviolet (UV) ozone treatment using an Hg vapor UV lamp that primarily emits light with wavelengths of 185 and 254 nm [43]. The UV ozone treatment is compared with thermal N_2 and O_2 treatments in Figure 7. Obviously, the O_2 + N_2 annealing can inhibit the moisture absorption of La_2O_3 by a large extent, but the N_2 annealing together with the UV ozone treatment keeps the La_2O_3 surface roughness almost unchanged after exposing to air for 24 h.

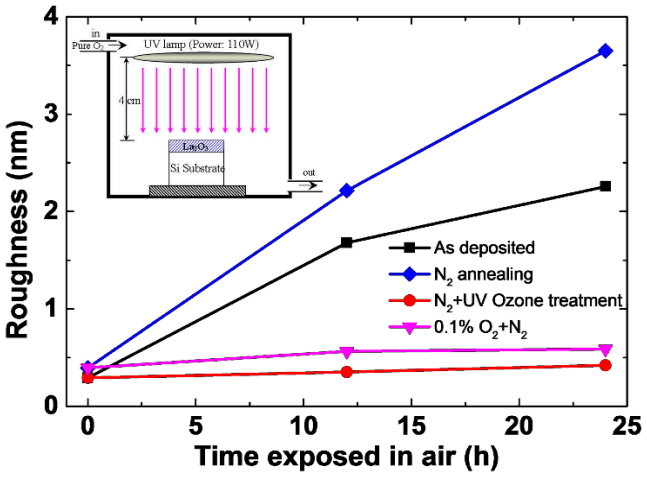

Figure 7. Roughness of La_2O_3 with different post-deposition treatments vs. exposure time in air [43].

2.2. Defects in La_2O_3

Although high-k dielectrics can keep the trend of device scaling, their higher density of bulk defects and poorer interface with Si than SiO_2 results in degradation in carrier mobility, thus making the device performance unsatisfactory [44–46]. As shown in Figure 8a, fixed charge, oxide trap, interface trap, interfacial dipole, and surface roughness are the factors that lead to Coulomb, phonon and surface-roughness scatterings (in Figure 8b), which govern the effective carrier mobility of MOS devices at low, moderate and high gate fields respectively. The origins of these scatterings are: Firstly, the defects in high-k oxide bulk cause charge trapping and lead to higher bias instability and unreliability [47]; secondly, optical phonons in high-k oxides have a low-lying soft polar mode which results in the remote scattering of channel carriers [48]. Besides, the larger surface roughnesses of high-k dielectrics with both the Si substrate and the gate than those of SiO_2 should be ascribed to the interaction between high-k elements with the Si substrate and the longer metal–O and metal-Si bonds than the Si–Si bond.

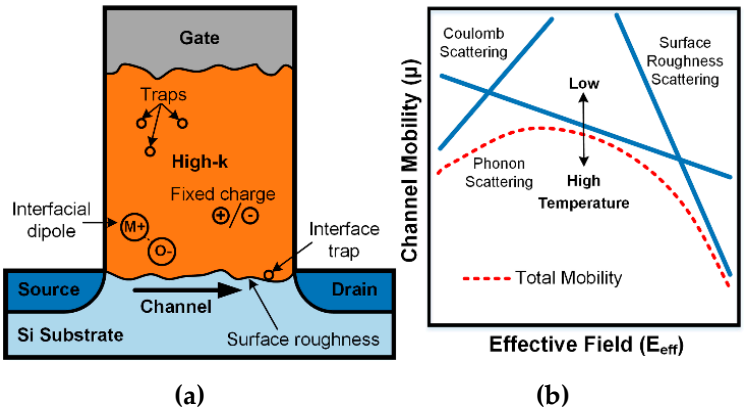

Figure 8. (**a**) Schematic diagram demonstrating the origins of mobility degradation in MOSFET. (**b**) Factors that impact carrier mobility.

Since the reliability issues of gate dielectric film (including mobility degradation, threshold-voltage shift, and biased temperature instability) are mainly governed by the neutral and charged defects located in the dielectric film and at the dielectric/substrate interface, it is necessary to explore the characteristics of these defects. Oxygen-related defects are the dominant point defects in binary high-k oxides, mainly including oxygen vacancy and oxygen interstitial. Unlike HfO_2 with only four-fold O sites, hexagonal La_2O_3 has two different types of oxygen vacancies (V_O), with four-fold and six-fold coordination, respectively. The energy levels of V_O in La_2O_3 are demonstrated in Figure 9a [49],

obtained by the first-principle calculations based on the total energy plane wave pseudopotential code CASTEP [50], with the band structure of La_2O_3 with neutral V_O shown in Figure 9b as an example [51]. Four-fold V_O has all five charged states including 2−, 1−, 0, 1+, and 2+. However, since high coordination prevents distortion from creating an extra gap state, the six-fold V_O only consists of 0, 1+, and 2+ states. Obviously in Figure 9a, all the V_O states in La_2O_3 are located above the band gap of Si, which differs from the case of HfO_2. The neutral V_O state in HfO_2 is below the conduction band of Si [52], and so can be filled by the electrons injected from the silicon substrate, leading to a positive shift in the capacitance-voltage (C–V) curve [53]. J. X. Zheng, et al. calculated the concentrations of V_O and oxygen interstitial (O_i) in La_2O_3 based on the density functional theory in the generalized gradient approximation using the projector augmented wave method, with results shown in Figure 9c [54]. For HfO_2, the concentrations of positively-charged oxygen vacancy and negatively-charged oxygen interstitial are too low (<10^{12} cm^{-3}) to significantly affect the device performance. However, for La_2O_3, the concentrations of V_O^{2+} and O_i^{2-} are higher than 10^{16} cm^{-3}, and so, apart from neutral V_O, charged V_O and O_i can also be the sources of charge trapping.

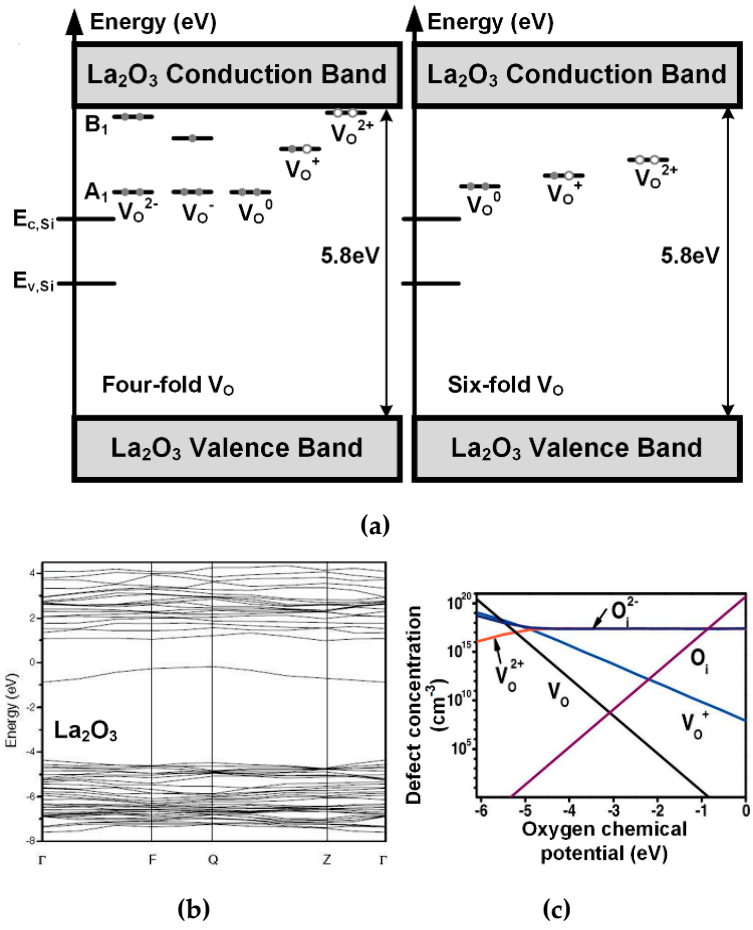

Figure 9. (**a**) Energy levels of four-fold and six-fold oxygen vacancies in La_2O_3 [49], (**b**) band structure of La_2O_3 with neutral oxygen vacancies [51], and (**c**) defect concentration in La_2O_3 at 1300 K [54].

Trap at the La_2O_3/semiconductor interface is another concern that impacts the device performance. La has been reported to easily react with semiconductor substrates such as Si and Ge to form a low-k interfacial layer (IL). As illustrated in Figure 10a, the thickness of the IL can be comparable to the thickness of the La_2O_3 bulk, which significantly decreases the effective k value of the dielectric and thus increases the EOT [55,56]. As shown in Figure 10d, post-deposition annealing can enhance this reaction because an obvious increase in the La-silicate peak can be found for higher annealing temperature [57]. However, a tradeoff exists between the k value and the interface-trap density (D_{it}), according to

Ref. [56]. As the thickness of the IL (with a k value of 5.8) increases from 0.7 to 3.0 nm, D_{it} decreases by almost two orders but the effective k value of the dielectric is reduced by ~70%. With a La-silicate IL, the interface states are depicted in Figure 10b [58]. It is known that La_2O_3 has an ionic bonding nature while the bond in the La-silicate layer is more covalent, thus creating a larger amount of oxygen vacancies at the La_2O_3/Si interface [59]. It has been reported that charge-pumping measurement can be used to detect the interface traps between ionic HfO_2 and covalent SiO_2, and so the traps located at the La_2O_3/La-silicate interface can be considered as slow states [60]. Figure 10c shows the density of this slow state (D_{slow}) together with D_{it} calculated based on the measured conductance of the La_2O_3-gated MOS capacitor, with D_{slow} much higher than D_{it} and almost distributed uniformly in the Si band gap [58].

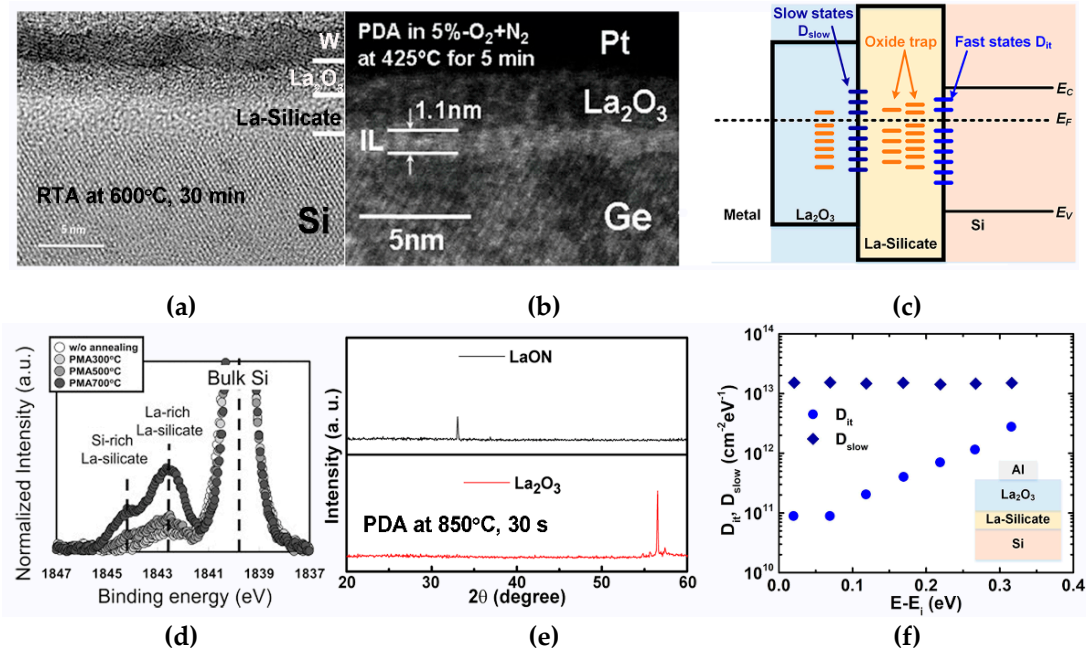

Figure 10. (**a**,**b**) TEM images of Si and Ge MOS structures with La_2O_3 as a gate dielectric [55,56], (**c**) band diagram showing the traps in a metal/La_2O_3/La-silicate/Si gate stack [58], (**d**) calculated D_{it} and D_{slow} in the band gap of Si with E_i as the midgap of the Si substrate [60], (**e**) Si 1s spectrum at the La_2O_3/Si interface for different annealing temperatures [57], and (**f**) XRD patterns of La_2O_3 and LaON films after annealing [61].

Besides, the grain-boundary state created by the crystallization of high-k material during high-temperature treatments is another kind of defect that induces shallow traps. Figure 10e shows the XRD patterns of La_2O_3 and LaON after annealing, and the weaker peak of LaON than that of La_2O_3 indicates that nitrogen incorporation can suppress the crystallization of La_2O_3 [61]. Apart from increasing the crystallization temperature, N incorporation is also capable of increasing the k value and reducing the border traps in the dielectric [62]. For many years, in order to decrease the defect density of the La_2O_3 gate dielectric, many efforts have been made, including high-temperature annealing, N incorporation, F or NH_3 treatment, doping other high-k metal elements to form complex oxides (e.g. LaYO [37], LaTaO [41]), and addition of an interfacial passivation layer (e.g., Al_2O_3 [27]). However, because of the trade-off between the k value and the dielectric/semiconductor interface quality, there is still ample room to improve the device performance

2.3. Effects of La on La-doped Ternary Oxides

As mentioned in the previous section, doping other high-k metal elements into La_2O_3 is capable of enhancing the device performance. It has been reported that doping La into other high-k materials

can also achieve improvements, and the most important effect of La doping is to passivate the oxygen vacancies in other high-k binary oxides. After several reports showing that La incorporated in HfO_2 could significantly improve the device performance [53–66], X. P. Wang et al. proposed that this improvement should be ascribed to the reduction of oxygen vacancies (V_O) in HfLaO [66]. Therefore, several studies on the physics of this phenomenon have been made and confirmed the V_O passivation role of La as discussed below.

The relaxed structures of V_O in HfO_2 and HfLaO were obtained by first-principle calculation based on the density-functional theory using a generalized gradient approximation (Figure 11a) [67], according to which the formation energies of V_O near La and far from La were calculated to be 6.29 and 5.73 eV respectively, both larger than the V_O formation energy of HfO_2 (5.58 eV), indicating that it is more difficult to form V_O's after La incorporation. The reason for this increased V_O formation energy by La incorporation can be explained by Figure 11b, with the contour plots for the wave functions corresponding to the V_O-related states. Although electrons are trapped in V_O in both HfO_2 and HfLaO cases, the electron distribution around V_O of HfO_2 differs from that of HfLaO. Since the La–O bond is 76% ionic and higher than Hf–O (70%) according to the Pauling's electronegativity theory, electrons from the O2p states are localized at the O sites beside the La atoms, thus reducing the interaction between La5d and O2p when compared to that between Hf5d and O2p. Therefore in Figure 11b, unlike in HfO_2, the oxygen atom nearest to La atoms does not contribute to the gap state at all [67]. Moreover, D. Liu et al analyzed the band structures of HfO_2 and HfLaO with V_O's and concluded that La was capable of passivating V_O's in HfO_2 and ZrO_2 by shifting the vacancy gap into the conduction band, thus suppressing the Fermi-level pinning at the dielectric/Si interface as shown in Figure 11c [68]. In the case of pure HfO_2, oxygen tends to diffuse to the Si substrate and leaves a positive V_O by releasing two electrons that fall down to the Fermi level of the metal gate. However, if a thin La_2O_3 layer lies on the HfO_2 dielectric, La can easily diffuse into HfO_2 under high-temperature annealing [69] and then the substitution of Hf by La creates holes in the valence band (VB). Therefore, in this case, the oxidation of Si drives this substitution without releasing electrons, and the VB holes are filled by the electrons in the conduction band to prevent the formation of V_O states in the band gap.

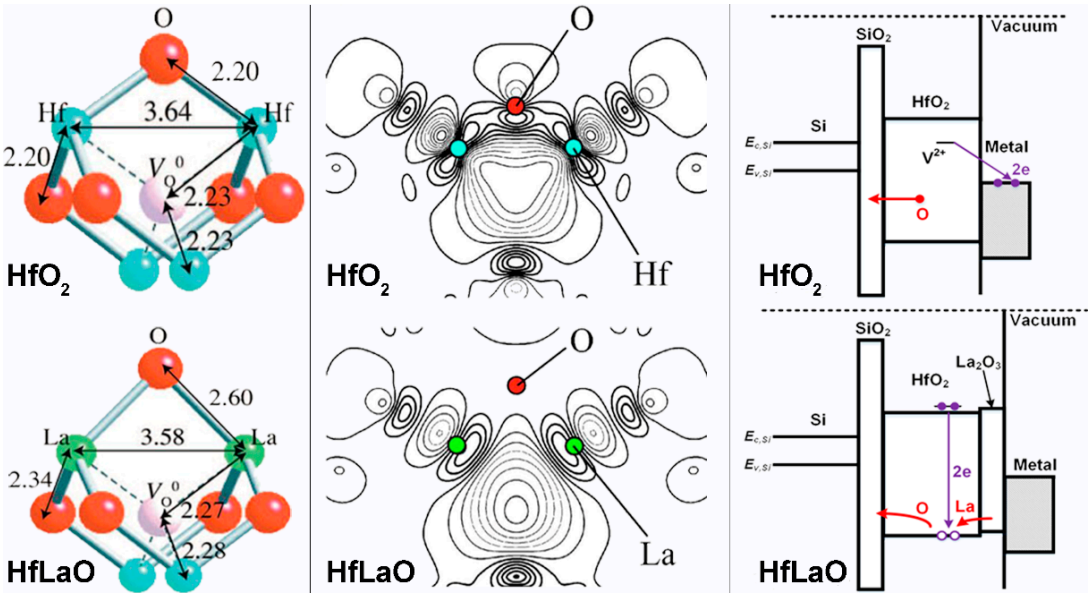

Figure 11. For HfO_2 and HfLaO: (**a**) relaxed structure of oxygen vacancies V_O [60], (**b**) contour plot of wave function corresponding to the V_O-related gap states [60], and (**c**) schematic band diagram showing oxygen vacancies [68].

Apart from oxygen-vacancy passivation, La incorporation has also been reported to be able to modify the flatband voltage (V_{FB}) of the gate stack in nFETs [69,70] and so shift their threshold voltages (V_{th}). An obvious negative shift of V_{FB} for HfLaO-gated MOS capacitor with increasing La concentration can be found in Figure 12a, and the effective work function (EWF) decreases by about 0.5 eV for the La content rising from 20% to 60% [71]. Recently, the EWF shift due to La incorporation into HfO_2 has been found to be linearly dependent on the La concentration, with −53 meV per 10^{14} atoms/cm^2 [72]. This should be ascribed to the formation of a dipole layer at the HfLaO/SiO_2 interface as shown in the inset of Figure 12b and the V_{FB} shift can be calculated by:

$$\Delta V_{FB} = -\left(\frac{Qd_1}{k_{SiO_2}} + \frac{Qx}{k_{HfLaO}}\right) + \frac{Q(x-d_2)}{k_{HfLaO}} = -Q\left(\frac{d_1}{k_{SiO_2}} + \frac{d_2}{k_{HfLaO}}\right) \quad (4)$$

where Q is the areal charge density in the dipole layer, d_1 and d_2 are the widths of dipole layers on the SiO_2 and HfLaO sides, k_{SiO_2} and k_{HfLaO} are the k values of SiO_2 and HfLaO, and x is the thickness of the HfLaO layer. Since an offset can be caused by the dipole layer inside the dielectric film and is independent of the dipole position, the V_{FB} shift almost remains constant as the CET varies (Figure 12a).

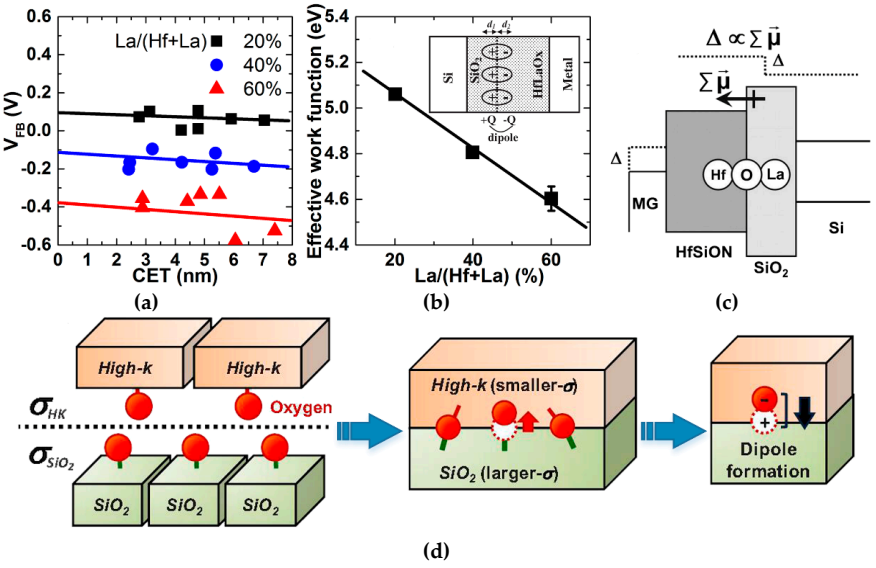

Figure 12. (**a**) V_{FB} and (**b**) effective work function of Au/$HfLaO_x$/SiO_2/p-Si capacitors with different La concentrations in the dielectric [71,72], (**c**) interface dipole moment model [73], and (**d**) schematic diagram for the formation of the interface dipole [74].

An interface dipole moment model has been proposed by P. D. Kirsch et al. through a study of V_{th} shift for nFETs with rare-earth element (La, Sr, Er, and Sc)-doped HfO_2 [73]. Similarly, the dipole vector formed by incorporating rare-earth oxides could induce a shift in EWF, resulting in the V_{th} tuning of MOS devices. According to the experimental results, V_{th} approximately varied proportionally and inversely proportionally with the electronegativity and ionic radius of the dopant respectively. This is consistent with the conclusion drawn by L. Lin et al. that it is the dopant electronegativity that influenced the magnitude of the interfacial dipole moment and thus ΔV_{FB} [74]. Moreover, the physical origin for the formation of the dipole layer has been ascribed to the difference in areal density of oxygen atoms (σ) between the oxides [75]. The formation process of the dipole layer is shown in Figure 12d, in which σ_{HK} and σ_{SiO_2} are the areal densities of oxygen atoms in high-k oxide and SiO_2 respectively. For the case that σ_{HK} is smaller than σ_{SiO_2}, in order to relax the structure, an oxygen atom tends to move towards the high-k side, thus resulting in the formation of a dipole consisting of a negatively-charged center in the high-k oxide and a positively-charged oxygen vacancy nearby.

3. Applications of La-based High-k Gate Dielectrics

3.1. Nonvolatile Memory

As the nonvolatile memory evolves from ROM (read-only memory) to flash memory, new materials, new structures and new operating principles have been continually explored in order to break the limitation that the electrons stored in the floating gate significantly decrease during the scaling down of floating-gate flash memory [76]. The new structures of flash memory include ferro-electric random-access memory (FeRAM), nanoelectromechanical memory (NEMM), magneto-resistive random-access memory (MRAM), phase-change memory (PCM), and charge-trapping memory (CTM). Although CTM introduced in 1967 is the oldest, its high storage density, simple fabrication and compatibility with the CMOS technology make it a promising candidate for the next-generation flash memory technology [77]. Nowadays, the structure of CTM is based on a metal gate/oxide blocking layer (BL)/nitride charge trapping layer (CTL)/oxide tunneling layer (TL) gate stack on nm Si substrate as shown in Figure 13a. P-type Si is more often used than n-type Si because the electrons in the n-type channel formed at the surface of a p-type substrate have higher mobility than the holes in the p-type channel formed at the surface of an n-type substrate. Whether the CTL stores electrons or not is the way to define '1' and '0' respectively. The TL is formed by an insulating material, which allows electron tunneling from the substrate to the CTL under a positive gate bias and prevents electrons from escaping from the CTL to the substrate under no gate bias. The BL is also formed by an insulating material, which can prevent the electron transfer between the CTL and the gate electrode. Positive or negative voltage is applied to the gate electrode for programming or erasing operation, during which the electric field inside the gate stack enables electrons to flow into or out of the CTL via the TL. In order to further scale down the device, high-k materials such as the BL, CTL and TL have been widely studied, among which La-based high-k materials have been reported to achieve good results as discussed below.

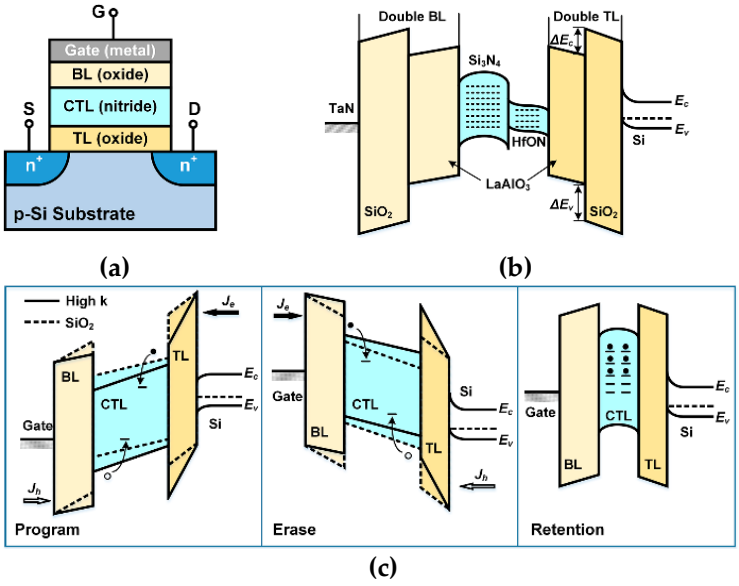

Figure 13. (**a**) Cross-sectional schematic of a MONOS CTM transistor; (**b**) energy band diagrams of CTM in program, erase and retention states; and (**c**) energy band of CTM with SiO_2/$LaAlO_3$ double TL [78].

Firstly, when considering replacing SiO_2 by high-k material as the BL, apart from the k value, requirements including (i) large band gap and band offset with respect to the CTL, (ii) low density of traps at the interface or in the dielectric bulk, (iii) thermal and kinetic stability, and (iv) compatibility with the CMOS technology, should be fulfilled. According to Figure 13b, with an ideal high-k BL,

the electric field across the tunneling layer can be enhanced, thus improving the program/erase (P/E) speed [78]. Owing to a large band gap (8.8 eV) and good stability, Al_2O_3 has become the best choice for BL, but its low k value (~9) limits the device scaling. Therefore, La-doped Al_2O_3 ($LaAlO_x$) has been studied for higher k value, and results showed that not only the program speed and V_{th} window increased, but the retention performance also improved [79]. The $LaAlO_x$ layer was deposited by ALD using $La(iPrCp)_3$, $Al(CH_3)_3$ and H_2O precursors and the atomic ratio of La/(La + Al) was 55%. Compared with Al_2O_3, $LaAlO_x$ as BL brought 40% and 32% improvements in program speed and V_{th} saturation window, better robustness to voltage stress, and better retention performance below 120 °C. Besides, HfLaO has also been applied as BL and exhibited improvements in V_{th} saturation window and robustness to voltage stress due to its higher k value (~22) compared to Al_2O_3. However, the retention performance degraded after La incorporation, probably due to decreased conduction-band offset [79,80].

Secondly, for the TL, a tradeoff exists between high P/E speed and good retention property, and so based on the investigation of the band-engineered barrier, the idea of multi-TL consisting of low-k and high-k dielectrics has been proposed. In Figure 13c, the $LaAlO_3/SiO_2$ double TL permits faster P/E because the ΔE_c and ΔE_v at the $LaAlO_3/SiO_2$ interface can give easier electron and hole tunnelings. Moreover, the added $LaAlO_3$ layer increases EOT, and so improves retention [81]. These were confirmed by experimental results: With the addition of the $LaAlO_3$ layer, the memory window measured at ± 16 V for 100 μs increased from 3.3 to 5.6 V, and at 150 °C, an initial ΔV_{th} of 5.6 V and a 10-year window of 3.8 V were achieved for the same P/E voltage and P/E time.

Moreover, La-based high-k materials have been widely investigated as the CTL due to the high k value and deep-level traps of La_2O_3 [53]. However, since the density of deep-level traps in La_2O_3 is not high enough, the memory window of the CTM with La_2O_3 as CTL was only 0.5 V at ± 16 V for 1 s [82]. The main methods to solve this problem are: (i) nitrogen incorporation, which has been reported to induce traps in the bandgap and also remove shallow traps along the grain boundaries in CTLs [83]; (ii) doping other high-k material (e.g. Nb_2O_5, TiO_2), which is another way to increase the deep-level trap density in La_2O_3 and suppress its reaction with the SiO_2 TL as well [84]; (iii) multi-CTL for band engineering, which is capable of enhancing charge-trapping efficiency [85] and improving device reliability by suppressing the impact of TL degradation [86]. Experimentally, these methods have all been studied, and the results in Figure 14 [61,84,87–90] show obvious improvements in the performance of the memory device. HfLaO nanocrystal can provide the largest memory window, but the 50% degradation after 10 years in the retention property is not good for real applications. Comprehensively speaking, NbLaON is the most promising candidate so far due to its relatively large memory window, good P/E transient characteristics and negligible degradation after 10 years.

3.2. Metal-oxide-semiconductor Field-effect Transistors (MOSFETs)

Having been the basic device of ICs, MOSFET's with high-k dielectrics have attracted a lot of efforts for more than 20 years. For the gate dielectric, the most important thing is to keep the carrier flow in the channel when biases are applied to the device. So, a sufficiently-large band gap and conduction-band (CB) offset with the channel material are necessary to prevent the current flow from the substrate to the gate. Moreover, the qualities of the dielectric film and the dielectric/substrate interface are also critical because as discussed in Section 2.2 (Figure 8), fixed charges, oxide traps, interface traps, interfacial dipoles, and surface roughness are the factors that lead to carrier scatterings and thus decreased carrier mobility. Therefore, it is important to explore different high-k materials and different post-deposition treatments in order to improve the device performance. Although HfO_2 has already been commercially dominant, La_2O_3 still holds its potential for future generations due to its larger CB offset with the Si substrate than its HfO_2 counterpart. As mentioned in Section 2.2, a La-silicate interfacial layer (IL) tends to be formed after high-temperature annealing, which is good for the interface quality but increases the EOT. K. Kakushima et al. have studied the properties of MOSFET with La_2O_3 as a gate dielectric, in which the La_2O_3 film was deposited by electron beam

evaporation at 300 °C on a p-Si (100) wafer [91]. After a 500 °C rapid thermal annealing (RTA) in forming gas (N_2:H_2 = 97:3), a 1.57 nm silicate IL was formed in the 3-nm dielectric, leading to an EOT increase from 0.48 to 1.15 nm. However, the mobility peak increased from 60 to 300 cm^2/Vs at room temperature and the subthreshold swing (SS) decreased from 120 to 66 mV/dec, which are impressive numbers for MOSFET.

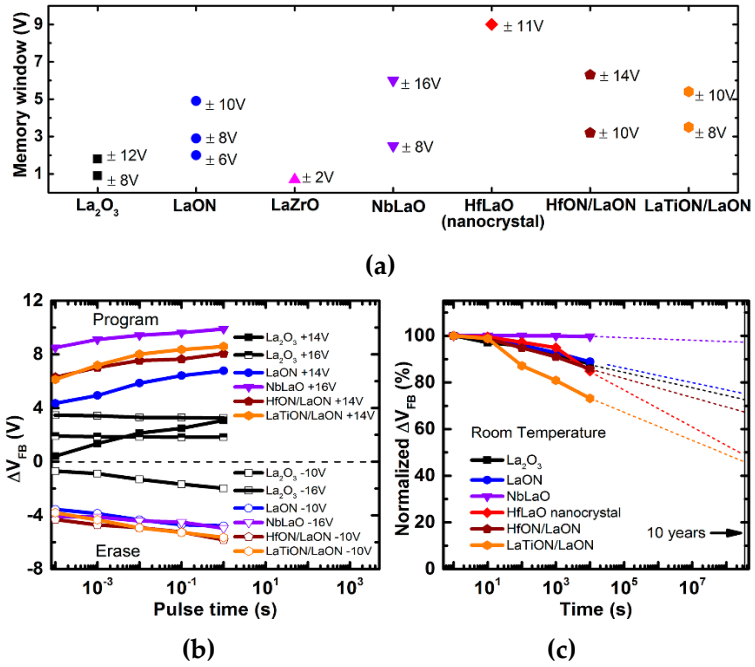

Figure 14. CTM with La-based high-k CTL: (**a**) memory window, (**b**) P/E transient characteristics, and (**c**) retention property [61,84,87–90].

Owing to the hygroscopicity of La_2O_3 as mentioned in Section 2.1, it is La-based complex oxides that are preferred because of the inevitable exposure to the air or low-vacuum environment. In 2003, $LaAlO_3$ was chosen as the gate oxide for future technology nodes in the semiconductor roadmap [92]. As a perovskite, $LaAlO_3$ has a relatively large band gap (5.6 eV), large CB offset (1.8 eV), small lattice mismatch to Si (1.3%), and small oxygen diffusion coefficient, which are all desirable for epitaxial gate dielectric on Si [93–95]. Si MOSFET with $LaAlO_3$ gate dielectric has been reported by I. Y. Chang, et al., where a 7.3-nm $LaAlO_3$ film was deposited on p-Si by RF sputtering and a post-deposition annealing was performed at 700 °C for 30 s in N_2 [96]. Results showed that the maximum effective mobility (μ_{eff}) at 300 K was 212.6 cm^2/Vs; SS was 69.4 mV/dec; and hysteresis was 8.6 mV. According to the analysis on the mechanisms that caused mobility degradation, the Coulomb scattering was roughly the same for $LaAlO_3$ and SiO_2-gated MOSFETs, indicating that $LaAlO_3$ is indeed a promising candidate. N incorporation into $LaAlO_3$ has been proved to improve the device properties, including EOT, gate leakage, SS, and drive current [97]. Moreover, HfLaO, LaTiO, LaZrO, LaYO, etc. have all been tried as the gate dielectric for MOSFETs, and the device properties are listed in Table 2 [91,96,98–102]. The carrier mobility of the La_2O_3/LaSiO sample could reach 300 cm^2/Vs, but its EOT was not small enough for further scaling down due to the low k value of SiO_2. The LaTiO sample was a good choice because of its high mobility (300 cm^2/Vs), small EOT (0.63 nm) and low V_{th} (0.12 V). However, both the deposition method and post-deposition treatment are different for the dielectrics in Table 2, thus making a fair comparison among the samples difficult. However, all these results demonstrate the high potential of La-based high-k oxides as the gate dielectric of MOSFET.

Table 2. Characteristics of MOSFETs with La-based high-k gate dielectrics (PVD = Physical Vapor Deposition).

Dielectric	Deposition	Annealing	EOT (nm)	$\mu_{eff,\ max}$ (cm^2/Vs)	$\lvert V_{th} \rvert$ (V)	SS (mV/dec)
La_2O_3/LaSiO [92]	E-Beam	500 °C, 30 min	1.15	300	0.4	66
$LaAlO_3$ [97]	Sputtering	700 °C, 30 s	1.73	213	~0.05	69
HfLaO [99]	Sputtering	900 °C, 30 s	1.3	225	~0.05	–
HfLaSiO [100]	PVD	850 °C, 1 min	1.2	160	–	–
LaYO [101]	E-Beam	600 °C, 5 min	1.7	181	0.59	95
LaZrO [102]	ALD	500 °C, 5 min	1.27	–	0.43	71
LaTiO [103]	PVD	600 °C	0.63	300	0.12	–

$LaLuO_3$ with high k value (~30) and low leakage current has also attracted much attention and has been investigated in SOI-MOSFETs [103,104]. E. D. Ozhen, et al. first deposited it on an SOI (100) wafer by molecular beam deposition at 450 °C with a thickness of 6 nm, and a PDA was performed at 400 °C in oxygen and forming gas (H_2:N_2 = 1:9) sequentially for 10 min each [103]. According to the experimental results, the V_{th} and SS of the SOI nFET and pFET were 0.22 V and −0.8 V, 72 mV/dec and 65 mV/dec, respectively. The $LaLuO_3$ film exhibited an EOT of 1.55 nm, low D_{it} of 4.5×10^{11} cm^{-2}·eV^{-1}, and the electron and hole mobilities on the SOI are similar to those of devices based on HfO_2 and HfSiON gate dielectrics with a similar EOT. However, the interface and bulk traps of the dielectric might cause a high level of 1/f noise, which could not meet the stricter requirements of the RF and analogue mixed-signal CMOS technologies. Therefore, M. Olyaei, et al. analyzed the low-frequency noise of the SOI-MOSFET with $LaLuO_3$ gate dielectric[98]. The normalized drain-current noise ($S_{ID}/I_D{}^2$) can be calculated by [105]:

$$\frac{S_{ID}}{I_D{}^2} = \frac{qkt\lambda N_t}{WLC_{ox}f\gamma}\frac{g_m{}^2}{I_D{}^2}\left(1 + \frac{\alpha\mu_{eff}C_{ox}I_D}{g_m}\right)^2, \quad (5)$$

where W and L are the width and length of the channel, λ is the tunneling attenuation distance, N_t is the volumetric oxide trap density, C_{ox} is the gate-oxide capacitance, g_m is the transconductance, α is the scattering parameter, and γ is the characteristic exponent. The calculation results showed that the $LaLuO_3$-gated device exhibited one to two orders of magnitude higher low-frequency noise than the standard MOSFETs, which is comparable to the devices with Hf-based dielectrics, implying that $LaLuO_3$ is a suitable candidate for balancing the tradeoff between device performance and device scaling.

3.3. Thin-film Transistors (TFTs)

TFT is a field-effect transistor operating as a voltage-controlled current source, and its conducting channel is formed in a thin film of semiconductor (<100 nm). When a bias is applied to the gate, carriers are accumulated at the interface between the gate dielectric and the thin-film semiconductor, thus forming a conducting layer as the channel. With an electric field along this channel generated by an applied drain-source bias, a drain current is created. Similar to the traditional MOSFET theory, the charges and traps in the gate dielectric and at the dielectric/semiconductor interface can influence the carrier mobility and threshold voltage, and so it is also important to improve the qualities of the high-k dielectric and the interface. For the development of TFT in a large-area flat-panel display with high resolution, the requirements cannot be satisfied by conventional Si as the channel material due to the low carrier mobility of amorphous Si and the non-uniform spatial distribution of grain structure in poly-Si. Oxide semiconductor as a channel material for TFT was proposed and studied at the beginning. ZnO TFTs were intensively studied from 2003 due to its high Hall mobility (~200 cm^2/Vs). Also, La-based high-k dielectrics were investigated, and especially a recent report proposed a solution-process method for $LaAlO_3$ deposition (spray pyrolysis) without the need for a vacuum environment to produce a TFT with μ_{eff} of 12 cm^2/Vs, I_{on}/I_{off} ratio of 10^6 and SS of 650 mV/dec [106]. Unfortunately, the deposited ZnO film was polycrystalline and so suffered from grain-boundary

problems, leading to inadequate carrier mobility. After that, amorphous oxide semiconductor started to attract attention, and materials including ZnInSnO, ZnSnO, GaZnSnO, HfInZnO, and InZnO have all been investigated for TFT applications [107–111]. However, considering all the requirements of TFT (e.g. carrier mobility, thermal stability, controllability of carrier concentration, compatibility with current processing techniques), InGaZnO (IGZO) has become the most promising channel material.

First reported in late 2004 [112], IGZO TFT has been applied for mass production and sales since 2013, and adopted in high-end electronic products including iPad Pro and Surface Pro. Also, owing to the problems of scaling down, studies have been made on the use of high-k dielectric for IGZO TFT, especially focusing on La-based high-k materials in recent years. HfLaO was the first La-based high-k dielectric investigated for IGZO TFT in 2009 and achieved low V_{th} (0.22 V), small SS (76 mV/dec), high carrier mobility (25 cm^2/Vs), and large I_{on}/I_{off} ratio (5×10^7), which was the best performance among devices with other high-k gate dielectrics (e.g. Y_2O_3, Si_3N_4, AlTiO) [113]. However, there is still much room for improvement. Therefore, different annealing ambients for HfLaO film were then studied with results showing that N_2 was a better annealing ambient than O_2 and NH_3 and the carrier mobility could reach 35 cm^2/Vs [114]. After that, more La-based ternary oxides have been studied with good results obtained. The characteristics of IGZO TFTs with promising La-based dielectrics are listed in Table 3 according to recent investigations [42,114–117], in which ZrLaO provided the highest carrier mobility (67.2 cm^2/Vs) but lower high-field reliability, while $LaAlO_3$ was able to achieve low operating voltage (0.29 V) and small SS (98 mV/dec) but low mobility (5.4 cm^2/Vs). Comprehensively speaking, NbLaO is the best candidate due to relatively high mobility (28.0 cm^2/Vs), relatively low V_{th} (1.84 V), high on/off ratio (3.6×10^7), and negligible hysteresis (0.07 V).

Table 3. Characteristics of IGZO TFTs with La-based high-k gate dielectrics.

Dielectrics	La_2O_3 [114]	HfLaO [114]	TaLaO [115]	NbLaO [42]	ZrLaO [116]	$LaAlO_3$ [117]
$\mu_{sat}(cm^2 \cdot V^{-1} \cdot s^{-1})$	16.6	35.1	23.4	28.0	67.2	5.4
V_{th} (V)	2.14	3.3	2.4	1.84	2.59	0.29
Hysteresis (V)	−0.61	−0.03	0.1	−0.07	−0.56	–
I_{on}/I_{off} (10^7)	1.7	0.51	2.6	3.6	0.11	0.011
SS (mV/dec)	210	206	177	170	240	98
C_{ox} ($\mu F/cm^2$)	0.21	0.24	0.262	0.26	–	0.23
k	8.5	10.9	11.8	10.1	8.9	10.4
RMS (nm)	0.96	–	0.51	0.24	0.82	–

As the large-area flat-panel display is developing for flexible applications nowadays, the idea of applying organic semiconductors as channel material has been proposed. Among the organic semiconductors, only a few have been reported to produce TFT's with a carrier mobility higher than 1 cm^2/Vs, namely 6T, dinaphtho [2, 3-b:29, 39-f] thieno [3, 2-b] thiophene (DNTT), and pentacene, with pentacene showing the greatest potential. Similarly, investigations of a pentacene-based organic thin-film transistor (OTFT) with La-based high-k dielectrics in recent years have achieved impressive device performances. C. Y. Han, et al. studied La incorporation into Y_2O_3, ZrO_2, and Nb_2O_5 for pentacene OTFT applications, and results showed that La incorporated in ZrO_2 and Nb_2O_5 significantly reduced their traps, thus increasing the carrier mobility [118]. The carrier mobilities of ZrLaO- and NbLaO-gated OTFTs were 70 times and 300 times those of their counterparts based on ZrO_2 and Nb_2O_5 respectively. However, the trap density in Y_2O_3 was increased by the La doping, leading to a degradation in carrier mobility. From another perspective, with Zr, Nb or Y added in La_2O_3, the moisture absorption of La_2O_3 could be suppressed, and so larger pentacene grains were grown on the smoother oxide surface (Figure 15a), thus resulting in higher carrier mobility. Table 4 lists the device properties of pentacene OTFT's with La-based ternary oxides as gate dielectrics [41,118–122], with both NbLaO and TaLaO providing carrier mobility higher than 1 cm^2/Vs. Similar to IGZO TFT, NbLaO can also achieve high performance for OTFT (high carrier mobility and high on/off ratio), which indicates its high potential in the applications of flexible electronics.

Table 4. Characteristics of pentacene OTFTs with La-based high-k gate dielectrics.

Dielectrics	La_2O_3 [118]	HfLaO [119]	HfLaON [120]	ZrLaO [121]	TaLaO [41]	LaYO [118]	NbLaO [122]
$\mu_{sat}(cm^2 \cdot V^{-1} \cdot s^{-1})$	0.091	0.71	0.71	0.72	1.21	0.33	1.14
V_{th} (V)	−2.51	−1.3	−0.69	0.97	2.66	−2.45	−1.35
I_{on}/I_{off} (10^4)	0.87	10	1.99	0.96	3.21	0.24	29
SS (V/dec)	476	78	427	578	339	646	208
C_{ox} ($\mu F/cm^2$)	0.223	0.95	0.297	0.236	0.234	0.222	0.222
k	7.54	21.7	11.5	10.6	10.9	8.46	10.8
RMS (nm)	0.96	–	0.138	–	0.357	–	0.326

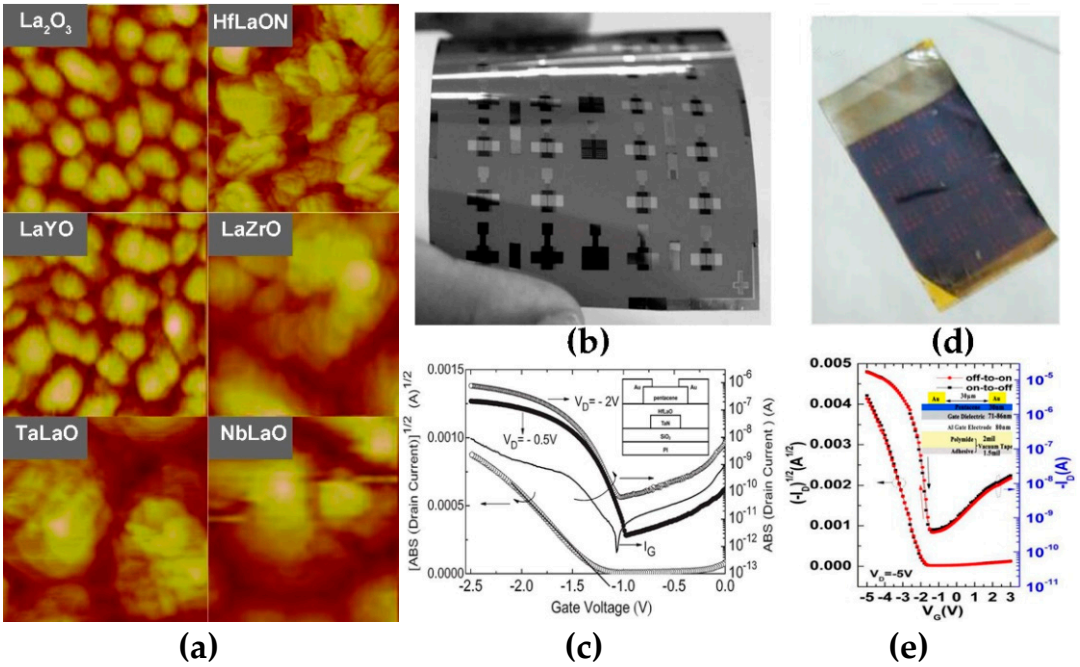

Figure 15. Pentacene OTFT: (**a**) surface morphology (1 μm × 1 μm) of pentacene films grown on different La-based high-k dielectrics [118], (**b**) devices made on PI substrate, (**c**) transfer characteristics for HfLaO gate dielectric on PI substrate [123], (**d**) devices made on vacuum tape, and (**e**) transfer characteristics for NbLaO gate dielectric on vacuum tape [124].

For flexible applications, pentacene OTFTs with La-based dielectrics have been tried on flexible substrates recently. M. F. Chang et al. reported pentacene OTFT on flexible polyimide (PI) (Kapton HPP-ST, Dupont) with HfLaO as a gate dielectric (Figure 15b) [123]. The device structure is depicted in the inset of Figure 15c: a 30 nm HfLaO dielectric was deposited on a TaN gate, followed by an O_2 treatment for 30 min at 200 °C, and Au was used as the source/drain electrodes. According to the transfer characteristics in Figure 15c, the carrier mobility, SS, V_{th}, and I_{on}/I_{off} ratio were extracted to be 0.13 cm^2/Vs, 130 mV/dec, −1.25 V, and 1.2 × 10^4 respectively, which can be useful for flexible electronics. Recently, vacuum tape has been reported to be the substrate of pentacene OTFT with NbLaO as a gate dielectric (Figure 15d) [124]. With the device structure shown in the inset of Figure 15e, Al electrode was first evaporated on vacuum tape as a gate electrode; then an 80 nm NbLaO film was deposited by RF sputtering; a PDA was performed in N_2 for 20 min at 200 °C; and Au was thermally evaporated as the source/drain electrodes. Similarly, the transfer characteristics in Figure 15e are used for parameter extraction, and the the carrier mobility, SS, V_{th}, and I_{on}/I_{off} ratio are 4.8 cm^2/Vs, 174 mV/dec, −1.90 V, and 4.52 × 10^4 respectively, which are impressive. Especially, the carrier mobility in this work is higher than most previously reported on OTFT's with flexible substrates, and is comparable to the highest (9.5 cm^2/Vs) up till now [125].

3.4. Ge and III-V Metal-oxide-semiconductor (MOS) Devices

In order to further increase the drive current of transistors to meet the requirements in the future, semiconductors with higher carrier mobility have been investigated to replace Si for a few decades. The replacement began with strained Si and SiGe, but limitations were found in mobility degradation and V_{th} shift. The next step was using Ge due to its superior intrinsic electron mobility (3900 cm^2/Vs) and hole mobility (1900 cm^2/Vs). Unfortunately, the insufficiently oxidized interfacial layer (GeO_x) with high D_{it} could significantly deteriorate the performance of Ge MOS devices, and so the studies in recent years mainly focused on the passivation of the Ge surface for lower D_{it}.

Rare-earth oxides (e.g. CeO_2, Dy_2O_3, Gd_2O_3 and La_2O_3) have been suggested for passivating the oxide/Ge interface. Especially for La_2O_3, a stable La-germanate interlayer can be formed as mentioned in Section 2.2 (Figure 10a), and is capable of inhibiting the volatilization of the GeO sub-oxides at the Ge surface, thus suppressing the formation of interfacial defects [126]. O. Bethge et al. reported the characteristics of an Au-Ti alloy/ZrO_2/La_2O_3/Ge gate stack, in which La_2O_3 was the interfacial passivation layer (IPL) (1 nm) and ZrO_2 was the gate dielectric (6.5 nm), both deposited by ALD [127]. The PDA was in Ar for 5 min at 350 °C and the post-metallization annealing (PMA) was performed in forming gas (H_2:N_2 = 1:9) for 30 min also at 350 °C. The extracted k value of the dielectric stack was promising (14.7), but the D_{it} at midgap of 1.2×10^{12} $cm^{-2}\cdot ev^{-1}$ was still not low enough. After that, nitrogen incorporation during the deposition of La_2O_3 by RF sputtering has been studied [128]. In order to suppress the moisture absorption of LaON, a 1-nm Al_2O_3 was deposited also by sputtering for covering purposes. Conditions for the PDA and PMA were 500 °C in N_2 for 5 min and 300 °C in forming gas (H_2:N_2 = 5:95) for 20 min respectively. Obvious improvements after nitrogen incorporation were obtained and LaON achieved a low D_{it} with the Ge substrate (4.96×10^{11} $cm^{-2}\cdot ev^{-1}$). Moreover, La-based ternary oxides and dual passivation layers have been investigated with good results available, and the characteristics of Ge MOS devices with La-based dielectrics and/or passivation layers reported recently are summarized in Table 5 [56,127–132].

Table 5. Characteristics of Ge MOS devices with La-based high-k oxides as IPL or gate dielectric.

Dielectric	La_2O_3 [56]	ZrO_2 [127]	LaON [128]	HfO_2 [129]	LaTiON [130]	HfTiON [131]	HfO_2 [132]
IPL	–	La_2O_3	–	LaON	–	LaTaON	TaON/LaON
Deposition	E-beam	ALD	Sputtering	Sputtering	Sputtering	Sputtering	Sputtering
T_{ox} (nm)	5.5	7.5	8	10	8	7	8
k	–	14.7	18.8	19.2	24.6	27.7	20.9
J_g (A/cm^2) at V_{FB}+/−1 V	1×10^{-4}	–	2.89×10^{-4}	5.53×10^{-4}	2.2×10^{-3}	7.8×10^{-4}	1.77×10^{-4}
CET (nm)	–	1.92	–	2.0	1.2	1.1	1.49
D_{it} ($cm^{-2}\cdot ev^{-1}$)	8×10^{11}	1.2×10^{12}	4.96×10^{11}	4.2×10^{11}	3.1×10^{11}	7.8×10^{11}	5.32×10^{11}

The ZrO_2/La_2O_3 dielectric stack has been applied by W. B. Chen et al. in Ge n-MOSFET with a laser annealing (LA) treatment to increase its gate capacitance density [133]. The 5-nm high-k IPL and dielectric stack were deposited by PVD, followed by a PDA in O_2. Then, the LA was performed in the air with laser spot sizes of 0.3 cm^2 (after focus) and 0.9 cm^2 (without focus) for n^+/p junction and high-k dielectric respectively and was stepped continuously in the x and y directions until the whole sample was covered. Results showed that with the LA treatment, C_{ox} rose from 1.8 $\mu F/cm^2$ to 2.7 $\mu F/cm^2$, thus decreasing the EOT from 1.6 to 0.95 nm. Besides, good transistor characteristics including high carrier mobility ($\mu_{eff,\ peak}$ ~600 cm^2/Vs), small SS (106 mV/dec) and low V_{th} (0.18 V) were obtained.

Compared with Ge, III–V compound semiconductors own even higher electron mobility and so have become promising candidates for Si replacement. Among all the III–V compounds, GaAs with five times higher electron mobility and larger band gap (1.42 eV) than Si has attracted the most attention in recent years, especially in MOS devices with high-k gate dielectrics. However, like Ge, GaAs also suffers from high D_{it} caused by its unstable and easily-formed native oxides [127], which lead to severe Fermi-level pinning. Therefore, similarly, the biggest challenge for GaAs-based MOS devices with high-k dielectrics is the surface passivation of GaAs to improve the interface quality. Si and Ge were

first studied as IPL with D_{it} reduction obtained [134,135]. However, since Si and Ge are amphoteric dopants for GaAs, the doping concentration in the channel might be influenced and so oxide IPLs are preferred. As mentioned in Section 2.2, the La-silicate interfacial layer is capable of improving the interface quality between Si and La_2O_3, and so the idea of applying an La_2O_3/Si stack has been proposed by T. Das et al. [136]. The Si and La_2O_3 layers were deposited on Zn-doped p-GaAs by RF sputtering, and a PDA at 500 °C in N_2 for 1 min was implemented. According to XPS analysis, La-O–Si bond was obviously detected, implying the formation of an LaSiO passivation layer. Like Ge, La-based complex oxides and dual IPL have been tried on GaAs recently with improvements achieved, and the characteristics are listed in Table 6 [136–142]. Compared with Ref. 129, improvements can be found in Refs. [137–142], indicating that as IPL, La-based oxides with nitrogen incorporation can provide higher interface quality with GaAs than with Si. In particular, for the case of $LaAlO_3$ deposited by molecular-beam deposition, D_{it} reached the order of 10^{10} $cm^{-2}{\cdot}ev^{-1}$, which is comparable to those of Si-based MOS devices.

Table 6. Characteristics of GaAs MOS devices with La-based high-k oxides as IPL or gate dielectric.

Dielectric	La_2O_3 [136]	LaYO [137]	$LaAlO_3$ [138]	$LaLuO_3$ [139]	TaYON [140]	ZrON [141]	NbAlON [142]	LaTiON [143]
IPL	Si	–	–	–	LaTaON	LaGeON	LaAlON	LaON
Deposition	Sputtering	ALD	MBD	ALD	Sputtering	Sputtering	Sputtering	Sputtering
T_{ox} (nm)	15	14	10	12	10	10	10	10
k	7.5	22	6.8	25	22.9	12.7	25.5	25.3
J_g (A/cm^2) at $V_{FB}+/-1$ V	1.2×10^{-5}	–	8×10^{-8}	–	1.3×10^{-5}	3.8×10^{-5}	6.2×10^{-6}	2.3×10^{-5}
CET (nm)	7.8	2.48	5.73	1.87	1.71	3.07	1.48	1.54
Hysteresis (mV)	260	–	30	–	35	30	45	–
D_{it} ($cm^{-2}{\cdot}ev^{-1}$)	1.2×10^{12}	5×10^{11}	5×10^{10}	7×10^{11}	9×10^{11}	1.2×10^{12}	7×10^{11}	1.05×10^{12}

Another III–V compound, GaN, has recently drawn considerable attention in high-speed, high-temperature and high-power applications due to its wide bandgap (3.3 eV), high breakdown field (~5×10^6 V/cm) and high electron saturation velocity. Much efforts have been made on GaN-based high-electron-mobility transistor (HEMT), especially with AlGaN/GaN substrate. Unfortunately, the trapping/detrapping of surface states and the high channel temperature under high drain voltage (V_{ds}) are the main concerns that lead to output-power degradation and generation of undesirable harmonic signals at high input swing. Therefore, a high-k insulator is needed between the gate electrode and the AlGaN Schottky layer in order to solve these problems without sacrificing the gate-to-channel modulation ability [144]. H.C. Chiu et al. reported an AlGaN/GaN MOS HEMT with La_2O_3 as a gate dielectric, and the device structure and TEM image of the gate stack are illustrated in Figure 16a [145]. According to the comparison of transfer characteristics between the La_2O_3 MOS HEMT and conventional GaN HEMT, the gate-to-channel modulation ability was slightly suppressed by the existence of the dielectric, leading to a slight decrease of drain current. However, the La_2O_3 MOS HEMT exhibited a flatter transconductance (g_m) vs. V_{gs} curve than the standard HEMT (Figure 16b), indicating that the intermodulation of a high-frequency signal could be reduced by the La_2O_3 layer and the distortion problem under high-power operation could be suppressed. The lower 1/f noise of the La_2O_3 MOS HEMT than that of the conventional HEMT (Figure 16c) implies that plasma-induced surface states could be avoided by the La_2O_3 dielectric. Besides, the C-V curve of the MOS-ring capacitor (Figure 16d) shows a sharp transition from depletion to two-dimensional electron gas (2DEG) accumulation, demonstrating a high-quality interface. Later, $LaAlO_3$ has been applied as the dielectric layer in MOS HEMT by C.Y. Tsai, et al., and was deposited by e-beam evaporation with a 400 °C PDA in O_2 for 5 min [146]. The transfer and mobility characteristics are shown in Figure 16e, from which low V_{th} (0.1 V), small on-resistance (R_{on}) (13.5 Ω·mm), high breakdown voltage (385 V), and relatively high peak mobility (201 cm^2/Vs) are obtained. Therefore, the insertion of the La_2O_3 dielectric in GaN-based HEMT has high potential to improve the device performance for high-power and high-linearity amplifier applications.

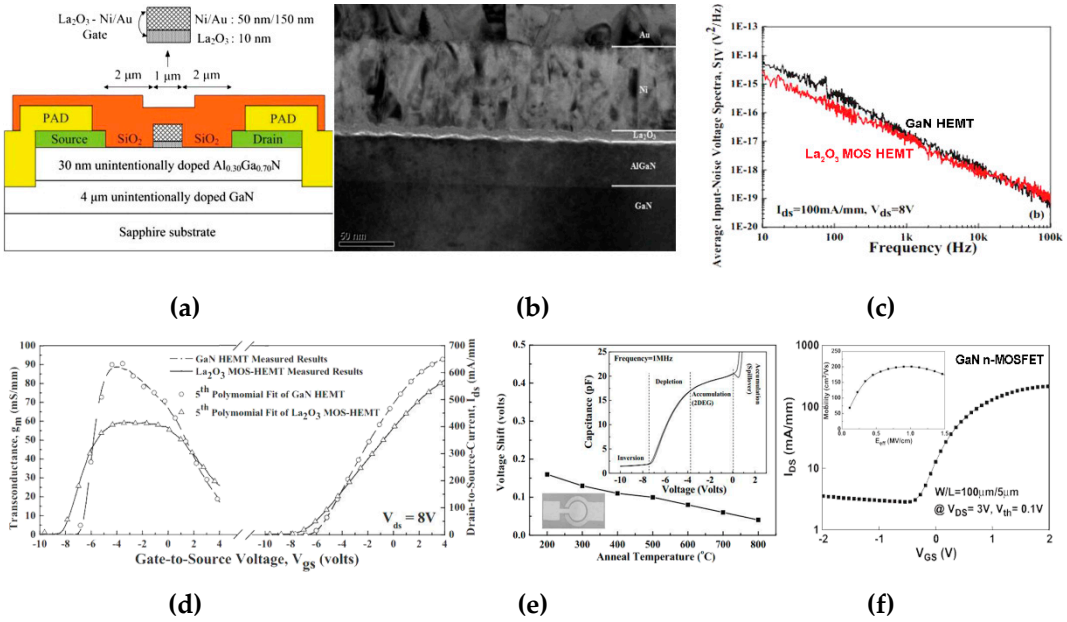

Figure 16. (**a**,**b**) Device structure and TEM image, (**d**) I–V, (**c**) noise, and (**e**) C-V and hysteresis voltage shift properties of La_2O_3 AlGaN/GaN MOS-HEMT [146]. (**e**) I–V and mobility characteristics of GaN n-MOSFET [145].

3.5. Other Novel Metal-oxide-semiconductor (MOS) Devices

For better supporting the roadmap of the semiconductor industry beyond the 14-nm technology node, fin field-effect transistor (FinFET) with multi-gate is considered to be the best candidate in order to avoid the adverse impact from the short-channel effects. Unlike MOSFET with one channel at the surface of the semiconductor substrate, FinFET has multiple channels which increase the equivalent channel width, but its working principle is same as that of the traditional MOSFET. Therefore, La-based high-k dielectrics are also promising in FinFET for the purpose of its down-scaling. Early in 2008, L. Witters, et al. tried La_2O_3 as a thin capping layer for HfSiO gate dielectric in FinFET [147]. Results showed that the La_2O_3 capping layer was effective in fabricating nFinFETs with low V_{th}, which is consistent with the discussion in Section 2.3 that the V_{th} of nFETs can be shifted in the negative direction by the insertion of La_2O_3. Recently, double-gate (DG) and tri-gate (TG) FinFETs with La_2O_3 as gate dielectric have been studied through device simulation. In Ref. [148], DG FinFETs with different gate dielectrics were simulated by the PADRE simulator from MuGFET. The device structure is shown in Figure 17a, where the gate length (L_g), EOT, fin width (W_{ch}), extension length to source/drain (L_s/L_d), channel and drain/source doping concentrations are set to be 12, 2, 10, 20 nm, 1×10^{16} cm^{-3} and 1×10^{19} cm^{-3}, respectively. According to the simulation results in Figure 17b, La_2O_3 gate dielectric provided the smallest drain-induced barrier lowering (DIBL) (53 mV/V) and SS (85 mV/dec). Besides, when compared to SiO_2, La_2O_3 exhibited a 132% increase in g_m, indicating its better gate control on the drain current. The same simulation was also performed on GaAs FinFET, and similarly, La_2O_3 was capable of achieving the smallest DIBL (47 mV/V), lowest SS (76 mV/dec), and highest g_m among all the gate dielectrics [149]. As for TG FinFET, simulation was carried out on SOI substrate by the SILVACO TCAD simulator with the device structure depicted in Figure 17d [150]. The L_g, EOT, fin width and height, buried-oxide thickness, body, and source/drain doping concentrations are set as 30, 1.2, 10, 20 nm, 5×10^{17} cm^{-3}, and 5×10^{20} cm^{-3}, respectively. Results showed that the V_{th}, SS and I_{on}/I_{off} of La_2O_3-gated FinFET are 0.312 V, 63.7 mV/dec and 6.2×10^6 respectively, which are comparable to those of a device with an HfO_2 gate dielectric.

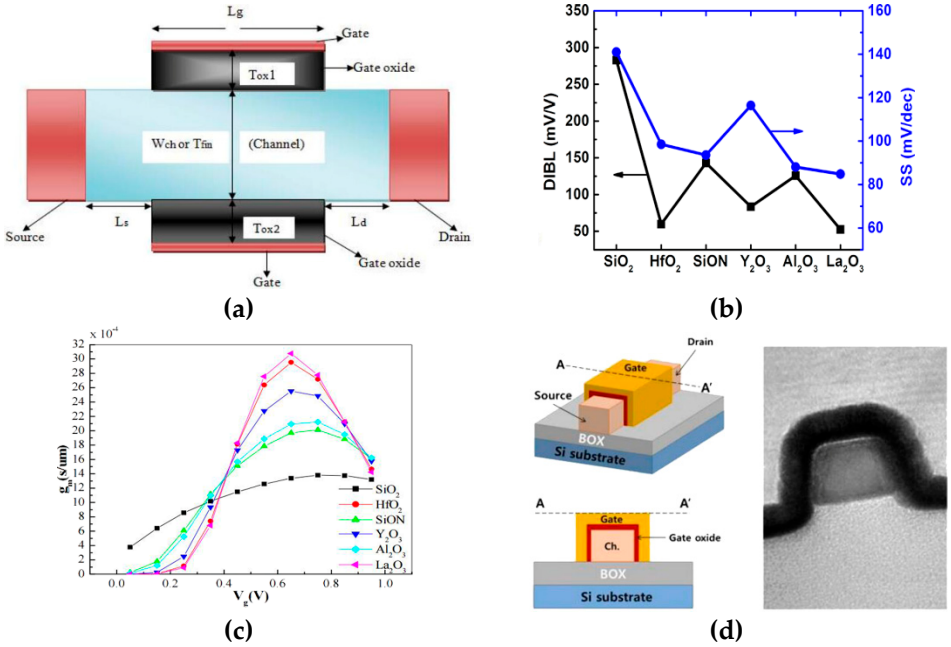

Figure 17. (**a**) Device structure, (**b**) DIBL and SS characteristics, and (**c**) g_m of DG FinFET's with different gate dielectrics [148,149]. (**d**) Device structure of TG FinFET [150].

Moreover, to achieve even higher drive current by devices with even smaller dimensions, the idea of nanowire-based transistors has been proposed and proved to be promising for future generations. However, the application of La-based high-k gate dielectric for nanowire transistors is still in the stage of simulation. Gate-all-around InAs transistors with different high-k gate dielectrics have been simulated based on the effective-mass theory using the Multigate Nanowire FET TCAD simulator by R. Gupta, et al [151]. The device structure is shown in the inset of Figure 18a, with a source/drain and gate length of 10 nm, oxide width (W_{ox}) of 1 nm, buried-oxide thickness (T_{box}) of 5 nm, substrate body width (W_{InAs}) of 5 nm, and substrate thickness of 25 nm. Similar to the results of FinFET with different high-k dielectrics, La_2O_3 outstood among the high-k materials, especially in transfer behavior and SS, as demonstrated in Figure 18a,b. Besides, an InGaAs/InAlAs nanowire superlattice FET (SL-FET) with HfO_2/La_2O_3 gate dielectric has been simulated by a full-band quantum simulator and its structure is shown in Figure 18c [152]. An optimal on-state current I_{on} of 1 mA/μm has been achieved at a gate voltage of 0.4 V, and a small SS (27 mV/dec) could sustain for six decades of drain current. Particularly, when comparing the HfO_2/La_2O_3 and Al_2O_3 gate dielectrics, with an interface-trap density of 1.6×10^{11} cm^{-2}, HfO_2/La_2O_3 could provide almost the same transfer behavior as Al_2O_3 without interface traps. Therefore, SL-FET with an La-based high-k dielectric should be a promising candidate for the future semiconductor industry.

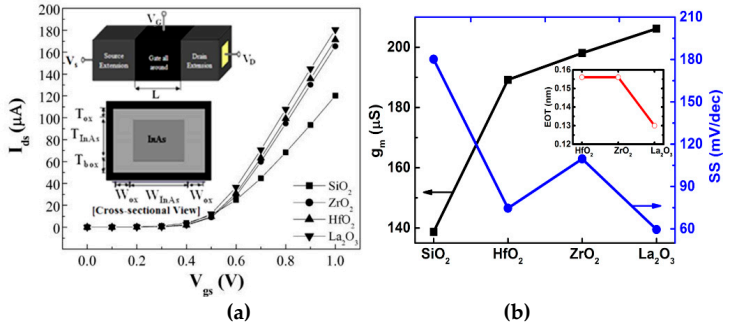

Figure 18. *Cont.*

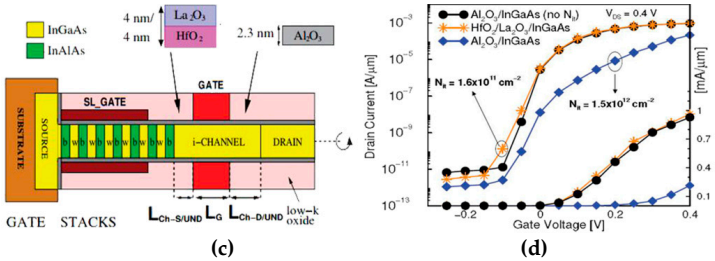

Figure 18. (**a**) Transfer characteristics and (**b**) I_{on}, I_{off}, g_m and I_{on}/I_{off} ratio of InAs nanowire gate-all-around transistors with different gate dielectrics [151]. (**c**) Device structure and (**d**) transfer characteristics of InGaAs/InAlAs nanowire superlattice-FET's with Al_2O_3 and HfO_2/La_2O_3 gate dielectrics [152].

4. Conclusions and Future Prospects

The progress of La-based high-k dielectrics in recent years has been reviewed, with an emphasis on MOS applications. Owing to its large band gap and high k value, La_2O_3 is considered as a promising gate dielectric for MOS devices. However, through the analyses on the physical and chemical characteristics of La_2O_3, its hygroscopicity and defects (including oxide traps, interface states and grain-boundary states) are the major concerns that lead to a degradation in device performance. The solutions to these problems can be summarized as: (i) high-temperature annealing in N_2 or inert gas, (ii) nitrogen incorporation, (iii) laser treatment, and (iv) doping of other high-k metal element (M) to form complex high-k ternary oxide. From another perspective, incorporating La into other high-k binary oxides is capable of passivating oxygen vacancies and modifying the flatband voltage of the MOS system and so improves the qualities of the dielectric film and high-k/semiconductor interface and reduces the V_{th} of the nFETs respectively, thus contributing to higher drive current and lower power consumption for meeting the future requirements of the semiconductor industry. According to the review of La-based dielectrics in different MOS devices, including non-volatile memory, MOSFET, TFT, Ge device, III-V device, FinFET and nanowire-based transistor, LaMO (M = Al, Hf, Nb, Ti, Ta, Zr, Y, and Lu) with or without nitrogen incorporation as a gate dielectric or passivation layer could provide impressive performance for Ge and III-V devices, especially with the MBD-deposited $LaAlO_3$ achieving a very low D_{it} in the order of 10^{10} $cm^{-2}{\cdot}eV^{-1}$. Besides, based on simulation results, La_2O_3 showed high potential as the gate dielectric of FinFET and nanowire transistors. All these advantages of La-based high-k dielectrics can pave the way for the MOS research in the directions of higher speed, lower power consumption and smaller dimensions, based on transistors with novel structures (e.g., tunnel FET), 2D material (MoS_2, graphene, etc.)-based transistors, and nanowire transistors with metal nano-structural plasmonics in MOS mode.

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