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Study on the Physical and Leakage Current Characteristics of an Optimized High-k/InAlAs MOS Capacitor with a HfO_2–Al_2O_3 Laminated Dielectric

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Abstract: High-k/n-InAlAs MOS capacitors are popular for the isolated gate of InAs/AlSb and InAlAs/InGaAs high-electron mobility transistors. In this study, a new kind of high-k/n-InAlAs MOS-capacitor with a HfO_2–Al_2O_3 laminated dielectric was successfully fabricated using an optimized process. Compared with the traditional HfO_2/n-InAlAs MOS capacitor, the new device has a larger equivalent oxide thickness. Two devices, with a HfO_2 (8 nm)–Al_2O_3 (4 nm) laminated dielectric and a HfO_2 (4 nm)–Al_2O_3 (8 nm) laminated dielectric, respectively, were studied in comparison to analyze the effect of the thickness ratios of HfO_2 and Al_2O_3 on the performance of the devices. It was found that the device with a HfO_2 (4 nm)–Al_2O_3 (8 nm) laminated dielectric showed a lower effective density of oxide charges, and an evidently higher conduction band offset, making its leakage current achieve a significantly low value below 10^{-7} A/cm^2 under a bias voltage from −3 to 2 V. It was demonstrated that the HfO_2–Al_2O_3 laminated dielectric with a HfO_2 thickness of 4 nm and an Al_2O_3 thickness of 8 nm improves the performance of the high-k dielectric on InAlAs, which is advantageous for further applications.

Keywords: high-k/InAlAs MOS-capacitor; HfO_2–Al_2O_3 laminated dielectric; leakage current; *C*–*V* characteristics

1. Introduction

Owing to the requirements of high speed, low dissipation, and low noise for modern integrated circuits, InAs/AlSb and InAlAs/InGaAs high-electron mobility transistors (HEMTs) are receiving great attention as new III–V compound devices because of their high electron mobility and electron saturation drift speed [1–4]. Because of its good compatibility with AlSb, InAs, and InGaAs, InAlAs is one of the most promising materials for the protection layer of InAs/AlSb and InAlAs/InGaAs HEMTs to enhance the carrier density in the channel [1,3]. Depositing a high-k dielectric film on InAlAs as a MOS capacitor can effectively suppress the leakage current [5–9]. However, the lack of reasonable high-k dielectrics is still a major problem that limits the performance of the isolated gate. HfO_2 is the main candidate for the high-k dielectric because of its high dielectric constant [5,7], but its direct deposition on InAlAs limits its performance owing to the poor lattice match with InAlAs [8]. Therefore, a thin Al_2O_3 film inserted between InAlAs and HfO_2 as a buffer layer has been proposed [8]. This structure can increase the quality of the MOS capacitor by providing a better match with InAlAs. Reference [8] initially reported the electrical and interfacial characteristics of a HfO_2–Al_2O_3/n-InAlAs MOS-capacitor. However, in [8], the impact of the thickness of HfO_2 and Al_2O_3 on the performance of the device was not investigated, and the leakage current performance, which is considered as the most important electrical characteristic of the MOS-capacitor was not mentioned either. In order to

optimize the fabrication process and improve the performance of the high-k/InAlAs MOS-capacitor with an HfO_2–Al_2O_3 laminated dielectric, a new kind of HfO_2–Al_2O_3/n-InAlAs MOS-capacitor was manufactured in this study, and its optimized fabrication process was discussed in detail. Two samples with HfO_2 (8 nm)/Al_2O_3 (4 nm) and HfO_2 (4 nm)/Al_2O_3 (8 nm) were designed and prepared to investigate the effect of the different thickness ratios of HfO_2 and Al_2O_3. Devices were tested by atomic force microscope (AFM), Focused Ion beam (FIB), scanning electron microscope (SEM), and X-ray photoelectron spectroscopy (XPS) to describe the physical characteristics. Based on the capacitance (C)–voltage (V) and current (I)–V test results, their physical characteristics were analyzed and their electrical characteristics, including the leakage current, were investigated in detail.

2. Materials and Methods

The structure diagram of the MOS capacitor is shown in Figure 1. To match with InAlAs and achieve better performance, InP was selected as the substrate rather than GaAs, which were frequently used in other studies [7–9]. InP is semi-insulating and a 350-μm-thick substrate was used. To decrease the lattice mismatch with InAlAs, a 200-nm-thick InP buffer layer was grown on the InP substrate by MBE at 470 °C. A 500-nm-thick Si-doped $In_{0.5}Al_{0.5}As$ layer with a doping concentration of 1×10^{17} cm^{-3} was deposited on the InP buffer layer. The high-k dielectric was then deposited by atomic layer deposition (ALD) [10–13]. The details of the ALD process to produce the HfO_2–Al_2O_3 laminated dielectric are given in Table 1. We controlled the ALD process circle to manufacture different dielectric thicknesses. A post-deposition annealing (PDA) process was applied to increase the quality of the oxide-semiconductor interface [14–17]. The process involved heating the film from ambient temperature to 380 °C in N_2 over 15 s, annealing for 60 s, and then cooling to ambient temperature over 300 s [6,7]. Finally, a Ti (20 nm)/Pt (20 nm)/Au (200 nm) metal structure was grown as the electrode by the magnetron sputtering technique. We grew two electrodes with different areas. The area of the small one is 150 μm × 150 μm (marked as C_1 in Figure 1), and the area of the large one is 1500 × 1500 μm^2 (marked as C_2 in Figure 1). When a voltage is applied between the two electrodes, C_1 is connected in series with C_2. Because the area of C_2 is 100 times larger than the area of C_1, the influence of C_2 on the total capacitance can be neglected, and the measured capacitance can be approximately equal to the value of C_1. The electrodes that grow on top of the oxide layer can avoid the pollution caused by the back contact process used in [8] (e.g., the metal directly deposited on the surface of InAlAs).

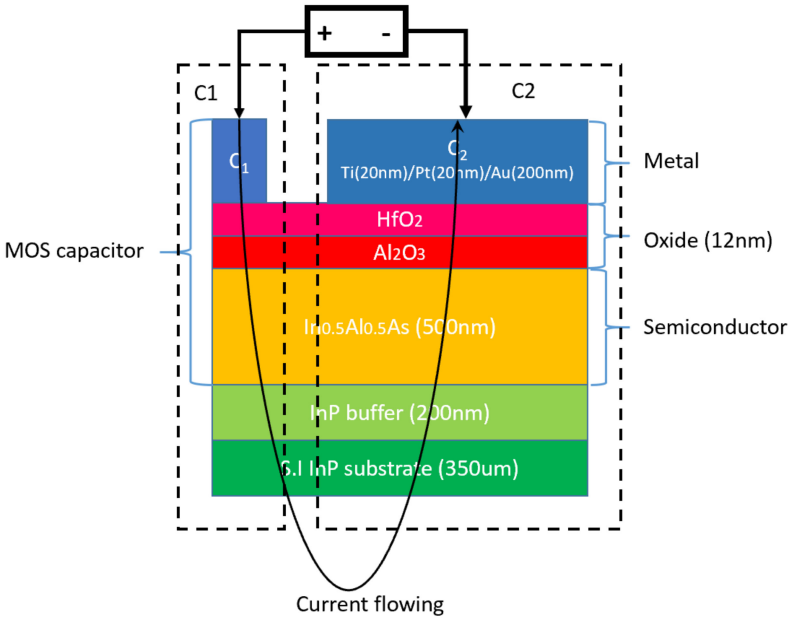
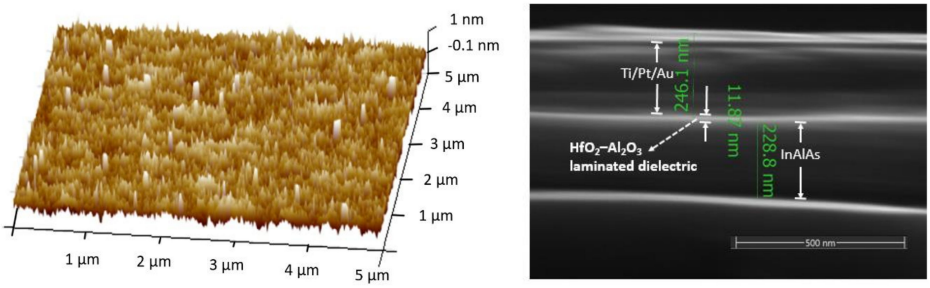


Figure 1. Structure diagram of the MOS capacitor.

Table 1. ALD process to prepare the HfO_2–Al_2O_3 dielectric.

Dielectric	Precursor	Pulse Time (s)	Deposition Temperature (°C)	Pressure (mbar)	Deposition Speed (nm/s)
Al_2O_3	TMT + N_2 + H_2O + N_2	0.5 + 2 + 0.5 + 1	245	2.3	0.1
HfO_2	TEMAH + N_2 + H_2O + N_2	1 + 2 + 1 + 2	245	2.3	0.1

A simple HfO_2/n-InAlAs MOS capacitor with an oxide thickness of 12 nm and two HfO_2–Al_2O_3/n-InAlAs MOS capacitors with HfO_2 (8 nm)/Al_2O_3 (4 nm) and HfO_2 (4 nm)/Al_2O_3 (8 nm) laminated dielectrics were fabricated. These three samples were designed to have the same physical oxide thickness of 12 nm for convenient comparison. The surface roughness RMS (root-mean-square) values of the three samples which are taken from the AFM test are observed as small, around 0.5 nm. The 5 μm × 5 μm AFM graph of the HfO_2 (4 nm)/Al_2O_3 (8 nm) MOS capacitor is show in Figure 2a. The FIB-SEM image of the across-section of the HfO_2 (4 nm)/Al_2O_3 (8 nm) MOS capacitor is shown in Figure 2b. These indicate a compactable and homogeneous device structure.



(**a**) (**b**)

Figure 2. (**a**) AFM graph of the HfO_2 (4 nm)/Al_2O_3 (8 nm) MOS capacitor; (**b**) FIB-SEM image of the across-section of the HfO_2 (4 nm)/Al_2O_3 (8 nm) MOS capacitor.

3. Results and Discussions

The accumulated capacitances of the MOS-capacitors C_{OX} were measured by the high-frequency capacitance method at 1 MHz, and the results are shown in Figure 3. The HfO_2/InAlAs MOS capacitor has a highest C_{OX} of 0.68 μF/cm^2, while the C_{OX} is lower with an inserted Al_2O_3 thin film. The C_{OX} value decreases with increasing thickness of the inserted Al_2O_3 layer. The highest C_{OX} values of the HfO_2 (8 nm)/Al_2O_3 (4 nm)/InAlAs and HfO_2 (4 nm)/Al_2O_3 (8 nm)/InAlAs MOS capacitors are 0.517 and 0.355 μF/cm^2, respectively. It is noted that C_{OX} shows a decrease as the MOS capacitor is driven further into accumulation. This is induced by the obvious leakage current under the high voltage bias condition. In addition, a low *C*–*V* hysteresis is observed for the sample with HfO_2 (4 nm)/Al_2O_3 (8 nm) laminated dielectrics. The reason can be explained by its lowest density of oxide charges that we discuss herein.

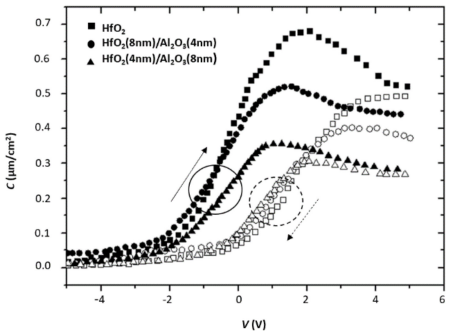


Figure 3. *C*–*V* measurements of the MOS capacitors.

The equivalent oxide thickness (EOT) values of the three samples were determined from the *C*–*V* curves [7,9]. The results are given in Table 2. Inserting Al_2O_3 increases the EOT. When the thickness of Al_2O_3 is 4 and 8 nm, the EOT values are 6.68 and 9.73 nm, respectively. Because the electric field intensity E_i is inversely proportional to the EOT for fixed bias voltage V_g, the higher EOT indicates that inserting an Al_2O_3 film between InAlAs and HfO_2 decreases E_i under the same V_g, which will help to decrease the leakage current. It is noted that the increased EOT would degrade the gate control ability of the device. The equivalent dielectric constant ε_{OX} was calculated according to the *C*–*V* test data [18]. The two samples with a HfO_2/Al_2O_3 laminated dielectric have lower ε_{OX} values than the sample with only a HfO_2 dielectric, and the ε_{OX} value decreases as the thickness of the Al_2O_3 film increases. This can be explained by the lower dielectric constant of Al_2O_3 than HfO_2.

Table 2. Physical and electrical parameters of the HfO_2/n-InAlAs and HfO_2–Al_2O_3/n-InAlAs MOS capacitors.

Parameter	HfO_2/n-InAlAs	HfO_2 (8nm)/Al_2O_3 (4nm)/n-InAlAs	HfO_2 (4nm)/Al_2O_3 (8nm)/n-InAlAs
C_{OX} (μF/cm^2)	0.680	0.517	0.355
EOT (nm)	5.08	6.68	9.73
ε_{OX}	9.22	7.01	4.81
C_{FB} (μF/cm^2)	0.374	0.319	0.249
V_{FB} (V)	−0.31	−0.44	−0.23
N_{eff} (cm^{-2})	1.83×10^{12}	1.81×10^{12}	0.78×10^{12}
ΔE_{CB} (eV)	1.120	1.179	1.563

The effective density of oxide charges N_{eff}, which indicates the quality of the MOS capacitor, and can be estimated from the flat-band capacitance C_{FB} and flat-band voltage V_{FB} [7,19]. The estimated values for the samples are listed in Table 2. First, we will compare the N_{eff} values of the samples with a single HfO_2 dielectric and a HfO_2 (8 nm)/Al_2O_3 (4 nm) laminated dielectric. Because Al_2O_3 possesses better matching with InAlAs than HfO_2, inserting an Al_2O_3 film improves the interface quality [8,9], which helps to suppress spreading of the impurities in the dielectric layer. However, another interface is generated between Al_2O_3 and HfO_2 because of insertion of the Al_2O_3 film, leading to generation of additional interface states, which will induce an increase in traps. These competing effects mean that the N_{eff} values of the two samples are similar. The N_{eff} values are 0.78×10^{12} cm^{-2} for the sample with a HfO_2 (4 nm)/Al_2O_3 (8 nm) laminated dielectric and 1.81×10^{12} for the sample with a HfO_2 (8 nm)/Al_2O_3 (4 nm) laminated dielectric. Thus, N_{eff} decreases as the thickness of Al_2O_3 increases. This reduction can be explained by the better interfacial quality of the sample with a thicker Al_2O_3 layer. In addition, the stability of Al_2O_3 is higher than HfO_2 and the oxygen atoms in Al_2O_3 are more difficult to remove by other impurity bonds (e.g., In– and As–) to form In–O and As–O traps, so the sample with a thicker Al_2O_3 layer has lower N_{eff}. For verification, XPS was performed to check the diffusion states of the As and In elements in the oxide layer. The XPS spectra before and after 30 s etching on the oxide layer are shown in Figure 4 (30 s etching is estimated to reach 6nm depth of oxide layer). The XPS spectra is shown in Figure 4. In general, the As 3*d* and In 3*d* peaks before etching are lower than those after 30 s etching because of the blocking action of the high-k dielectric on impurities. Compared with the Hf–O bond, the Al–O bond shows a stronger blocking effect on diffusion of impurity particles, so the sample with HfO_2 (4 nm)/Al_2O_3 (8 nm) has a lower concentration of As than the sample with HfO_2 (8 nm)/Al_2O_3 (4 nm). Although Al_2O_3 can block the diffusion of As, the 4 nm thickness does not perform a good blocking role, indicating that Al_2O_3 must have a reasonable thickness for a good blocking effect on impurities. Diffusion of As in the oxide layer is suppressed when the thickness of Al_2O_3 is increased to 8 nm, which suppresses the formation of charge traps in the oxide layer and reduces the N_{eff} value. In addition, the In content before etching is negligible because of the weak diffusion of In in the oxide layer. The lower N_{eff} is helpful to suppress the hysteresis phenomenon in the *C*–*V* curve. This explains the lowest *C*–*V* hysteresis for the sample with the HfO_2 (4 nm)/Al_2O_3 (8 nm) laminated dielectric (Figure 3).

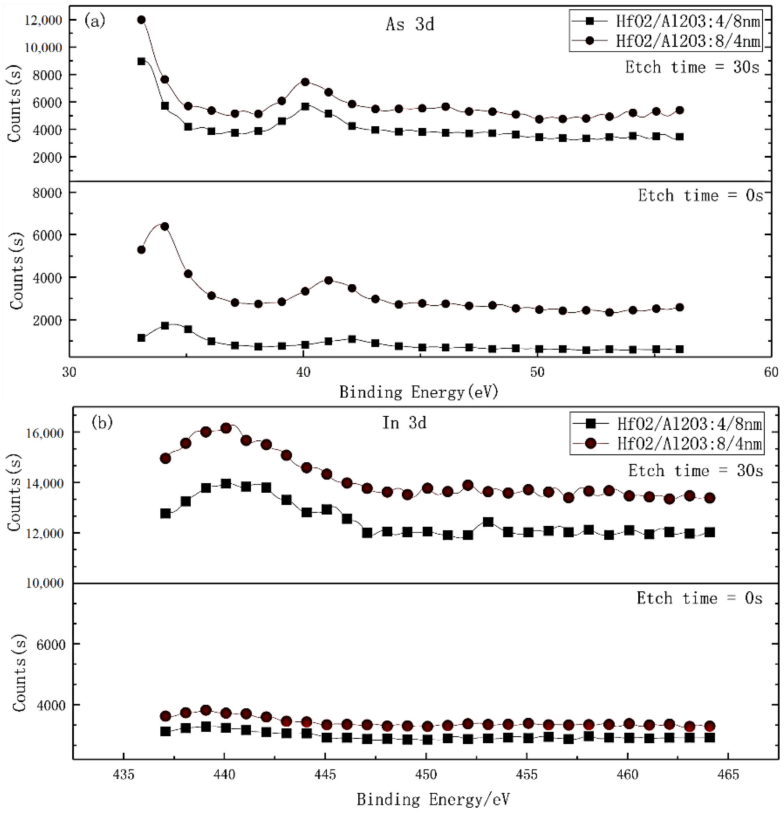


Figure 4. XPS spectra before and after etching for 30 s: (**a**) As 3*d*; (**b**) In 3*d*.

The leakage currents of the MOS capacitors are shown in Figure 5. For negative bias voltage, compared with the reported results in [7,9], the leakage current density of the new HfO_2 (4 nm)/Al_2O_3 (8 nm)/n-InAlAs MOS capacitor is significantly lower in the V_g range from −3 to 2 V (below 10^{-7} A/cm^2), and it is one order of magnitude lower than that of the HfO_2/n-InAlAs MOS capacitor. One reason is that inserting an Al_2O_3 film enhances the match between HfO_2 and InAlAs by suppressing the formation of a low-k interfacial layer. In addition, Al_2O_3 has a higher barrier height than HfO_2, which makes the HfO_2–Al_2O_3/n-InAlAs MOS capacitor possess less accessibility for carriers to overcome the barrier and form leakage current. Under positive bias voltage, electrons cross the barrier at the high-k/InAlAs interface (φ_B) and contribute to the leakage current [20,21]. In general, the conduction band offset (ΔE_{CB}) between oxide and the semiconductor layer is used to determine φ_B [6]. To further investigate the reason for the barrier effect on the leakage current, ΔE_{CB} was calculated by the Krant method [6]. The results are listed in Table 2. It should be noted that the sample with HfO_2 (4 nm)/Al_2O_3 (8 nm) laminated dielectric shows the highest band offset ΔE_{CB} (1.563 eV), which can be explained by its higher barrier height of Al_2O_3, so the sample with an 8-nm-thick Al_2O_3 film shows significantly lower leakage current. The sample with HfO_2 (8 nm)/Al_2O_3 (4 nm) laminated dielectric shows a competitive ΔE_{CB} value single (1.179 eV) with the sample with HfO_2 dielectric (1.120 eV). However, the sample with HfO_2 (8 nm)/Al_2O_3 (4 nm) laminated dielectric shows a higher leakage current than the sample with single HfO_2 dielectric when a positive bias voltage is applied. It can be explained as following: A 4nm Al_2O_3 layer is too thin to suppress the leakage current effectively; meanwhile, the additional states on the Al_2O_3–HfO_2 interface degrade the leakage current. Therefore, the sample with HfO_2 (8 nm)/Al_2O_3 (4 nm) dielectric shows the lowest leakage. The leakage current mechanism of devices is complicated, and will be investigated in detail in our next work.

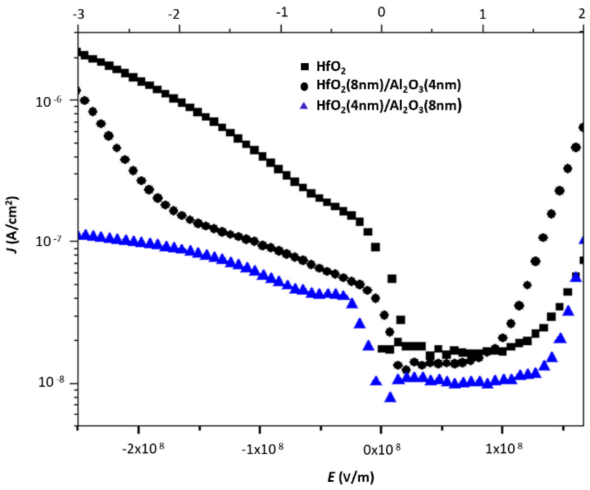


Figure 5. Leakage current density J_{leakage} measurements under bias voltage from −3 to 2 V for the three MOS capacitors.

The physical and electrical parameters of the HfO_2/n-InAlAs and HfO_2–Al_2O_3/n-InAlAs MOS capacitors are compared in Table 2.

4. Conclusions

In conclusion, compared with the HfO_2/n-InAlAs MOS capacitor, the HfO_2–Al_2O_3/n-InAlAs MOS capacitor has the higher EOT and lower N_{eff}, which help to suppress the leakage current. The HfO_2–Al_2O_3/n-InAlAs MOS capacitor has a high conduction band offset, making its leakage current below 10^{-7} A/cm^2 under bias voltage from −3 to 2 V. Therefore, the Al_2O_3–HfO_2 laminated dielectric improves the high-k gate dielectric on InAlAs and suppresses the leakage current. The HfO_2–Al_2O_3/n-InAlAs MOS capacitor with HfO_2 thickness of 4 nm and Al_2O_3 thickness of 8 nm is a good candidate for the isolated gate of InAs/AlSb and InAlAs/InGaAs HEMTs.

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Conflicts of Interest: The authors declare no conflict of interest.

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