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Low-Temperature Deposition of High-Quality SiO_2 Films with a Sloped Sidewall Profile for Vertical Step Coverage

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Abstract: SiO_2 is one of the most widely used dielectric materials in optical and electronic devices. The Josephson voltage standard (JVS) chip fabrication process has rigorous requirements for the deposition temperature and step-coverage profiles of the SiO_2 insulation layer. In this study, we deposited high-quality SiO_2 insulation films at 60 °C using inductively coupled plasma-chemical vapor deposition (ICP-CVD) to fulfill these requirements and fabricate JVS chips simultaneously. SiO_2 films have a high density, low compressive stress, and a sloped sidewall profile over the vertical junction steps. The sidewall profiles over the vertical junction steps can be adjusted by changing the radio frequency (RF) power, ICP power, and chamber pressure. The effects of sputtering etch and sloped step coverage were enhanced when the RF power was increased. The anisotropy ratio of the deposition rate between the sidewall and the bottom of the film was lower, and the sloped step coverage effect was enhanced when the ICP power was increased, or the deposition pressure was decreased. The effects of the RF power on the stress, density, roughness, and breakdown voltage of the SiO_2 films were also investigated. Despite increased compressive stress with increasing RF power, the film stress was still low and within acceptable limits in the device. The films deposited under optimized conditions exhibited improved densities in the Fourier transform infrared spectra, buffered oxide etch rate, and breakdown voltage measurements compared with the films deposited without RF power. The roughness of the film also decreased. The step-coverage profile of the insulation layer prepared under optimized conditions was enhanced in the junction and bottom electrode regions; additionally, the performance of the device was optimized. This study holds immense significance for increasing the number of junctions in future devices.

Keywords: inductively coupled plasma-chemical vapor deposition; film stress; silicon oxide; step coverage

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1. Introduction

SiO_2 is one of the most widely used dielectric materials in optical and electronic devices, such as insulators [1], dielectric barriers [2], and waveguides [3]. The properties of SiO_2 films that are critical for providing insulation, such as the step-coverage profile (or gap-filling effectivity), film stress, and breakdown voltage, are also crucial for robust device operation. Typically, trade-offs exist between different properties in their optimization, when choosing the deposition parameters in the processing window. However, there are instances in which simultaneous optimization is required. For example, in the fabrication of superconductive Josephson junction chips according to the Josephson voltage standard (JVS), SiO_2 film deposition is complex. On the substrate, two or three junction stacks are etched with a vertical sidewall to obtain the same junction areas for the vertically stacked junctions such that they have the same critical current and normal resistance. Additionally, the SiO_2 insulation layer should have very low stress and good insulation to make the

device robust enough for cooling cycles from room temperature to 4.2 K. Furthermore, the column microstructures of the sputtered Nb films tend to form grain boundaries near the rectangular or cusping step corners, as shown in Figure 1a, causing the Josephson junctions to show a hysteresis current-voltage (*I-V*) curve (Figure 1b) or even device failure. The columnar grain structure of the sputtered niobium can be seen more clearly in the STEM images in [4]. As shown in Figure 1a, the Nb film at the VIA sidewall does not develop grain boundary cracks because the VIA sidewall is sloped. Hence, if the SiO_2 film exhibits a sloping topography in the step coverage profile, the problem of grain boundary cracking can be overcome. Therefore, it is necessary to choose a suitable deposition method for the deposited film to meet the aforementioned conditions.

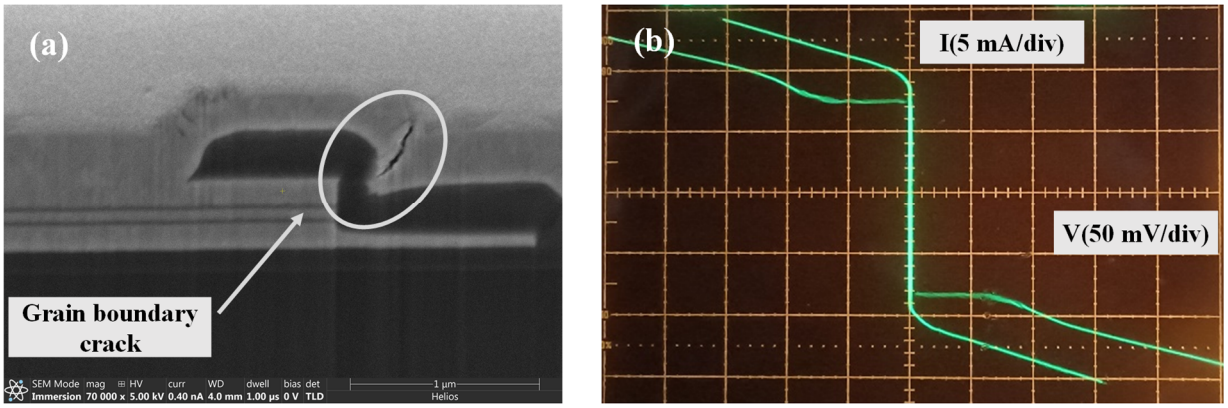

Figure 1. (**a**) Focused ion beam SEM image of an Nb grain boundary crack, and (**b**) hysterical *I-V* curve.

In the microelectronics industry, SiO_2 can be formed on silicon via thermal oxidation, plasma-enhanced chemical vapor deposition (PECVD) [5], and atomic layer deposition (ALD) [6] on different wafers. Plasma-enhanced chemical vapor deposition (PECVD) is widely used to deposit SiO_2 insulation layers but typically requires a relatively high deposition temperature of approximately 300 °C. However, for Nb/Nb_xSi_{1-x}/Nb JVS chips, it is essential to maintain the wafer temperature lower than 120 °C during fabrication, as the amorphous Nb_xSi_{1-x} barrier layer can undergo phase segregation at high temperatures [7]. Inductively coupled plasma chemical vapor deposition (ICP-CVD) uses independent ICP and RF sources. Plasma is inductively coupled to the ICP source, which regulates plasma density. The RF source is capacitively coupled to the plasma and allows for independent control of the ion energy during deposition. Hence, it is possible to obtain high-density plasmas with appropriate ion energies for ICP-CVD and deposit high-quality SiO_2 films at low temperatures (150–200 °C). Many studies have been conducted on using ICP-CVD for the deposition of SiO_2 films [8]. The influence of the process parameters on the stress, refractive index, and density of thin films is still a hot topic of research [9,10]. Many studies have focused on the effect of process parameters on electrical properties, such as capacitance-voltage (C-V) characteristics [11], breakdown electric field [12], and leakage currents [13].

Other authors have used TMS to study the mechanism of dense silicon dioxide film deposition and the behavior of plasma radicals during deposition [14]. In the early 21st century, many reports suggested that the effect of ion bombardment caused by the addition of an RF bias can optimize the gap filling and performance of SiO_2 films [15–21]. However, the deposition temperatures in these studies were typically maintained at 150–200 °C. Only a few studies on SiO_2 films deposited at 100 °C focused on the porosity, electrical properties, and stress of the thin films at low temperatures [22,23]; the SiO_2 layer tended to become less dense and more porous at ultralow temperature (<100 °C). Few reports have described the topography of thin-film step coverage at such low temperatures. However, there has been no research to solve the challenges associated with the deposition of SiO_2 films according to JVS requirements.

In this study, high-quality SiO_2 films were deposited at 60 °C to fulfill the requirements of depositing a SiO_2 insulation layer with a high density, low compressive stress, and sloped sidewall profile over the vertical junction steps, as required in JVS chip fabrication. The sidewall profiles over the vertical junction steps could be adjusted by changing the RF power, ICP power, and chamber pressure. Furthermore, the effects of RF power on the stress, density, and breakdown voltage of the SiO_2 films were studied.

2. Experimental

In this study, SiO_2 films were deposited using a Corial 200D ICP-CVD (Bernin, France) system. The apparatus is illustrated in Figure 2. Plasma was generated by an inductive coil connected to the top generator through a matching circuit. Another 13.56 MHz RF power supply was connected to the lower electrode. Upon turning the RF supply on, an RF bias was generated, and positive particles were drawn to bombard the sample surface. The gases used in SiO_2 deposition included SiH_4, Ar, and O_2. SiH_4 was fed through a gas ring near the wafer chuck, whereas O_2 and Ar entered the reaction chamber via the top shower. During the deposition, the substrate cooling chiller was set at 60 °C, and the deposition pressure was varied from 4 to 10 mTorr. The ICP source power was varied from 200 to 800 W, the RF bias power was varied from 50 to 200 W, and the RF bias was varied from 0 to 60 V.

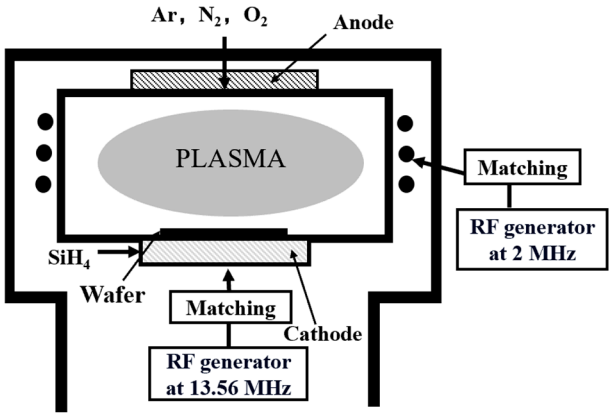

Figure 2. Schematic of the ICP-CVD apparatus.

To fabricate the substrates, a 500 nm-thick multi $Nb/Nb_xSi_{1-x}/Nb$ Josephson junction structure was sputtered on a 4-inch silicon substrate, following which vertical steps of 350-nm-height junctions were etched by reactive ion etching (RIE). The patterned substrate was cut into 2 cm × 2 cm pieces for deposition experiments. Finally, SiO_2 films were deposited on the patterned substrates at different ICP powers, RF powers, and deposition pressures to optimize the deposition parameters and obtain ideal sloped sidewall profiles.

Scanning electron microscopy (SEM, ZEISS Ultra 55, Gottingen, Cermany) was employed to observe the covering profiles of the thin films at all steps. The film thickness was measured using an ellipsometer, and the film stress was measured using a MOS KAS (k-Space, Dexter, MI, USA) stress gauge. Fourier-transform infrared (FTIR) spectroscopy (Bruker, Vertex 70V, Billerica, MA, USA) was performed to analyze the chemical bonds of the deposited SiO_2 films. A buffered solution ($HF/NH_4F/H_2O$ = 1:2:3) was used to wet-etch the film at room temperature to measure the density of the SiO_2 films. The buffered oxide etch (BOE) rate was determined by dividing the thickness of the film by the corrosion time. The surface morphology and roughness were examined using atomic force microscopy (AFM, Bruker, Dimension FastScan, Tucson, AZ, USA). The roughness values were calculated from the heights of the AFM images. Specially designed patterned samples with 300 nm thick Nb electrodes and 200 nm thick SiO_2 films were fabricated to measure the breakdown voltage using a parameter analyzer (Tektronix, Keithley 4200, Portland, OR,

USA). To confirm the functionality of the SiO_2 insulation layer, Josephson junction devices were fabricated using an optimized ICP-CVD process.

3. Results and Discussion

3.1. Influence of Process Parameters on the Step Coverage Profile

To prevent grain boundary cracking when establishing the coverage of the Nb wiring layer, the angle between the sidewall and the bottom of the ideal SiO_2 film step cover should be greater than 90°. Moreover, there should be no grooves caused by the shadow effect at the corner between the sidewall and bottom. The deposition parameters of the film were varied to achieve an ideal step cover profile. The effects of the ICP power, RF power, and working pressure on the step coverage profile were studied by evaluating the cross-sectional SEM images of the samples deposited under different conditions.

3.1.1. Effect of RF Power on the Step Coverage Profile

Figure 3 shows the step-coverage profiles for various RF power values. The SEM images show desirable sloped step coverage upon increasing the RF power to 200 W. This improvement was because the deposition rate at the step shoulder was much lower than that at the top and bottom. The deposition included contributions from the film deposition (growth) and sputter etching (removal) steps in the ICP-CVD. The deposition–sputtering ratio (D/S) is a useful parameter for describing this relationship and achieving the desired gap filling [15]. To evaluate the effect of RF power on the step coverage profile, we studied the relationship between RF power and the D/S ratio.

$$D/S = \frac{\text{deposition rate} + \text{suptter etching rate}}{\text{suptter etching rate}} \quad (1)$$

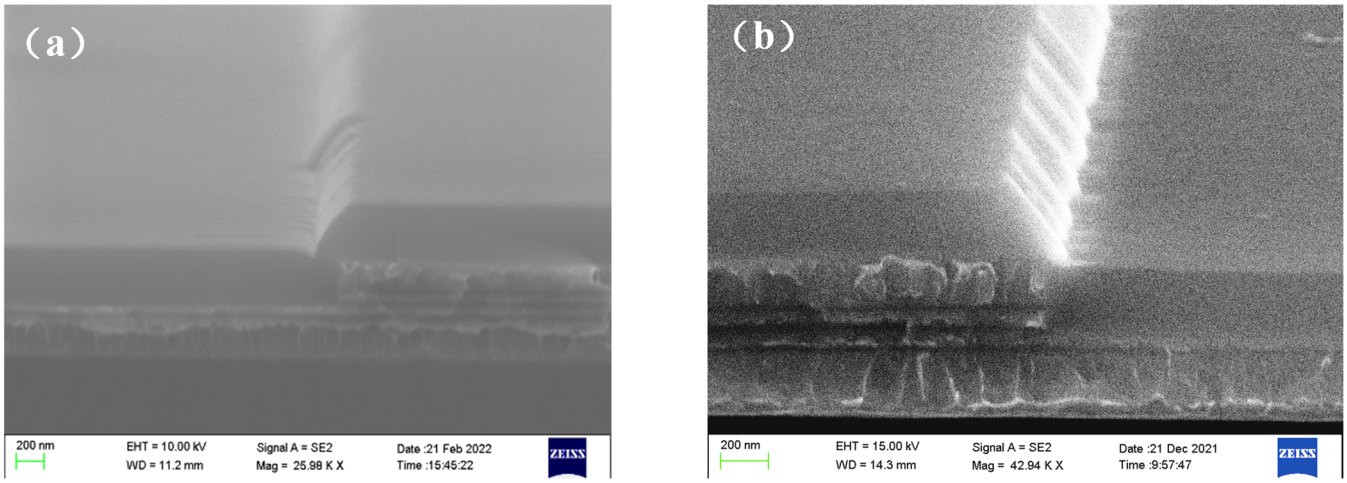

Figure 3. SEM images of the step coverage profiles for RF powers of (**a**) 100 W and (**b**) 200 W. The ICP power was set at 800 W, and the deposition pressure was set at 4 mTorr.

The deposition rate was characterized by the deposition thickness of the film per unit time. In contrast, the sputter etch rate was obtained by feeding a gas mixture of Ar and O_2, and cutting off the SiH_4 supply [17].

The deposition data for various RF powers are listed in Table 1. When the RF power was increased from 100 W to 200 W, the sputtering etching rate increased from 1.6 nm/min to 5.9 nm/min, while the D/S value decreased significantly from 41 to 11. However, the RF power did not considerably affect the net deposition rate.

Table 1. Deposition data for various RF powers.

RF Power (W)	Bias (V)	Sputtering Etching Rate (nm/min)	Deposition Rate (nm/min)	*D/S*
100	4.3	1.5	68.3	46.5
200	42	7.5	70.8	10.44

The RF power source produced a negative bias to attract positive ions in the plasma to bombard the substrate during deposition. Increasing the RF power significantly increased the positive ion energy and directionality toward the substrate surface [24]. The sputter etching rate depended on the angle between the surface plane and the incident direction of the ions and was higher in the step shoulder region than on the surface plane. Similar results have been reported for tapered sidewall profiles of gap-filled SiO_2 films fabricated by intensive ion bombardment [19]. Another noteworthy deduction from Figure 3 was that the notch where the sidewall met the top surface at the lower step disappeared with increasing RF power. This was caused by the redistribution of sputtered materials [25].

3.1.2. Effect of ICP Power on the Step Coverage Profile

In ICP-CVD, ions and neutrals contribute; hence, both ionic and radical deposition reactions occur. The directional ionic deposition reaction leads to very little sidewall growth [15,26]. In contrast, the radical deposition reaction has a conformal deposition contribution on the bottom and sidewall [17]. The effects of ICP power and deposition pressure on the coverage profile mainly depend on the balance between the two types of reactions in the deposition. To clarify the mechanism, we evaluated the anisotropy ratio, that is, the ratio of the deposition thickness on the sidewall to that at the bottom of the steps, for different process parameters:

$$\text{anisotropy ratio} = W/H \tag{2}$$

As indicated in Figure 4a, H is the bottom deposition thickness, and W is the sidewall deposition thickness. The anisotropy ratio can also represent the ratio of the deposition rate between the sidewall and bottom. When the vertical component of the incident ions is high, and the radial deposition reaction is conformal, the anisotropy ratio can be approximated using the following equations:

$$W = D_t \times t \tag{3}$$

$$H = (D_t + D_i - E) \times t \tag{4}$$

$$\text{anisotropy ratio} = \frac{D_t}{D_t + D_i - E} \tag{5}$$

where t is the deposition time, D_t is the sum of the radical deposition rates, D_i is the sum of the ionic deposition rates, and E is the sputter-etching rate on the plane [17]. Table 1 shows that E was much lower than the deposition rate; hence, we focused on the deposition rate during the analysis.

Figure 4 shows the step-coverage profiles for different ICP powers while maintaining the RF power and deposition pressure at 200 W and 6 mTorr, respectively. Figure 5 shows the anisotropy ratios of the samples, as shown in Figure 4. The anisotropy ratio decreased with increasing ICP power, and at the same time, the coverage profile was more ideally sloped. Better sloped step coverage was obtained with a higher ICP power for a higher deposition rate on the step bottom than on the lateral sidewall. This is attributed to the higher plasma density and increased ion reaction rate [18]. In this scenario, the self-shadowing effect is less, leading to better-sloped step coverage with an increased angle.

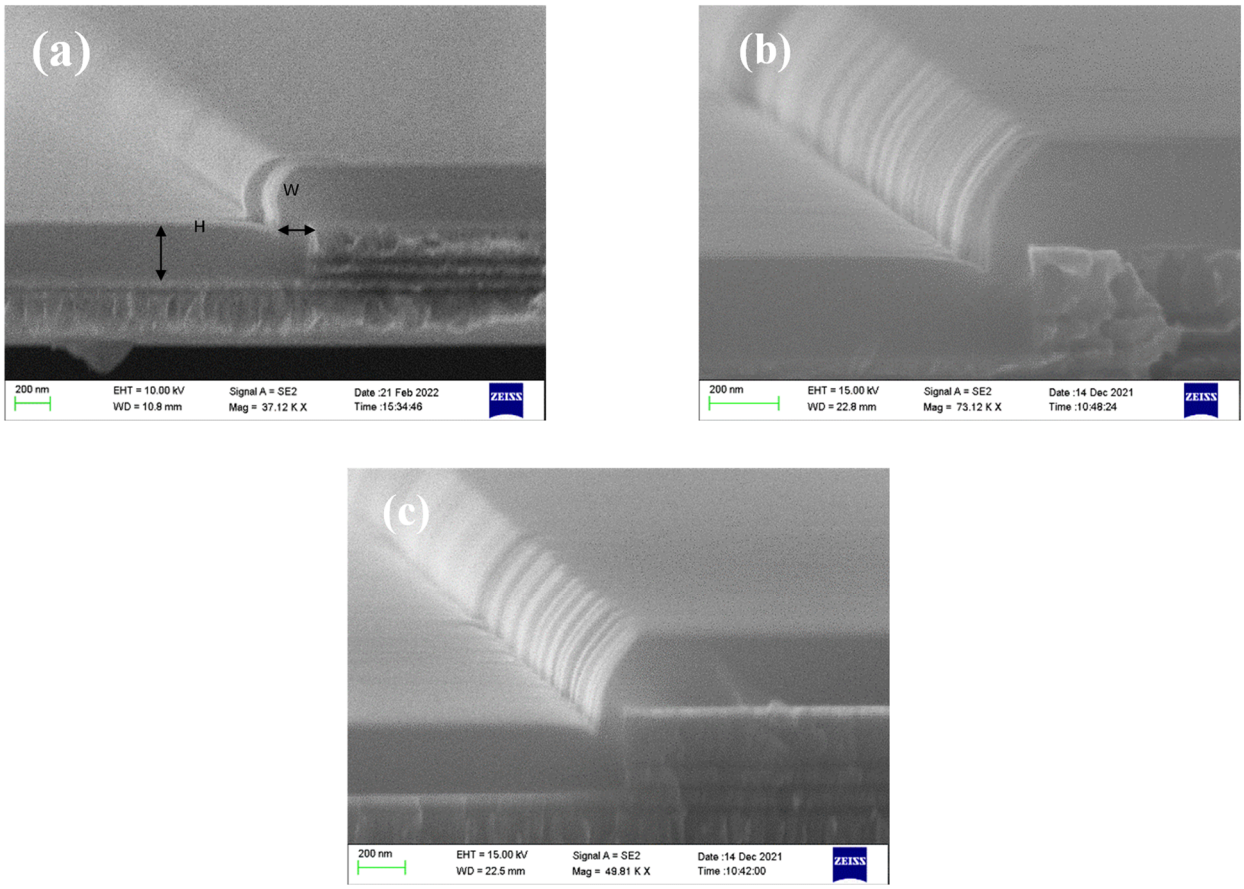

Figure 4. SEM images of the step coverage profiles for ICP powers of (**a**) 200 W, (**b**) 500 W, and (**c**) 800 W. The RF power was set at 200 W, and the deposition pressure was set at 6 mTorr.

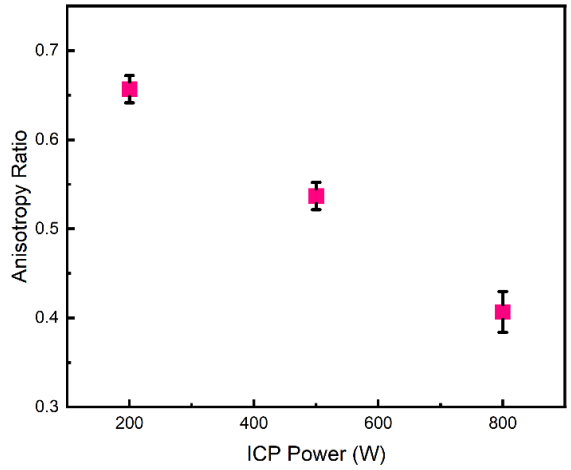

Figure 5. Anisotropy ratio of the sidewall film thickness to bottom deposition thickness for different ICP powers.

3.1.3. Effect of Deposition Pressure on the Step Coverage Profile

Figure 6 shows SEM images of the step coverage profiles at different deposition pressures. Figure 7 shows the anisotropy ratio of the sidewall thickness to the bottom thickness. Upon decreasing the film deposition pressure, there was a distinct decrease in the anisotropy ratio, and the coverage profile improved. Simultaneously, the grooves at the junction of the sidewall and bottom step of the film become narrower, and even disappeared entirely. Although a decrease in the deposition pressure induced a decrease in the plasma

density, it also induced a reduction in the isotropic backscatter in the gas phase [8] and better directionality of ions owing to fewer collisions in the sheath [11]. This increased the contribution of the ion reaction in the deposition, leading to a lower anisotropy ratio and a better coverage profile.

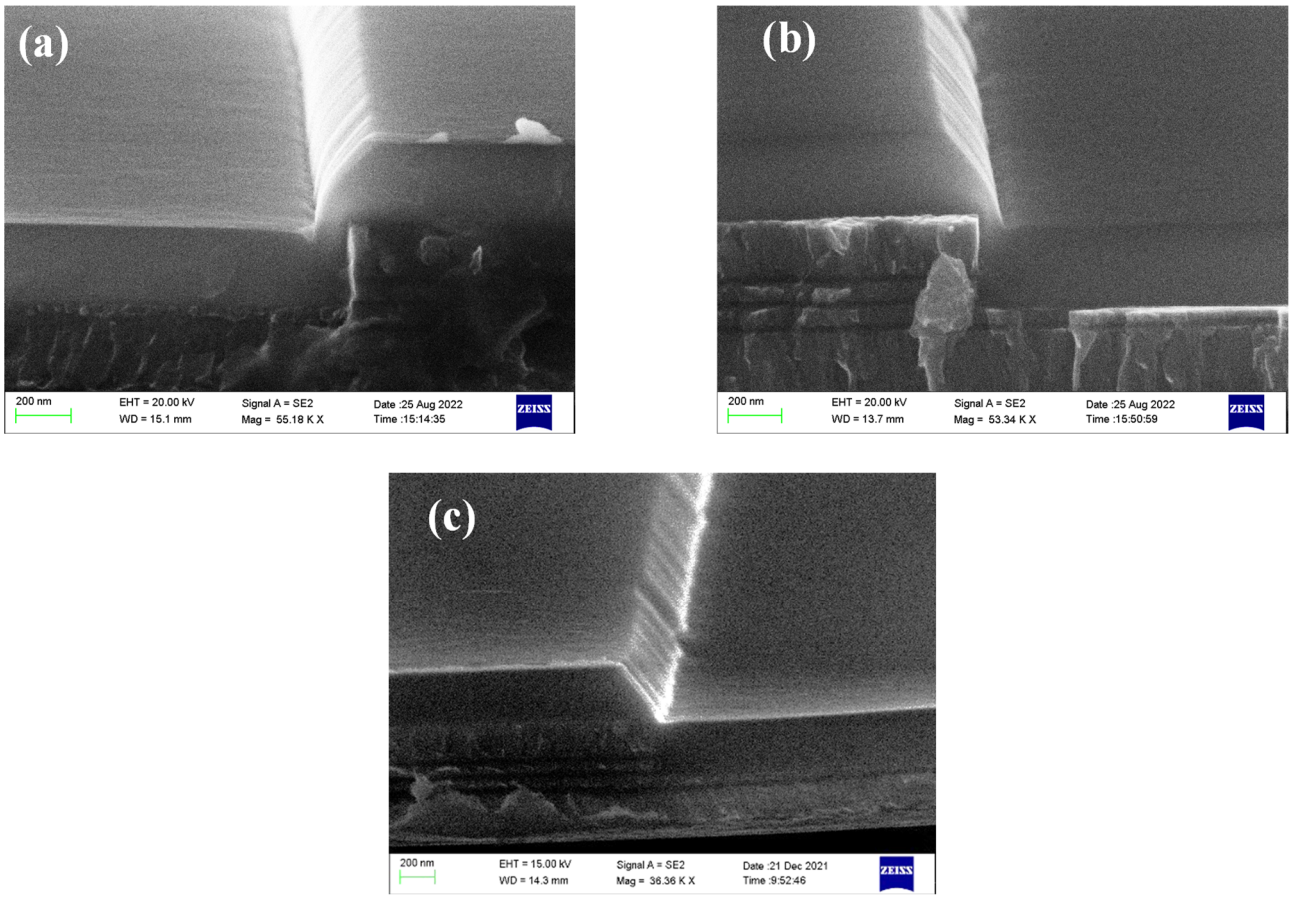

Figure 6. SEM images of the step coverage profile of the sample for deposition pressures of (**a**) 6 mTorr, (**b**) 5 mTorr, and (**c**) 4 mTorr. The RF power was set at 200 W, and the ICP power was set at 800 W.

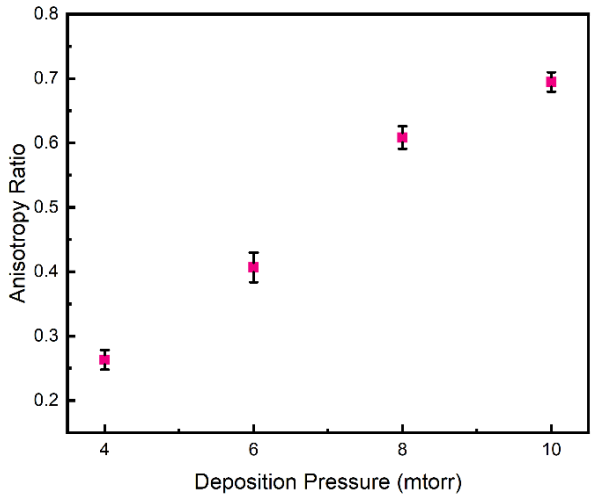

Figure 7. Anisotropy ratios of sidewall film thickness to bottom thickness for different deposition pressures.

Thus, we obtained optimized SiO_2 films deposited at a low temperature with an ideal sloped vertical step coverage profile at 60 °C. The optimized films were deposited at a pressure of 4 mTorr by applying ICP and RF powers of 800 and 200 W, respectively.

3.2. Film Properties

3.2.1. Film Stress

The application of an RF power negatively biases the substrate, which attracts positive ions to bombard the substrate surface during deposition, typically yielding compressive films due to energetic bombardment and rapid growth. The film stress was studied by depositing SiO_2 films on 2 inch Si wafers at different RF powers while maintaining the ICP power and deposition pressure at 800 W and 4 mTorr, respectively (Figure 8). The film stress was measured and calculated using a multi-beam optical scanning curvature measurement system (KSA MOS UltraScan). A negative value indicated that the stress of the SiO_2 film was compressive. Greater compressive stress was obtained by increasing the RF power in the allowed region of the equipment.

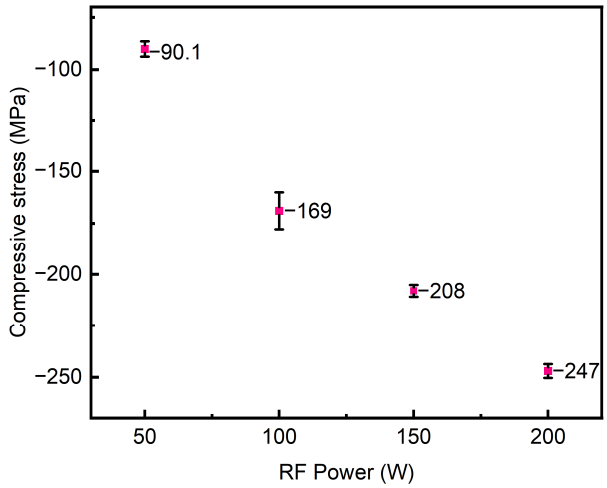

Figure 8. Compressive stress as a function of the RF power.

3.2.2. FTIR Spectroscopy

Figure 9 shows the FTIR absorption spectra of the SiO_2 film (400 nm) before (6 mTorr, ICP power: 800 W) and after (4 mTorr, ICP power: 800 W, RF power: 200 W) optimization. The characteristic peaks of Si–O–Si stretching, bending, and rocking occurred at 1000.93, 788.79, and 453.21 cm^{-1}, respectively, under the optimized conditions, and at 987.43, 783.02, and 445.50 cm^{-1} under the original conditions. Compared with the peak position of the Si–O–Si stretching band (1090 cm^{-1}), which is related to the quality of the film when it contains thermal oxides of the same thickness, the peak positions of the films deposited at 60 °C were generally lower. This is attributed to the longitudinal optical (LO) component of the high-frequency vibration of SiO_x. Porous films deposited at low temperatures have longer Si–O bonds and a certain degree of strain in the Si–O–Si bridging bonds [27]. However, the characteristic peaks of Si–O–Si increased after optimization and were closer to those of the thermal oxide, indicating an increase in the length of the $(–Si–O–)_n$ chain network [28,29].

This phenomenon is typically associated with the microscopic relaxation of the atomic structure of silica induced by ion bombardment and leads to an improvement in oxide quality, such as in terms of density [29]. Other researchers have suggested that the shoulder at 1200 cm^{-1} increases in intensity as SiO_2 films become more porous and less dense [28]. As shown in Figure 9, the absorption intensity of the shoulder at 1200 cm^{-1} decreased under the optimized conditions, signifying the densification of the SiO_2 films.

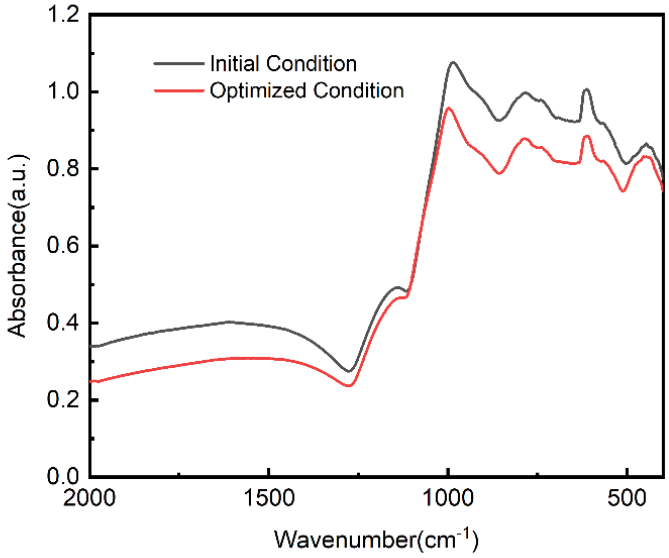

Figure 9. FTIR spectra of SiO_2 thin films under optimized conditions and initial conditions.

3.2.3. Buffered Oxide Etch (BOE) Rate

To further confirm the improvement in the quality of the film, the BOE rate was measured for the same samples on which FTIR studies were performed. A buffered solution ($HF/NH_4F/H_2O$ = 1:2:3) was used to wet-corrode the films at room temperature. The BOE results and refractive index values determined using an ellipsometer (Gaertner, LSEb Stokes, Singapore, Singapore) are listed in Table 2. The wet-etch rate of the thermally oxidized SiO_2 film was the lowest, whereas that of the deposited SiO_2 films was much higher. The etch rate of the films deposited under the optimized deposition conditions was half that of those deposited under the original conditions. Considering that the reported results of the BOE rate do not depend on the pressure in ICP-CVD when it is less than a specific range (<1 Pa) [30,31], it can be concluded that RF power-induced ion bombardment reduces the porosity of the film [29] and improves the film density. Thus, the conclusions from the FTIR results (Section 3.2.2) are verified.

Table 2. BOE etch rate and refractive index of SiO_2 films prepared under various conditions.

Deposition Condition	Refractive Index	BOE Etch Rate
Original conditions (6 mTorr, ICP power: 800 W)	1.4617	795 nm/min
Optimized conditions (4 mTorr, ICP power: 800 W, and RF power: 200 W)	1.4653	405 nm/min
Thermal oxide	1.46	85 nm/min

3.2.4. Roughness

The surface morphology of the SiO_2 films was analyzed using atomic force microscopy (AFM). Figure 10 shows the AFM and 3D images obtained from the samples with a scanning area of 1 μm × 1 μm. The surface roughness values of the films are listed in Table 3. As shown in the figure, the film after optimization had a lower roughness than the previous one. The main reason for the reduction in roughness was the addition of bias. The bombardment of ions with high energy increased the lateral migration of Si and O atoms during deposition and weakened the growth trend of the SiO_2 thin film columnar grains. The surface roughness of the film was reduced, and the surface became smoother [32].

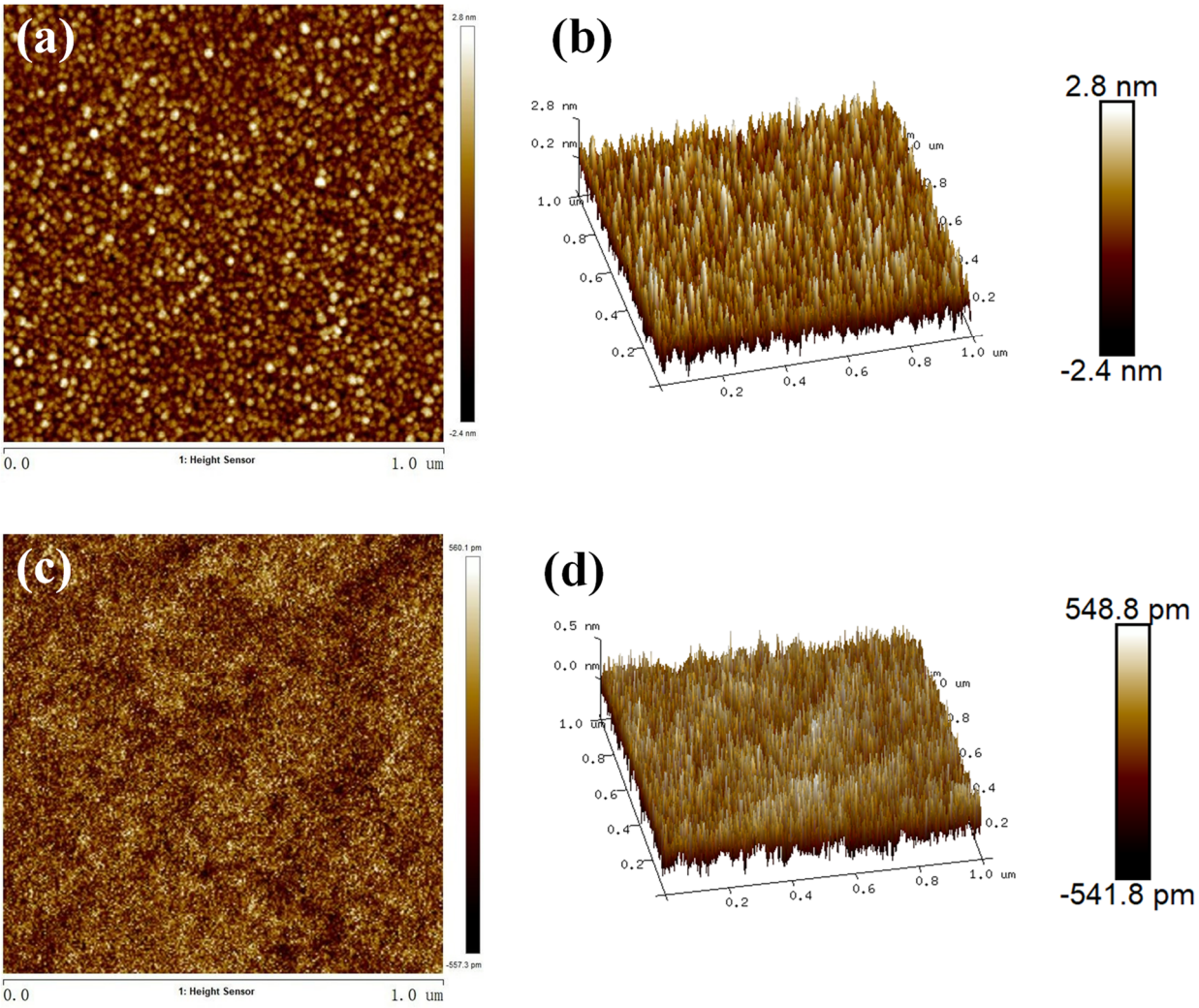

Figure 10. AFM images of SiO_2 thin films under initial conditions (**a**,**b**), and optimized conditions (**c**,**d**).

Table 3. Surface roughness (in nm) of SiO_2 films prepared under various conditions.

Deposition Condition	AVG	RMS
Original conditions	0.770	0.618
Optimized conditions	0.162	0.129

3.2.5. X-ray Reflection

X-ray reflectivity (XRR) was used to measure the thickness, density, and the surface roughness of SiO_2 films deposited under original and optimized conditions. The measured and fitted XRR patterns are shown in Figure 11. The critical angle of the optimized film was lower than that of the film deposited at the original condition. The fitted film thickness, density, and the surface roughness are listed in Table 4. Obviously, the RMS result simulated from XRR data was higher than the value obtained by AFM. This might be because XRR is a macroscopic determination, whereas AFM is performed on limited, much smaller areas [33]. Furthermore, it was measured that optimized film has an atomic density as high as 2.64 g/cm^3, whereas the film deposited at original condition had a density of 2.477 g/cm^3. It should be noted that the XRR fitted data present a similar tendency of variation for surface roughness and density, to the measurement results of AFM and BOE.

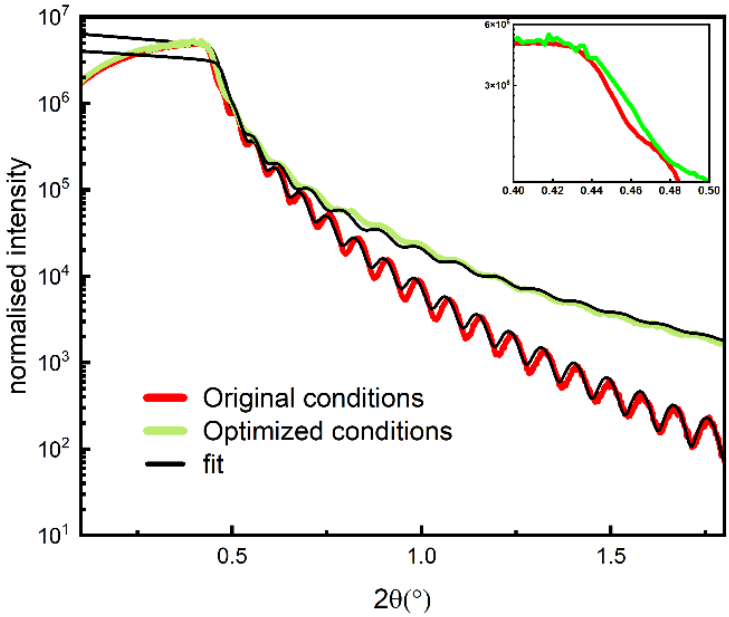

Figure 11. XRR measured and fitted patterns of SiO_2 films deposited under original and optimized conditions.

Table 4. The fitted date of SiO_2 films for both conditions.

Deposition Condition	Thinkness	Roughness	Density
Original conditions	96.35	1.3715	2.4771
Optimized conditions	75.72	0.7163	2.6429

3.2.6. Breakdown Voltage

Typical high-frequency (1 MHz) *I-V* measurements (Tektronix, Keithley 4200, Portland, OR, USA) were performed to determine the electrical properties of the SiO_2 films deposited under the original and optimized conditions. Subsequently, 300-nm-thick Nb base electrodes, 200-nm-thick SiO_2 insulation layer, and 300-nm-thick Nb top electrodes were fabricated to facilitate the measurements. The measurements were performed multiple times in different test cells on the sample, and the results are shown in Figure 12. The SiO_2 insulation layer deposited under the original conditions broke down at 60–70 V (3–3.5 MV/cm), while that deposited under the optimized conditions broke down at 80–90 V (4–4.5 MV/cm). The breakdown curves under the two conditions are shown in the insets of Figure 12. As shown in the figure, a platform caused by the charge capture effect was observed before the breakdown of the oxide layer under the process conditions, but was not observed after optimization.

The breakdown voltage was related to the macroscopic density of the film. Under similar conditions, the breakdown voltage of the film at a deposition temperature of 150 °C can reach 9 MV/cm [28]. The breakdown voltage of the film deposited at low temperature was lower than that deposited at high temperature. This was mainly because the reaction products, such as OH^- and H^+ groups, increased in concentration and coalescence, leading to the formation of voids and, eventually, to a low film density at low temperatures [22]. The results in Figure 12 show that the electrical properties of the deposited films improved when a DC self-bias was applied. This behavior correlated with the macroscopic densification effect reported in Section 3.2.3. Although the effect of the bias voltage was not as significant as the effect of temperature, it could also compensate for the deterioration of low temperature on the breakdown voltage to a certain extent, and improve electrical performance.

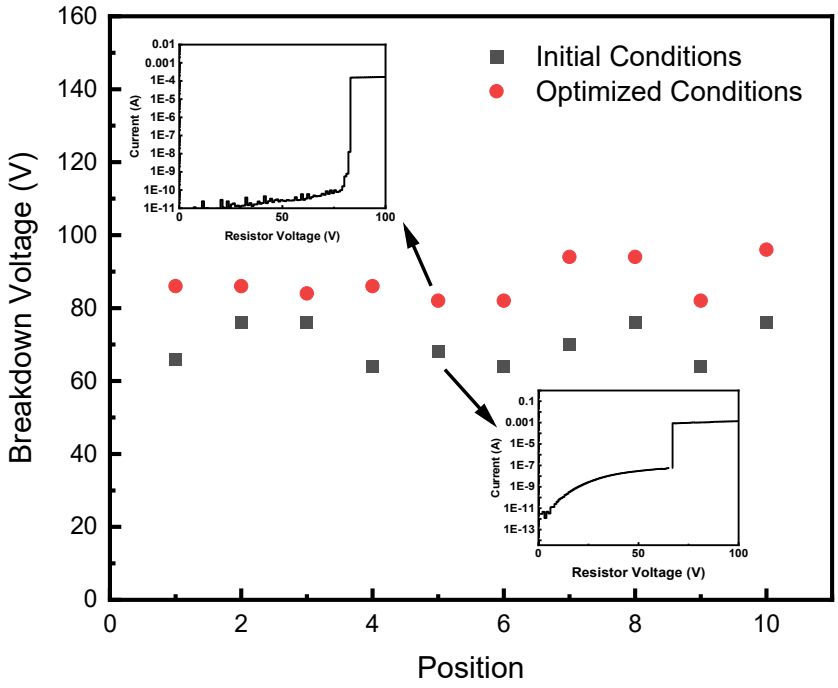

Figure 12. Breakdown voltage at various test locations under two conditions.

3.2.7. Application in the Device

A batch of superconductive Josephson junction chips was fabricated by applying an optimized SiO_2 film deposition process to confirm the functionality of the device. The measured direct-current *I-V* characteristics are shown in Figure 13. Nb films deposited by magnetron sputtering have column microstructures and tend to form grain boundaries near rectangular step corners, leading to hysterical *I-V* curves (Figure 1b). An ideal non-hysterical *I-V* curve was obtained for the fabricated Josephson junction chips, which indicates that the optimized SiO_2 film deposition process is useful for improving chip fabrication.

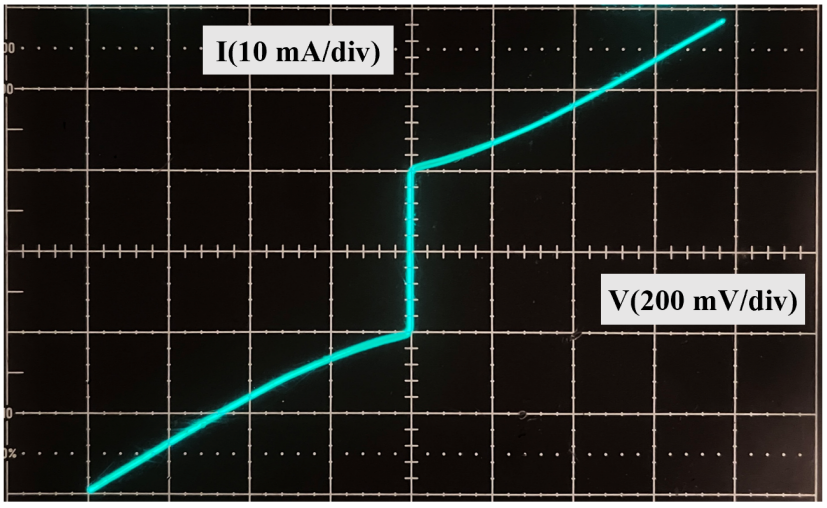

Figure 13. *I-V* characteristic curve after optimization.

4. Conclusions

In this study, we deposited high-quality SiO_2 insulation films at 60 °C using ICP-CVD to fulfill the rigorous requirements for chip fabrication according to the JVS. The SiO_2 films had a high density, low compressive stress, and sloped sidewall profile over the vertical

junction steps. The sidewall profiles over the vertical junction steps could be adjusted by changing the RF power, ICP power, and chamber pressure. The effects of sputtering etch and sloped step coverage were enhanced when the RF power was increased. The anisotropy ratio of the deposition rate between the sidewall and bottom of the film was lower, and the sloped step coverage effect improved when the ICP power was increased, or the deposition pressure was decreased. The effects of RF power on the stress, density, and breakdown voltage of the SiO_2 films were also studied. Despite increased compressive stress with increasing RF power, the film stress was still low and within acceptable limits. The films deposited under optimized conditions showed improved densities in FTIR spectra, BOE rate, XRR, and breakdown voltage measurements, compared with the films deposited without applying RF power. The roughness of the film also decreased for the optimized condition.

The device performance was optimized for the preparation of the insulation layer in the JVS chip. This study is essential for increasing the number of junction layers in Josephson junction quantum voltage devices. The current number of junction stack layers is three. After further optimization, the number of junction layers is possible to increase to five. Because an increase in the number of junction layers depends on the optimization of the multistep process.

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