

Article

Designing Optically & Utilization of Thermopile Chip with Resonant Cavity Absorber Structure as IR Absorber

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Abstract: This paper presents a novel thermopile chip in which the resonant cavity structure was fully utilized as an absorber by an optical design. The resonant cavity absorber structure was designed using Al as the bottom reflective metal layer, air as the intermediate dielectric layer, and SiO₂/TiN/Si₃N₄ sandwich layers as the top absorption layer, while the bottom reflective metal (Al) was deposited on the cold junctions of the thermopile. The simulation and calculation results show that the thermopile chip with resonant cavity absorber structure not only has great infrared absorption in the wide infrared absorption range but also can effectively prevent the cold junctions from absorbing infrared radiation and inhibit the rise of temperature. As a result, the temperature difference between the hot junctions and the cold junctions is increased, and the responsivity of the thermopile chip is further improved. Moreover, the duty cycle of the thermopile chip is greatly improved due to the double-layer suspension structure. Compared with the traditional thermopile chip structure, the sizes of the thermopile chip with the resonant cavity absorber structure can be further reduced while maintaining responsivity and specific detectivity.

Keywords: infrared detector; resonant cavity; energy applications; absorptance



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1. Introduction

The thermopile IR detector is applied in many fields, because it has the advantages of no need for cooling and chopping, broad spectral response, low cost and simple output circuit [1–4]. The thermopile chip is the core component of thermopile IR detector and has been greatly optimized and has opened the door to mass production, with the help of conventional complementary metal oxide semiconductor (CMOS) and micro electromechanical system (MEMS) technologies. The thermopile chip is generally a central suspended structure with a supporting layer, thermopile, absorber, and other layers deposited on a silicon substrate. The hot junctions and the cold junctions of the thermopile are respectively distributed on the edge and center of the silicon substrate hollowed out in the center, and the hot junctions are covered by the absorber, as shown in Figure 1. The thermopile infrared detector contains two energy conversion processes of light-heat and heat-electricity, and its performance also depends on the superposition of the two conversions efficiency. Thus, the

absorber can play a crucial role on the thermopile chip. The absorber is required for great absorption at both 3–5 μm and 8–14 μm , while a thermopile chip is used as the sensing element of an infrared thermometer [5,6], nondispersive infrared (NDIR) gas detector [7,8] or infrared imager [9–11]. The porous materials with dendritic and soft structure, like gold-black, can have great absorption at ultra-wide wavelength range and are typically used as the absorber of thermopile chip [12–17]. However, these porous materials are generally too fragile and not compatible with CMOS [18,19]. Owing to the interference of light, the resonant cavity absorber structures can also have great absorption at a specific band and are also often used as the absorber of thermopile chips. However, the resonant absorption structure is a stack of multilayer films, so its absorption characteristics largely depend on the matching relationship between the refractive index and thickness of the multilayer film, and often only absorb specific wavelength bands. In addition, the resonant cavity absorption structure is often sensitive to thickness errors, and the thickness of each layer of the film needs to be accurately controlled during the preparation process. In fact, an Si_3N_4 layer or $\text{SiO}_2/\text{Si}_3\text{N}_4/\text{SiO}_2$ sandwich structure is also usually used as the absorber of thermopile chips. However, the Si_3N_4 layer or $\text{SiO}_2/\text{Si}_3\text{N}_4/\text{SiO}_2$ sandwich structure has higher absorption only at 8.5–13.5 μm and lower absorption at 2.5–8 μm [20,21].

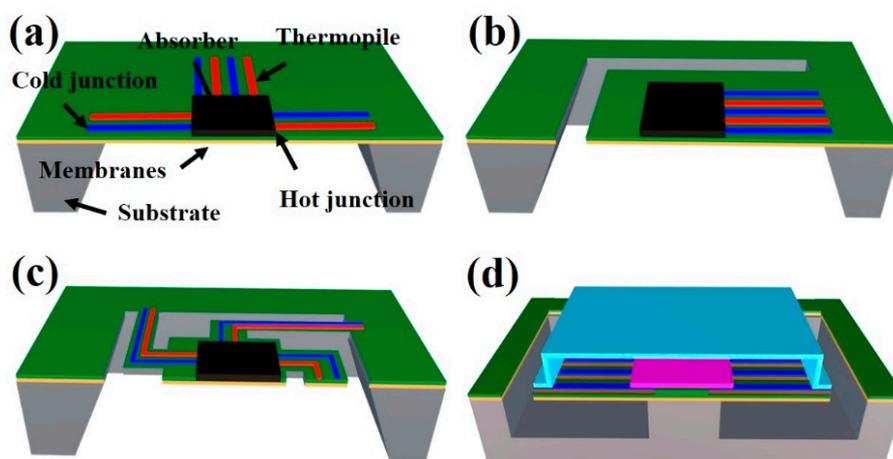


Figure 1. Typical thermopile chip structures: (a) close membrane structure, (b) cantilever beam structure (c) suspension bridge structure, and (d) the designed thermopile chip structure with resonant cavity.

The structures of thermopile chips are mainly divided into three types: close membrane structure, cantilever beam structure, and suspension bridge structure (Figure 1a–c) [22–25]. Compared to the cantilever beam and suspension bridge structures, the close membrane structure is the current mainstream structure of thermopile chip, which is provided with smaller thermal resistance, shorter response time, and a simpler manufacturing process. However, the above chip structures all have the problem of mutual restriction between the absorption zone and the thermocouple zone, and further reduction in thermopile chip size cannot maintain relatively higher responsivity and detectivity.

In this paper, we designed a novel thermopile chip in which the resonant cavity structure was fully utilized as an infrared absorber by an optical design (Figure 1d). In the resonant cavity absorber structure, the Al, air, and $\text{SiO}_2/\text{TiN}/\text{Si}_3\text{N}_4$ sandwich layers were used as the bottom reflective metal layer, intermediate dielectric layer and top absorption layer, respectively. The designed thermopile chip was proven to be provided with a high duty cycle, great infrared absorption, and a wide infrared absorption range.

2. Design of Resonant Cavity Absorber Structure

As shown in Figure 2a, the resonant cavity absorber structure generally consists of three parts: the top absorption metal layer, the middle dielectric layer, and the bottom

reflective metal layer [26,27]. The absorption characteristics of the resonant cavity absorber structure are based on the theory of optical interference absorption. The incident light and reflected light will produce light interference effects at the top absorption metal layer when the optical thickness of middle dielectric layer is of a quarter-wavelength thickness, thereby achieving higher infrared absorption at specific band. Thus, it is difficult for the resonant cavity absorber structure to achieve ultra-wide spectral absorption like the porous materials and to realize a detector in various fields such as gas detection and non-contact human temperature measurement. Moreover, the matching of each thin film, especially the thickness, has a great influence on the absorption characteristics of the resonant cavity absorber structure. Thus, the resonant cavity absorber structure generally requires a precise design of the absorption structure and control of the manufacturing process.

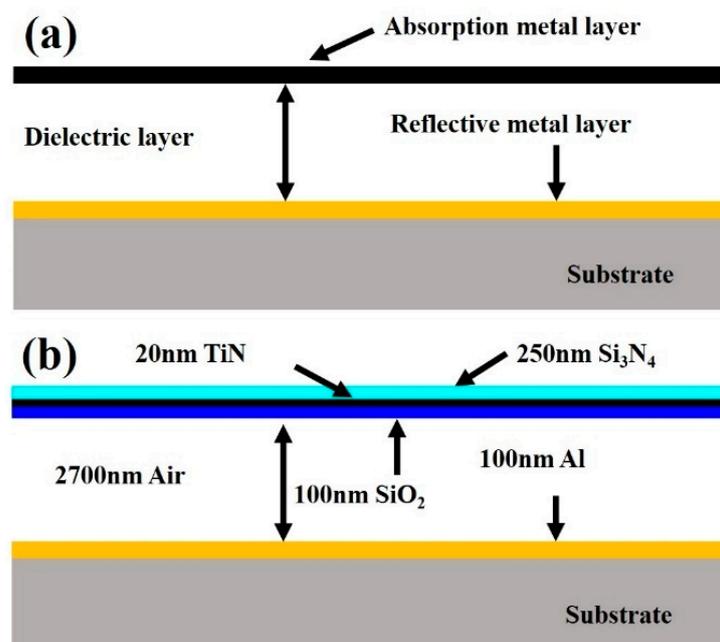


Figure 2. Schematics of (a) common and (b) the designed resonant cavity absorber structures.

The Essential Macleod is a simulation software for the transmission, reflection and absorption characteristics of optical multilayer films. In order to design a resonant cavity absorber structure with broad spectrum absorption and low film thickness error sensitivity, we first used the Essential Macleod to simulate and calculate the reflection and absorption characteristics of different materials based on the theory of optical interference absorption and then chose reasonable materials for each layer of the resonant cavity absorber structure, as shown in Figure 3. The simulation results show that the average reflectance of the Al layer could reach more than 97% at 2–14 μm . Thus, an Al layer was used as the bottom reflective metal layer of the resonant cavity absorber structure. According to the theory of optical interference absorption, It is easier to obtain a resonant cavity absorber structure with broad spectrum absorption with an intermediate dielectric layer with low refractive index [28]. The refractive index of air is 1, which is very suitable as the intermediate dielectric layer of the resonant cavity absorber structure. As seen in Figure 3, the Si₃N₄, SiO₂, and TiN have higher absorption at 3–14 μm , 8–10 μm , and 10–14 μm , respectively, which is why we chose the SiO₂/TiN/Si₃N₄ sandwich layers as the top absorption layer of the resonant cavity absorber structure. Moreover, the Si₃N₄ and SiO₂ layers are designed to be deposited on the upper and lower sides of TiN layer, respectively, where the Si₃N₄ layer can act as a passivation layer and have a certain protective effect on the TiN layer, and the SiO₂ layer can act as a supporting layer and play a positive role in supporting the overall structure. The SiO₂/TiN/Si₃N₄ sandwich layers as the top absorption layer can well reduce the difficulty of preparation and the sensitivity of the resonant cavity absorber

structure to the film thickness error and improve the mechanical strength, stability and yield of the resonant cavity absorber structure.

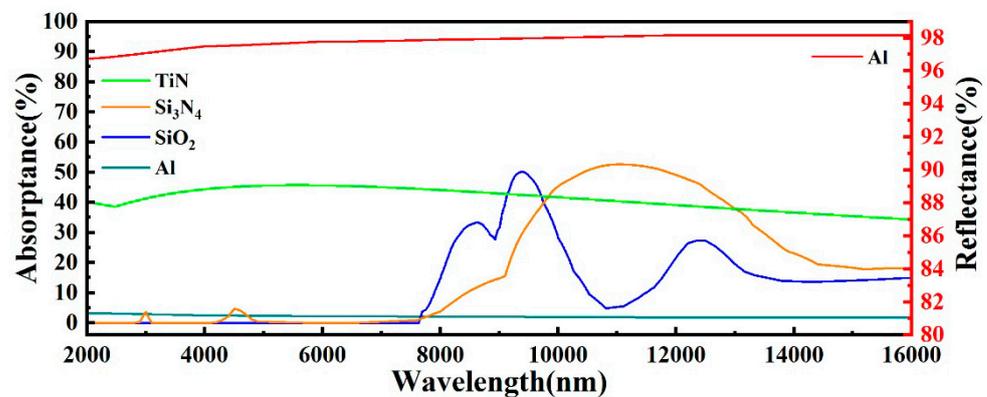


Figure 3. Calculated spectra of the TiN, Si₃N₄, SiO₂, and Al layers.

Based on the theory of optical interference absorption, we used the Essential Macleod to simulate and calculate the optical thicknesses of the intermediate dielectric layer and top absorption metal layer, thereby adjusting the absorption wavelength range of the structure, as shown in Figure 4. The simulation and calculation results show that the resonant cavity absorber structure has great absorption at 3–5 μm and 8–14 μm when the thicknesses of the air cavity, TiN layer and Si₃N₄ layer are 2700, 20, and 250 nm, respectively, as shown in Figure 2b. As shown in the red spectral curve in Figure 4a, the average absorbances of the designed resonant cavity absorber structure are ~89.56% and ~93.51% at 3–5 μm and 8–14 μm , respectively, which is comparable to those of porous materials [12–17]. However, as shown in the black spectral curve in Figure 4a, the conventional standard cavity absorption structure designed with Al as the bottom reflective metal layer, SiO₂ as the intermediate dielectric layer, and Ti as the top absorption layer only has an absorbance close to 91% in 3–5 μm [18]. Therefore, the thermopile chip with the designed resonant cavity absorber structure can not only be used as the detector elements of the non-contact infrared thermometer and thermal imager, but also as the NDIR gas detector element for detection of CO₂, CO, NO₂, and CH₄ gases. Generally, the absorption of the resonant cavity absorber structure is highly sensitive to the thickness error of each layer, and the thickness of each layer needs to be accurately controlled during the preparation process to achieve the ideal absorption effect. In fact, the deposition processes of MEMS and CMOS both have a certain thickness error, so the Essential Macleod software was used to simulate the absorption spectra of the designed resonant cavity absorber structure, under mean thickness error of 5%. As shown in Figure 4b, the absorption spectra of the designed resonant cavity absorber structure have no obvious deviation in absorbance compared with that of the theoretical design (Figure 4b). Thus, under the mean thickness error (5%) of the general MEMS and CMOS deposition processes, the designed resonant cavity absorber structure still has high absorption and stability. The structure design using air as the middle dielectric layer and SiO₂/TiN/Si₃N₄ sandwich layers as the top absorption layer can effectively broaden the absorption wavelength range and reduce the sensitivity to thickness error.

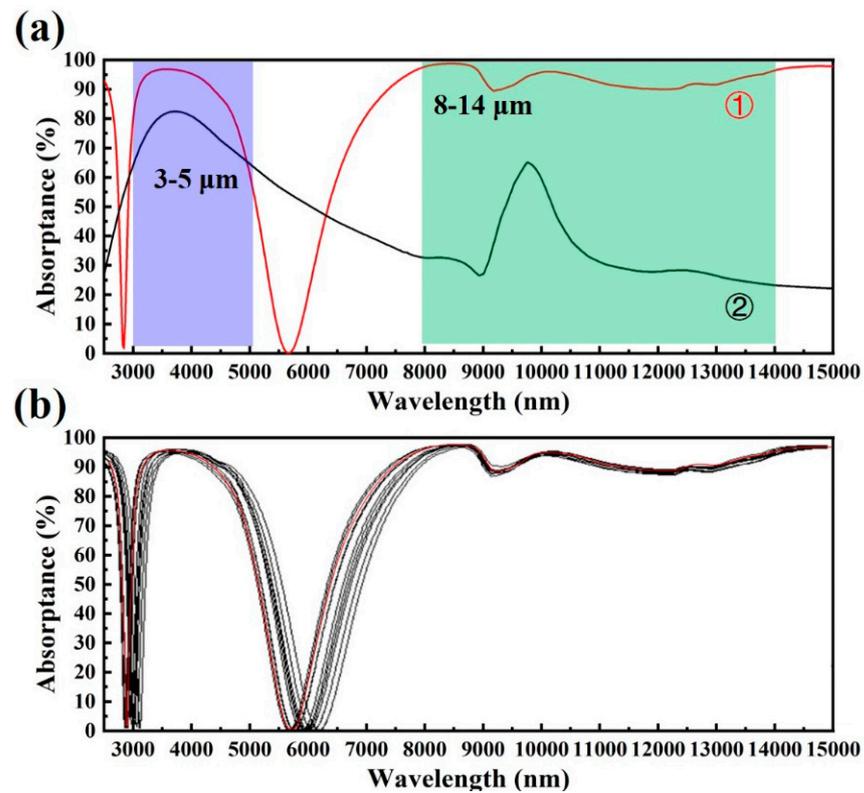


Figure 4. Theoretical absorption spectra of the designed resonant cavity absorber structures without (a) and (b) with mean thickness error of 5%.

3. Design of Thermopile Chip

Based on the designed resonant cavity absorber structure, we propose a new type of thermopile chip structure, as shown in Figure 5. In this paper, we adopted monocrystalline silicon as the substrate and N-/P-Poly-Si as the thermocouple. The SiO₂ layers were used as the support, insulating and passivation layers of the thermopile. The hot junctions of the thermopile were laid on the floating membrane, and the cold junctions were distributed on the center of substrate. Moreover, the N-Poly-Si and P-Poly-Si were connected using Al as interlayer at the hot junctions and the cold junctions of the thermopile, respectively.

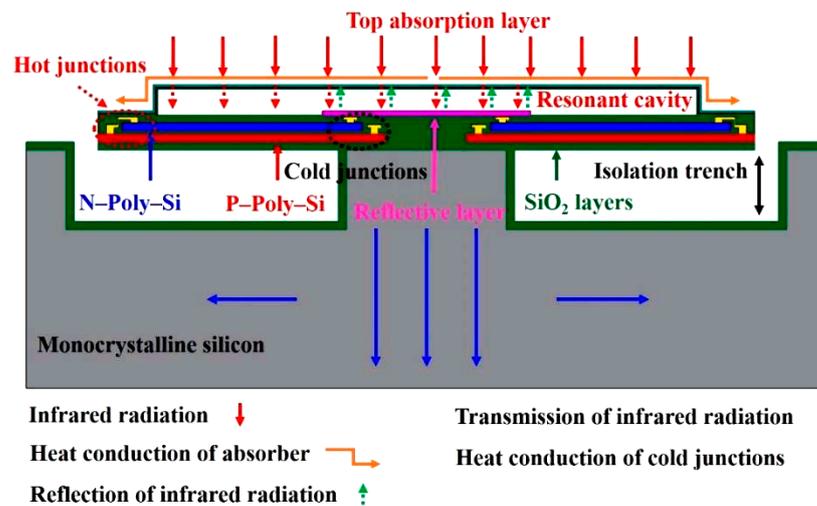


Figure 5. Schematics of structure and energy flow of thermopile chip with resonant cavity absorber structure.

The responsivity (R), noise equivalent power (NEP), specific detectivity (D^*), and time constant (T) are the main three performance parameters for evaluating the thermopile chip, and R is the most obvious and direct way to characterize the thermopile chip by the ratio of ΔU to incident infrared radiation power (P_0) and can be calculated from Equation (1) [3]:

$$R = \frac{\Delta U}{P_0}$$

When infrared radiation is applied to the thermopile chip, there will be a temperature difference (T_{diff}) between the hot junctions and the cold junctions of the thermopile, and T_{diff} is converted into a measurable output voltage (ΔU) based on the Seebeck effect. The ΔU for a thermopile is then calculated from Equation (2) [3]:

$$\Delta U = NT_{diff}|\alpha_A - \alpha_B| = NT_{diff}\alpha_{AB}$$

Therefore, increasing the T_{diff} between the hot junctions and the cold junctions of the thermopile is the most direct and effective way to improve the performance of the thermopile chip.

In order to better understand and design the structure of the thermopile chip and make the designed resonant cavity absorber structure be perfectly combined with the thermopile chip, we used the finite element analysis software to simulate the thermopile chip's thermal field. As shown in Figure 6, compared with other double-layer suspension thermopile chips, the thermopile chip we designed has a higher T_{diff} between the hot junctions and the cold junctions [29–31]. Since both the doped polysilicon and SiO_2 layers have certain absorption characteristic of infrared radiation, the cold junctions of the thermopile also have infrared absorption characteristic [20,21]. When the infrared radiation is irradiated on the surface of the thermopile chip, the cold junctions will also perform infrared absorption and light-to-heat conversion except the hot junctions and the infrared absorber. As shown in Figure 6a, the absorption of infrared radiation by the cold junctions will increase the temperature of the cold junction and thus weaken the responsivity of the thermopile chip. To solve this problem, we designed the cold junctions of the thermopile specifically, that is, the bottom reflective metal layer (Al) of the resonant cavity absorber structure was deposited on the cold junctions of the thermopile. Figure 3 shows that the Al layer has very low absorptance and very high reflectance (~97%) at 2–14 μm so that the Al layer can well reflect the infrared radiation irradiated on the cold junctions, prevent the cold junctions from absorbing infrared radiation, and inhibit the rise of temperature, resulting in further improvement of responsivity and specific detectivity (as shown in Figure 6b). Furthermore, the Al layer can also serve as the reflective metal layer of the resonant cavity absorber structure, forming the interference of light and strengthening the infrared absorption characteristic of the top absorption metal layer. The top absorption layer of the resonant cavity absorber structure can be connected to the hot junctions through the support column, which facilitates the transfer of the heat of the top absorption layer to the hot junctions as shown in Figure 6b. This can further increase the temperature difference between the hot junctions and the cold junctions, and reduce the response time of the thermopile chip. In particular, the intermediate dielectric layer (air) is located between the absorption layer and the thermopile, and as a result, the heat loss is reduced, and furthermore, the mutual restriction of area between the absorption zone and the thermocouple zone is also solved, leading to a very high duty cycle. Thus, the sizes of the designed thermopile chip can be further reduced while maintaining responsivity and specific detectivity compared with the three types of traditional thermopile chips.

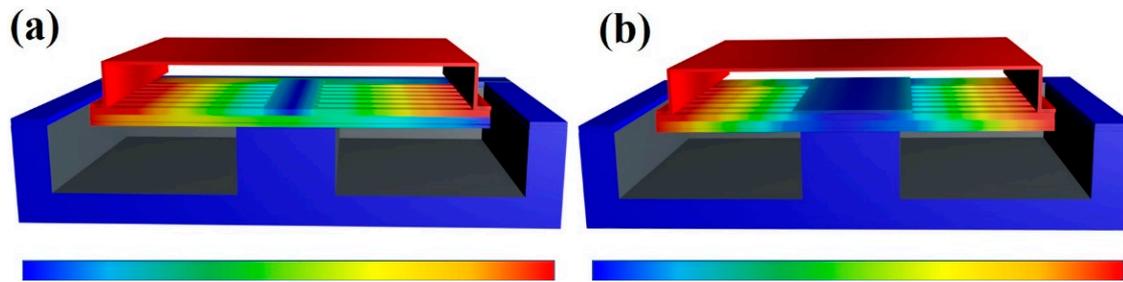


Figure 6. The (a) standard and (b) our design double suspension structures thermal field simulation.

4. Preparation Process of Thermopile Chip

On the basis of the designed structure of the thermopile chip, the preparation process was proposed, combining CMOS and MEMS processes. Firstly, an SiO₂ layer of ~200 nm thick was deposited on the surface of the silicon substrate as a masking layer using a thermal oxidation process, and then the photolithography and reactive ion etching (RIE) processes were used to pattern and etch the SiO₂ layer (Figure 7a). Secondly, the isolation trench with depth of 6000 nm was obtained by the RIE process for the bare silicon substrate (Figure 7b). Thirdly, a thermal oxidation process was used again to generate an SiO₂ layer of ~200 nm thick on the etched silicon substrate as a release barrier (Figure 7c). Then, a polysilicon layer of ~3000 nm thick was grown by low pressure chemical vapor deposition (LPCVD) and then planarized, which served as a sacrificial release layer (Figure 7d). An SiO₂ layer of ~500 nm thick was deposited by LPCVD on the polysilicon layer, which served as a thermopile support layer (Figure 7e). A polysilicon layer of ~500 nm thick was deposited by LPCVD on the support layer as one layer of the thermocouple and doped with boron (B) by ion implantation to form P-type polysilicon, and then the P-type polysilicon was patterned by the RIE process (Figure 7f). Next, an SiO₂ layer of ~100 nm thick was deposited again by LPCVD as the insulating layer of the P-type polysilicon layer (Figure 7g). A polysilicon layer of ~500 nm thick was deposited by LPCVD on the insulating layer as another layer of the thermocouple and doped with phosphorus (P) by ion implantation to form N-type polysilicon, and then the N-type polysilicon was patterned by the RIE process (Figure 7h). An SiO₂ layer of ~100 nm thick was deposited by LPCVD as the insulating layer of the N-type polysilicon layer (Figure 7i). Subsequently, the two insulating layers were etched to form the connection holes at the hot junctions and the cold junctions by the RIE process (Figure 7j). Then, an Al layer of ~500 nm thick was deposited by magnetron sputtering technology (MST) and patterned and etched by the photolithography and RIE processes, which served as the electrical connection between the thermocouples and the electrode (Figure 7k). The withstanding temperature of the substrate was greater than 700 °C while employing LPCVD to deposit the SiO₂ or Si₃N₄ layer, which brought about serious damage to the deposited Al layer. Finally, the SiO₂ layer of ~100 nm thick, as the passivation layer of the thermopile, was deposited by plasma enhanced chemical vapor deposition (PECVD) (Figure 7l).

For the preparation of the resonant cavity absorber structure, an Al layer of ~100 nm thick was first deposited by MST as the bottom reflective metal layer, and then the photolithography and RIE processes were used to pattern and etch the Al layer (Figure 8a). The un-etched Al layer covered the cold junctions of the thermopile, which not only served as the reflective metal layer but also could reflect the infrared radiation irradiated at the cold junctions. Then, an amorphous silicon layer of ~2700 nm thick was deposited by PECVD as the sacrificial layer (Figure 8b). Subsequently, an SiO₂ layer of ~100 nm thick was deposited by PECVD as the support layer of the top absorption metal layer; next, a TiN layer of ~20 nm thick was deposited by MST as the top absorption metal layer, and then an Si₃N₄ layer of ~250 nm thick was deposited by PECVD as the passivation layer of the top absorption metal layer, thereby forming a complete SiO₂/TiN/Si₃N₄ resonant cavity absorber structure (Figure 8c). Finally, the sacrificial layer composed of amorphous

silicon was dry-etched and released by the release hole etching and XeF₂ gas phase release processes to form the thermopile chip with the resonant cavity absorber structure (Figure 8d).

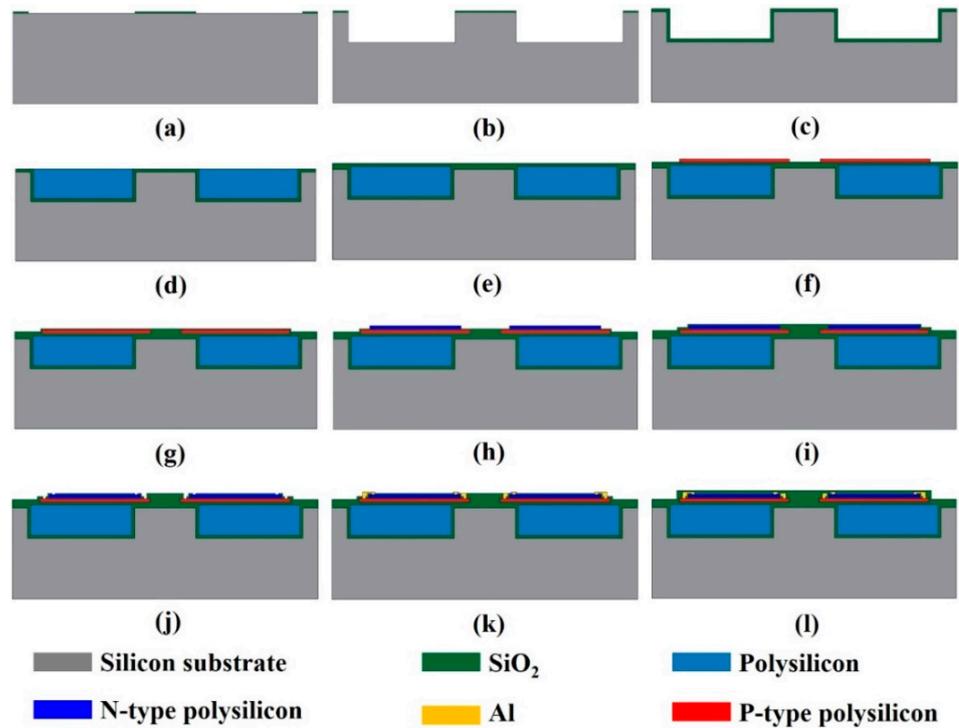


Figure 7. Schematic of preparation process of the designed thermopile. (a) deposition of SiO₂ layer of 200 nm thickness, (b) isolation trench with depth of 6000 nm, (c) thermal oxidation, (d) developing sacrificial release layer, (e) 500 nm thick thermopile support layer, (f) 500 nm thick polysilicon layer RIE process, (g) insulating layer, (h) polysilicon layer, (i) 100 nm insulating layer, (j) formation of connection holes, (k) 500 nm thick Al layer and (l) 100 nm thick SiO₂ layer.

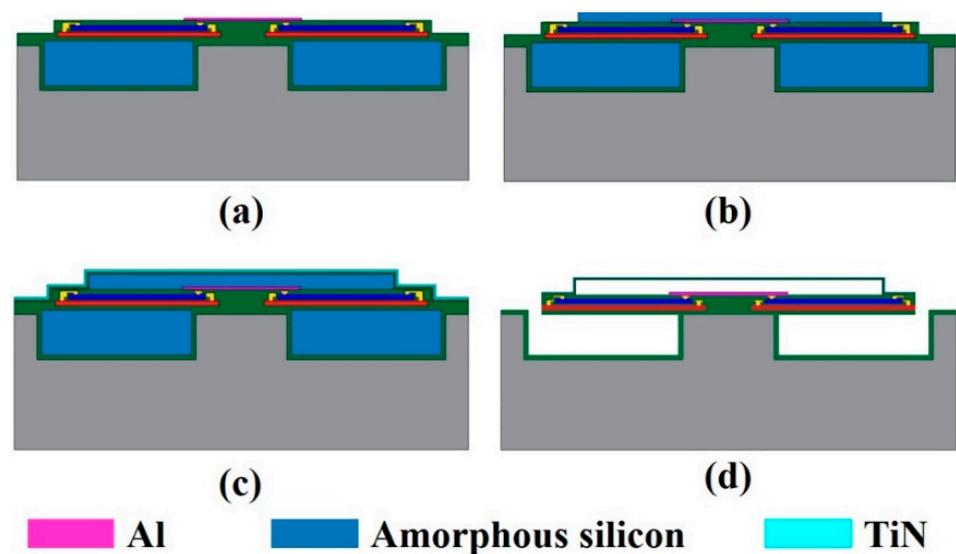


Figure 8. Schematic of preparation process of the designed resonant cavity absorber structure. (a) 100 nm thick bottom reflective metal layer, (b) 2700 nm thick amorphous silicon layer, (c) resonant cavity absorber structure, (d) final thermopile chip.

5. Conclusions

A novel thermopile chip with resonant cavity absorber structure was designed by an optical simulation in this work. In the resonant cavity absorber structure, the Al, air, and SiO₂/TiN/Si₃N₄ sandwich layers were innovatively used as the bottom reflective metal layer, intermediate dielectric layer, and top absorption layer, respectively. The designed resonant cavity absorber structure exhibited ~89.56% and ~93.51% average absorptances at 3–5 μm and 8–14 μm, respectively. In particular, the bottom reflective metal layer (Al) was deposited on the cold junctions of the thermopile, which made the Al layer not only act as the reflective metal layer to reflect the infrared radiation and to form the resonant cavity absorber structure, but also prevented the cold junctions from absorbing infrared radiation and inhibiting the rise of temperature. As a result, the temperature difference between the hot junctions and the cold junctions was increased, and the responsivity of the thermopile chip was improved. Moreover, the duty cycle of the thermopile chip was greatly improved due to the double-layer suspension structure. Compared with the traditional thermopile chips, the sizes of the designed thermopile chip can be further reduced while maintaining responsivity and specific detectivity.

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Data Availability Statement: Data are available in the paper.

Conflicts of Interest: The authors declare no conflict of interest.

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