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Numerical Insights into the Influence of Electrical Properties of n-CdS Buffer Layer on the Performance of SLG/Mo/p-Absorber/n-CdS/n-ZnO/Ag Configured Thin Film Photovoltaic Devices

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Abstract: A CdS thin film buffer layer has been widely used as conventional n-type heterojunction partner both in established and emerging thin film photovoltaic devices. In this study, we perform numerical simulation to elucidate the influence of electrical properties of the CdS buffer layer, essentially in terms of carrier mobility and carrier concentration on the performance of SLG/Mo/p-Absorber/n-CdS/n-ZnO/Ag configured thin film photovoltaic devices, by using the Solar Cell Capacitance Simulator (SCAPS-1D). A wide range of p-type absorber layers with a band gap from 0.9 to 1.7 eV and electron affinity from 3.7 to 4.7 eV have been considered in this simulation study. For an ideal absorber layer (no defect), the carrier mobility and carrier concentration of CdS buffer layer do not significantly alter the maximum attainable efficiency. Generally, it was revealed that for an absorber layer with a conduction band offset (CBO) that is more than 0.3 eV, J_{sc} is strongly dependent on the carrier mobility and carrier concentration of the CdS buffer layer, whereas V_{oc} is predominantly dependent on the back contact barrier height. However, as the bulk defect density of the absorber layer is increased from 10^{14} to 10^{18} cm^{-3} , a CdS buffer layer with higher carrier mobility and carrier concentration is an imperative requirement to a yield device with higher conversion efficiency and a larger band gap-CBO window for realization of a functional device. Most tellingly, simulation outcomes from this study reveal that electrical properties of the CdS buffer layer play a decisive role in determining the progress of emerging p-type photo-absorber layer materials, particularly during the embryonic device development stage.

Keywords: CdS; buffer layer; carrier mobility; carrier concentration; SCAPS-1D; photovoltaic

1. Introduction

The conversion of solar energy into usable electricity via a solid-state pn-junction based photovoltaic (PV) device holds immense opportunities in the quest to reduce our present dependence on fossil fuels and subsequently lower the detrimental greenhouse gases emissions [1,2]. Currently, global PV installations are comprised of monocrystalline silicon (c-Si), multicrystalline silicon (mc-Si) and thin film technologies [3]. Thin film photovoltaics can be further divided into 3 successfully commercialized technologies, which are copper

indium gallium diselenide (CIGS), cadmium telluride (CdTe) and amorphous silicon (a-Si). Among these, CIGS and CdTe have garnered tremendous interest in the PV research community, which eventually translated into systematic theoretical and experimental studies and consequently achieved a power conversion efficiency (PCE) of more than 22% [4]. However, the scarcity of indium (In) and tellurium (Te) is predicted to hamper the future adoption of CIGS and CdTe at a multi-terawatt level scale [5,6]. Therefore, various earth-abundant, low cost and pure sulfide-based materials such as $\text{Cu}_2\text{ZnSnS}_4$ (CZTS), Cu_2SnS_3 (CTS), FeS_2 and SnS are being rigorously experimented with as for plausible next generation thin film technologies [7–14]. These aforementioned photo-absorber materials are often adopted in the well-established Mo/absorber/CdS/ZnO substrate type device configuration that was developed by ARCO back in 1988, which was one of the key innovations that catalyzed the development of high efficiency CIGS solar cells [15].

Cadmium sulfide (CdS) is an important II–VI compound semiconductor, with high transparency, direct band gap transition ($E_g \sim 2.4$ eV), high electron affinity (4.2 eV) and n-type conductivity [16,17]. CdS also improves the lattice heterojunction interface match, enhances the excess carrier lifetime and optimizes the band alignment of the devices it is used in [18]. CdS thin film deposition can be done by using various methods, such as magnetron sputtering, chemical vapor transport (CSVT), chemical bath deposition (CBD) and thermal evaporation [19–21]. Most of the techniques are very complex and hard to control, and also costly [22]. CBD has been considered as one of the most common fabrication techniques to deposit a buffer layer in solar cells due to its simple deposition process, low costs, high yield and eco-friendliness [23]. Besides, this process can be controlled easily through pH, salt concentration and temperature variations, thereby obtaining a high quality thin film with the desired thickness and crystallinity [7,21]. Different materials with a wider band gap and non-toxic materials such as ZnS (O,OH) and ZnS have also been investigated as a potential buffer layer for thin film solar cells [24–27].

However, these buffer layers suffer from complicated reaction mechanism and light soaking effects, presenting potential cell durability and reproducibility issues [28]. Knowledge of the optical, electrical and structural characteristics of CdS films is significant in many scientific, technological and industrial applications in the field of optoelectronic devices, especially involving solar cells [23]. Despite comprehensive data on CBD films of CdS in the literature, the optoelectronic properties of these films are not well understood yet. This is because the optoelectrical properties are, to some extent, influenced by the film microstructure, which in turn depends on the preparation and post-deposition conditions. Interestingly, the electrical resistivity of the CdS thin film which essentially depends on the carrier concentration and carrier mobility, has been reported to differ by several orders of magnitude, due not only to the doping level, but also to the film microstructure and thickness [29–31]. However, systematic studies using numerical simulation on the effects of the carrier mobility and carrier concentration of CdS buffer layer and thus its electrical properties, on the performance of thin film solar cells have not been carried out so far.

Hence, in this study, we have intentionally focused the scope of our numerical simulation by using 1D-SCAPS software to elucidate the interdependence of carrier mobility and carrier concentration of the CdS buffer layer on the PCE of various substrate-type thin film solar cells. A generic substrate-type Soda lime glass (SLG)/Mo/p-absorber/n-CdS/n-ZnO/Ag device configuration has been adopted. In order to maximize the applicability of simulation outcomes, all the possible permutations and combinations of absorber band gap from 0.9 to 1.7 eV and electron affinity from 3.7 to 4.7 eV have been considered. Furthermore, absorber layers with no defect (ideal) and with a peak defect density of 10^{14} cm^{-2} (low), 10^{16} cm^{-2} (medium) and 10^{18} cm^{-2} (high) have also been considered with variations in the carrier mobility and carrier concentration of the CdS buffer layer. The fundamental aim of this study is to accentuate the importance of having a high quality CdS buffer layer (from a electrical property point of view, focusing on high carrier mobility and a high carrier concentration), during the initial development period of a novel photo-absorber

material, particularly in substrate-type thin film photovoltaic device configurations that are akin to CIGS technology.

2. Materials and Methods

In this numerical simulation study, SCAPS-1D (version 3.3.07) software has been utilized to simulate the effects of variable carrier mobility and carrier concentration of the CdS buffer layer on the overall performance of substrate-type thin film photovoltaic devices. SCAPS-1D is a one dimensional computer program used to simulate the DC and AC electrical characteristics of thin film heterojunction solar cells, which was developed and constantly updated by a research team led by Marc Burgelman at the University of Gent [32]. The modeling capabilities of SCAPS were specifically designed to mimic the characteristics of CIGS and CdTe thin film solar cells; however, it has also been tested and used for a variety of other cell types. The generic device structure which has been adopted in this study and subsequently modeled in SCAPS is as shown in Figure 1 below. Tables 1–4 show the list of physical and electronic material properties of all layers, which have been adopted and modeled in the SCAPS simulation tool in the study. A brief literature from the material property perspective for each layers and pertinent theoretical framework is given in the subsequent paragraphs, with the aim to derive a credible justification for the selection of material and hetero-interface electronic parameters which have been used in this study, as shown in Tables 1–4.

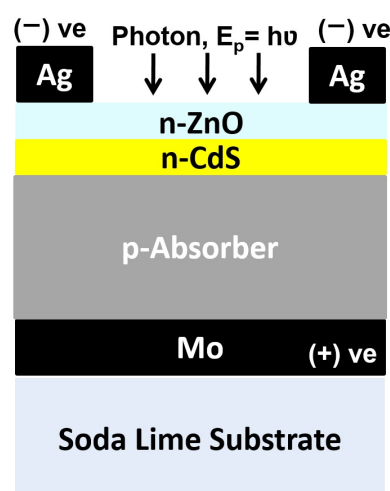


Figure 1. Substrate-type thin film device configuration.

Table 1. List of physical and electronic properties for interface parameters.

Interface Parameters	Front	-	Back
Metal work function (eV)	4.47 (Ag)	-	4.95 (Mo)
Majority carrier barrier height Φ_b (eV)	$\Phi_{bn} = 0$	-	$\Phi_{bp} = E_{g\text{-Absorber}} - \Phi_{bn}$
Electron surface recombination Velocity, S_e ($\text{cm}\cdot\text{s}^{-1}$)	10^7	-	10^7
Hole surface recombination Velocity, S_h ($\text{cm}\cdot\text{s}^{-1}$)	10^7	-	10^7
Reflectivity	0.05	-	0.80

Table 2. List of physical and electronic properties for layer parameters.

Layer Parameters	n-ZnO	n-CdS	p-Absorber
Layer thickness (nm)	50	50	2500
Dielectric constant, ϵ_r	9	10	13.6
Electron mobility, μ_n (cm ² /V.s)	100	~	100
Hole mobility, μ_p (cm ² /V.s)	25	~	25
Acceptor concentration, N_A (cm ⁻³)	0	0	1×10^{16}
Donor concentration, N_D (cm ⁻³)	1×10^{18}	~	0
Band gap, E_g (eV)	3.3	2.4	0.9–1.7
Electron affinity, χ (eV)	4.4	4.2	3.7–4.7
Effective density of states in Conduction band, N_C (cm ⁻³)	2.2×10^{18}	2.2×10^{18}	2.2×10^{18}
Effective density of states in Valence band, N_V (cm ⁻³)	1.8×10^{19}	1.8×10^{19}	1.8×10^{19}
Electron thermal velocity (cm s ⁻¹)	1×10^7	1×10^7	1×10^7
Hole thermal velocity (cm s ⁻¹)	1×10^7	1×10^7	1×10^7

~Please see Table 3.

Table 3. Classification of electrical properties of the CdS buffer layer.

Parameters	Set A	Set B	Set C	Set D
Donor concentration, N_D (cm ⁻³)	1×10^{14}	1×10^{14}	1×10^{18}	1×10^{18}
Electron mobility, μ_n (cm ² /V.s)	1	100	1	100
Hole mobility, μ_p (cm ² /V.s)	0.25	25	0.25	25
Electrical resistivity ($\Omega \cdot \text{cm}$)	62,415	624.15	6.2415	0.0624

Table 4. Defect properties of all layers used in this study.

Layer Parameters	n-ZnO	n-CdS	p-Absorber
Defect Type	Neutral	Neutral	Neutral
Electron capture cross section (cm ²)	10^{-12}	10^{-13}	10^{-15}
Hole capture cross section (cm ²)	10^{-12}	10^{-13}	10^{-13}
Energetic distribution	GauSS	GauSS	GauSS
Reference for defect energy level E_t	Above E_v	Above E_v	Above E_v
Energy level with respect to reference (eV)	1.650	1.200	$(0.6/1.1) \times E_{g\text{-Absorber}}$
Characteristic energy (eV)	0.100	0.100	0.100
Total defect density, $N_{T\text{-total}}$ (cm ⁻³)	1.772×10^{16}	1.772×10^{17}	$0\text{--}1.772 \times 10^{17}$
Peak defect density $N_{T\text{-peak}}$ (eV ⁻¹ ·cm ⁻³)	1×10^{17}	1×10^{18}	$0\text{--}1 \times 10^{18}$

The effects of the SLG substrate on the heterojunction band energy layout was not taken into consideration in the simulation due to the limitations posed by the SCAPS software used in this study. Nonetheless, in reality, diffusion of sodium (Na) from soda lime glass into the absorber layer has been well-documented as one of the adventitious doping mechanisms, which promotes grain growth and elemental interdiffusion and also enhances carrier concentration and defect passivation for several types of photo-absorber

materials such as CIGS, CZTS, CTS, FeS₂ and SnS [33–37]. Conventionally, in a substrate-type device architecture, molybdenum (Mo) thin film is the primary choice as a back contact due to its chemical inertness, good thermal stability and suitable electrical and optical (reflectivity) properties [38,39]. The work function of the Mo back contact was set to 4.95 eV [40]. Consequently, the majority carrier barrier height at the Mo/absorber interface changed for different values of the band gap and electron affinity of the absorber layer in accordance with Equation (1) below [41]:

$$\Phi_{Bp} = E_g - \Phi_{Bn} \quad (1)$$

where E_g is the absorber layer band gap and Φ_{Bn} is the minority carrier barrier height, which on the other hand is given by Equation (2) as shown below [40].

$$\Phi_{Bn} = \Phi_{Mo} - \chi_s \quad (2)$$

Φ_{Mo} is the Mo metal work function and χ_s is the electron affinity of the absorber layer. Absorber layer thickness was fixed at 2500 nm throughout the entire simulation. The band gap and electron affinity values of the absorber layer were simultaneously varied from 0.9 to 1.7 eV and from 3.7 to 4.7 eV, respectively. Consequently, the corresponding conduction band offset (CBO) (with respect to CdS buffer layer, $\chi_{CdS} = 4.2$ eV), ΔE_c changed accordingly based on Equation (3), as given below [42]:

$$\Delta E_c = \chi_{\text{absorber}} - \chi_{CdS}; \text{ for } n - \text{CdS}/p - \text{absorber heterojunction} \quad (3)$$

where χ_{absorber} and χ_{CdS} are the electron affinity values for the p-absorber layer and n-CdS buffer layer, respectively. With the above-mentioned CBO definition, the following sign convention was established. In a positive CBO ($\chi_{\text{absorber}} > \chi_{CdS}$) or also known as a spike-like CBO, photogenerated electrons have to utilize kinetic energy in order to overcome an energy barrier in the absorber/buffer hetero-interface. Meanwhile in a negative CBO ($\chi_{\text{absorber}} < \chi_{CdS}$) or also termed as a cliff-like CBO, photogenerated electrons gain kinetic energy at this absorber/buffer hetero-interface [43]. This permutation and combination approach has enabled a wide range of performance plot for various known absorber materials, which are currently being experimentally investigated at a lab-scale. A few material systems are identified and tabulated with their band gap, electron affinity and the computed CBO values (with the respect to CdS buffer layer) in Table 5.

Table 5. Band gap, electron affinity and the resulting conduction band offset (CBO) values calculated using Equation (3) for a few shortlisted newly emerging and established absorber material.

Absorber Material	Band Gap, E_g (eV)	Electron Affinity, χ (eV)	CBO, ΔE_c (eV)	Reference for the Reported E_g and χ Values
CIGS	1.15	4.5	0.3	[44]
CdTe	1.5	3.9	−0.3	[45]
CZTS	1.5	4.5	0.3	[46]
CZTSe	1.05	4.54	0.34	[47]
CTS	0.95	4.77	0.57	[48]
SnS	1.1	3.52	−0.68	[49]
FeS ₂	0.95	4.71	0.51	[50]
Sb ₂ S ₃	1.76	4.7	0.50	[51]

Moving on to the central theme of this simulation study, which is the electrical properties of CdS buffer layer, Table 3 shows the 4 different scenarios investigated in this present study. Donor concentration and carrier mobility are varied according to the values given in

the Table 4, consequently the electrical resistivity of CdS buffer layer changes according to Equation (4) as described below [52]:

$$\rho = \frac{1}{q\mu_n N_D} \quad (4)$$

where ρ is the resistivity, q is the electron's charge, while μ_n and N_D is the electron mobility and donor concentration of CdS buffer layer. Basically, the following key features can be deduced from Table 3: Set A and B represents the CdS buffer layer with a lower carrier concentration ($1 \times 10^{14} \text{ cm}^{-3}$) and varying electron mobility (set A: $1 \text{ cm}^2/\text{V}\cdot\text{s}$, set B: $100 \text{ cm}^2/\text{V}\cdot\text{s}$). On the other hand, set C and D represents a CdS buffer layer with a higher carrier concentration ($1 \times 10^{18} \text{ cm}^{-3}$) and varying electron mobility (set C: $1 \text{ cm}^2/\text{V}\cdot\text{s}$, set D: $100 \text{ cm}^2/\text{V}\cdot\text{s}$). As a result, the CdS buffer layer in set A possesses the highest electrical resistivity of $62,415 \text{ }\Omega\cdot\text{cm}$, and this value progressively decreases for set B ($624.15 \text{ }\Omega\cdot\text{cm}$) and set C ($6.2415 \text{ }\Omega\cdot\text{cm}$), whereas the CdS buffer layer in set D possesses the lowest electrical resistivity of $0.0624 \text{ }\Omega\cdot\text{cm}$. Another material property of the absorber layer which was intentionally varied is the defect density. In the first part of this simulation, an ideal absorber layer was assumed, hence the peak defect density of the absorber layer was set to 0 for all cases. In the second part of the simulation, 3 distinct peak defect densities of the absorber layer were assumed; 1×10^{14} , 1×10^{16} and $1 \times 10^{18} \text{ eV}^{-1}\cdot\text{cm}^{-3}$, respectively. No CdS/absorber interfacial recombination mechanism was implemented in this study. On the other hand, the defect properties of other layers were kept constant. Table 4 summarizes the defect properties for all the relevant layers adopted in this study. The thickness of the CdS buffer layer was kept constant at 50 nm in all cases [53]. A 50 nm thick n-ZnO layer was incorporated as a transparent conducting oxide (TCO) layer on the top CdS buffer layer and was followed by a front contact metal electrode (Ag front electrode). In order to enable ohmic contact between the front electrode and a n-ZnO TCO layer, the work function of the Ag front electrode was set to 4.47 eV. Ag has been reported to possess work functions in the range of 4.26 to 4.74 eV depending on the crystal facet orientation [54]. In other words, a flat-band condition ($\Phi_{bn} = 0$) was assumed in the front Ag/n-ZnO metal-semiconductor junction. All numerical simulations were carried out at a constant temperature of 300 K for all cases. No additional series resistance and shunt resistance parameters were defined for simplicity. Built-in standard solar spectrum (AM1.5G-1 Sun) with an integrated power density of 1000 W/m^2 was chosen as an illumination bias.

The numerical work presented herein has been carried out in two parts. In the first part, an ideal absorber layer with no defect was assumed and all 4 types of CdS buffer layer (Set A, B, C and D) were considered in the simulation. The outcome and discussion pertaining the first part is delineated in Section 3.2. The second part of this simulation takes into account the absorber layer with its defect density. As mentioned previously, 3 distinct peak defect densities of the absorber layer were assumed, which are $1 \times 10^{14} \text{ eV}^{-1}\cdot\text{cm}^{-3}$ (low), $1 \times 10^{16} \text{ eV}^{-1}\cdot\text{cm}^{-3}$ (medium) and $1 \times 10^{18} \text{ eV}^{-1}\cdot\text{cm}^{-3}$ (high). In the second part, only the CdS buffer layers represented in set A and set D, which corresponds to buffer layers with the lowest and highest resistivity, respectively, were considered. The outcome and discussion pertaining the second part is described in Section 3.3.

3. Results and Discussion

3.1. Interfacial Electronic Parameters of Mo/p-Absorber/n-CdS Heterostructure

Although the primary focus of this study was aimed at elucidating the effects of the electrical properties of the CdS buffer layer on the performance of a thin film photovoltaic device, one aspect of this simulation study that must be explicated prior to delving into the aforementioned scope is the back contact barrier height (Φ_{Bp}). This is due to the fact that the back contact barrier height, which is an important interfacial electronic parameter at the Mo/p-absorber metal-semiconductor interface changes with the band gap and electron affinity of the p-absorber layer, as described in Equations (1) and (2). Figure 2 below depicts

the resulting back contact barrier height as a function of the band gap and electron affinity of the absorber layer.

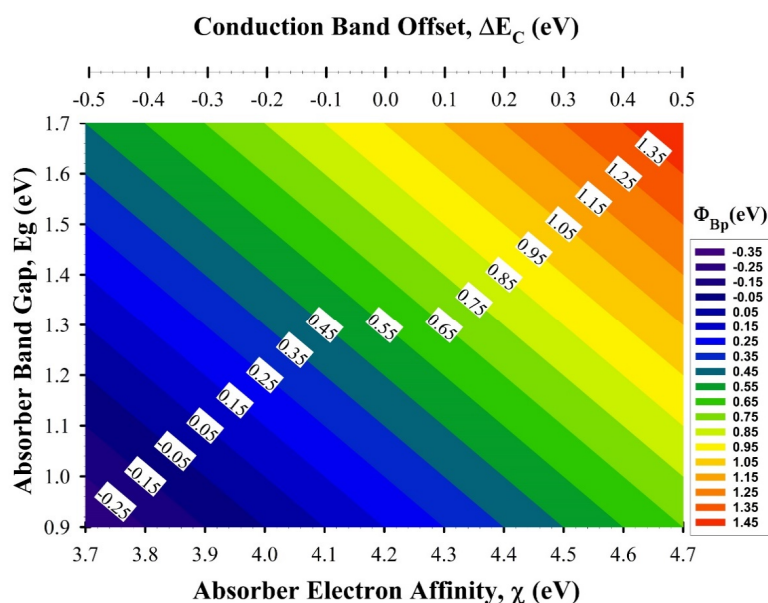


Figure 2. Back contact barrier height (Φ_{Bp}) as a function of band gap and electron affinity (top x -axis correlates with the resulting CBO values) of the absorber layer.

The top x -axis represents the CBO values for the corresponding electron affinity of the absorber layer given in the bottom x -axis, which is in accordance with Equation (3). Negative and zero back contact barrier height denotes ohmic contact between Mo and the p-absorber layer, while a positive value represents a rectifying contact. In an optimal photovoltaic device, ohmic contact is preferred, which is defined as contact that allows unimpeded flow of the hole through diffusion from the valence band of the p-absorber layer into the partially filled band of metal. An ohmic metal–semiconductor contact generally exhibits linear current–voltage characteristics in both biasing directions ($-V$ to $+V$) [55]. On the other hand, a rectifying contact or also known as a Schottky contact is less favorable due to the existence of a potential barrier which retards the hole diffusion from the p-absorber into the back contact metal. Therefore, referring to Figure 2, it can be deduced that an absorber layer with an electron affinity of 3.7 to 4.0 eV and a band gap of 0.9 to 1.2 eV (bottom-left corner of the plot), forms an ohmic contact with the Mo back contact. Concomitantly, the absorber layer within this range forms a cliff-like CBO of -0.50 to -0.20 eV with the CdS buffer layer. Meanwhile, the rest of the potential absorber material which fall outside the aforementioned electron affinity and band gap region was projected to form a Schottky contact with Mo metal.

There are 2 essential characteristics pertaining to the resulting back contact barrier height values, which have significant impacts on the applicability of this simulation work. Firstly, in this simulation, no interfacial layer between the Mo back contact and p-absorber layer was assumed, hence Figure 2 represents the theoretical values of a back contact barrier height. In reality, interaction of chalcogen atoms such as S and Se with Mo back contact during layer deposition and heat treatment is known to induce an unintentional interfacial layer [56,57]. This interfacial layer substantially alters the charge transport at the Mo/p-absorber interface. For instance, in theory, a CIGSe absorber layer is supposed to form a Schottky contact with Mo due to its large work function; however, the formation of an advantageous p-MoSe₂ interfacial layer warrants ohmic contact and subsequently promotes photogenerated charge collection at the back contact region [58,59]. On the other hand, in CZTS based devices, a n-MoS₂ interfacial layer has been recognized as a detrimental component which is responsible for higher series resistance, thus leading to

lower conversion efficiency [60,61]. The central reason for not including an interfacial layer in this simulation approach is essentially due to the non-specificity of absorber layer material, thus rendering any inclusion interfacial layer to be speculative in nature. Secondly, we were well aware that by masking the effects of back contact barrier height with a flat-band option ($\Phi_{Bp} = 0$) for the entire range of the absorber layer, this in turn, affects the electrical properties of the CdS buffer layers on the performance of the thin film photovoltaic device, which the central and intended theme of this study suggests could be greatly augmented. However, we consciously chose not to exercise this option with the aim to preserve the relevance of the simulation outcome with regards to the adoption of Mo as the back contact in the SLG/Mo/p-absorber/n-CdS/n-ZnO/Ag device configuration. The significance of the back contact barrier height and its influence on the photovoltaic performance parameters will be highlighted in the subsequent section whenever the need arises.

3.2. Case I: Ideal Absorber Layer (No Defect)

Figure 3 below depicts the effects of carrier mobility and carrier concentration of the CdS buffer layer on the efficiency of a thin film solar cell with an ideal absorber layer.

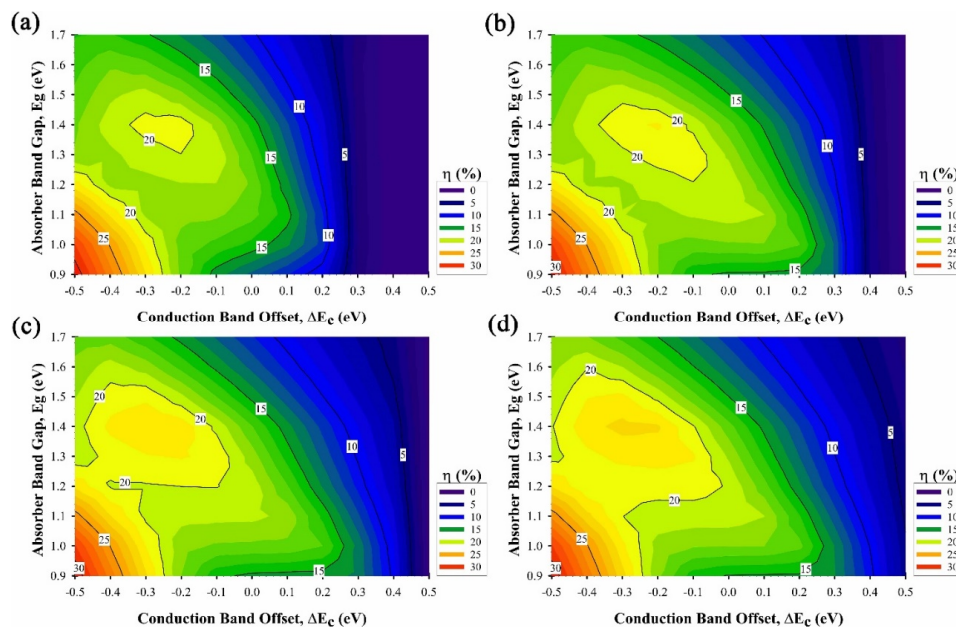


Figure 3. Effect of μ and N_D of the CdS buffer layer on the conversion efficiency of thin film solar cell with an ideal absorber layer: (a) Set A: $\mu = 1 \text{ cm}^2/\text{V}\cdot\text{s}$ and $N_D = 10^{14} \text{ cm}^{-3}$, (b) Set B: $\mu = 100 \text{ cm}^2/\text{V}\cdot\text{s}$ and $N_D = 10^{14} \text{ cm}^{-3}$, (c) Set C: $\mu = 1 \text{ cm}^2/\text{V}\cdot\text{s}$ and $N_D = 10^{18} \text{ cm}^{-3}$, and (d) Set D: $\mu = 100 \text{ cm}^2/\text{V}\cdot\text{s}$ and $N_D = 10^{18} \text{ cm}^{-3}$.

By comparing Figures 3a–c and 3b–d, it can be clearly seen that for a constant carrier mobility, a CdS buffer layer with higher carrier concentrations results in a minor increase in the conversion efficiency. By scrutinizing Figure 3 as well, a couple of similar patterns were observed and highlighted as follows. Firstly, regardless of the electrical properties of the CdS buffer layer, an absorber layer with lowest band gap of 0.9 eV and CBO of -0.5 eV produces the thin film solar cell with the highest efficiency in the 30% range. Secondly, the lowest performing devices are generally composed of an absorber layer with CBO in the range of 0.3 to 0.5 eV. On the other hand, a couple of conspicuous distinctions were observed on the conversion efficiency pattern with respect to the different electrical properties of the CdS buffer layer, namely affecting the carrier mobility. Firstly, it could be clearly seen that as the carrier mobility increases from 1 to $100 \text{ cm}^2/\text{V}\cdot\text{s}$ irrespective of carrier concentration, the low efficiency window ($<5\%$) shrinks considerably. Concurrently, an efficiency of more than 20% which was initially centered at a band gap of 1.4 eV and

CBO of -0.25 eV expands to a larger region, which is indicative of the wider suitability of the CdS buffer layer for a broader range of photo-absorber materials.

We attempt to delineate the observed trend as depicted in Figure 3 by dissecting the relevant photovoltaic performance parameters, which ultimately govern the solar cell conversion efficiency. Generally, the conversion efficiency is calculated according to Equation (5) as shown below, whereby FF is the fill factor, V_{oc} is open circuit voltage, J_{sc} is short circuit current and P_{in} is input power [62].

$$\eta = \frac{FF V_{oc} J_{sc}}{P_{in}} \quad (5)$$

For the purpose of clarity and simplicity, simulation outcomes pertaining to the CdS buffer layer of set A and set D, which represents the lower and upper limit in terms of carrier mobility and carrier concentration values, were chosen for comparative analysis. Figures 4 and 5 illustrate the (a) V_{oc} , (b) J_{sc} , (c) FF and (d) η for a thin film photovoltaic device with a CdS buffer layer of set A and set D, respectively. Corresponding results for the CdS buffer layer of set B and set D are given in supplementary information (SI) as Figures S1 and S2, respectively. It is important to note that absorber layer with negative CBO values yields higher efficiency compared to a absorber layer with a positive CBO. This observed occurrence is contrary to the outcome of practical measurements whereby a small positive CBO in the range of 0.1 to 0.4 eV conventionally results in higher conversion efficiency and a negative CBO is expected to yield lower efficiency [63–66]. However, these phenomena are not reflected in this study due to the fact that the beneficial effects of a small positive CBO and detrimental effects of a negative CBO only come into play if a n-CdS/p-absorber hetero-interface recombination mechanism is taken into account. Due to the scope of this study, which focuses primarily on the electrical properties of the CdS buffer layer and its suitability for a set of variable absorber layers with different bulk defect densities, interfacial recombination mechanism was not incorporated. The interdependence between CdS electrical properties with an element of an interfacial recombination mechanism and their combined influence on the photovoltaic performance of various thin film solar cells deserves an entirely discrete numerical simulation study. Nonetheless, partial treatments of the suggested study as above, which solely focuses on CIGS solar cells, can be found elsewhere [67,68].

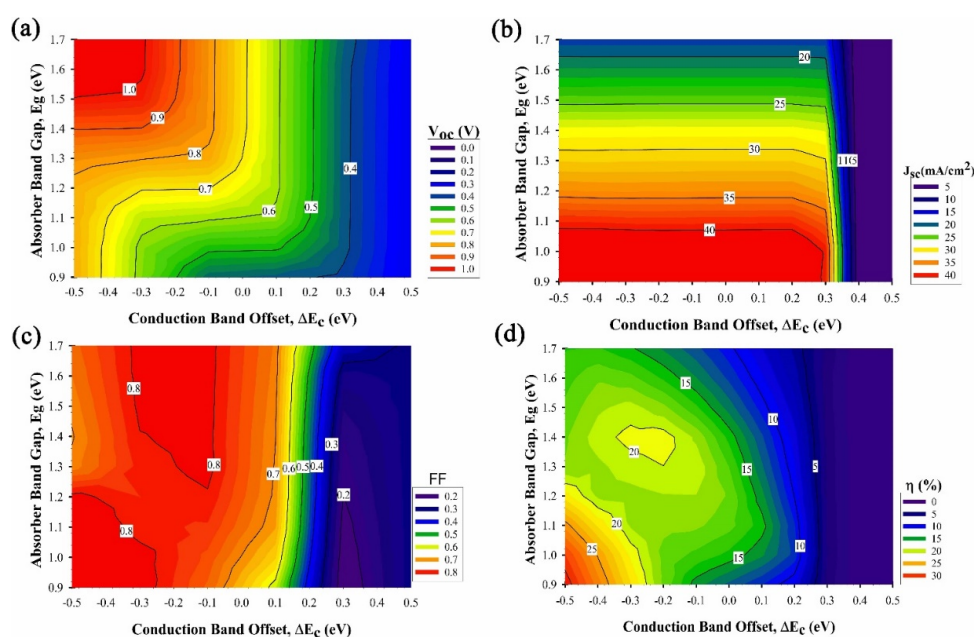


Figure 4. Photovoltaic performance parameters (a) V_{oc} , (b) J_{sc} , (c) FF and (d) efficiency for an ideal p-absorber layer with a CdS buffer layer of Set A (μ : $1 \text{ cm}^2/\text{V}\cdot\text{s}$ and N_D : 10^{14} cm^{-3}).

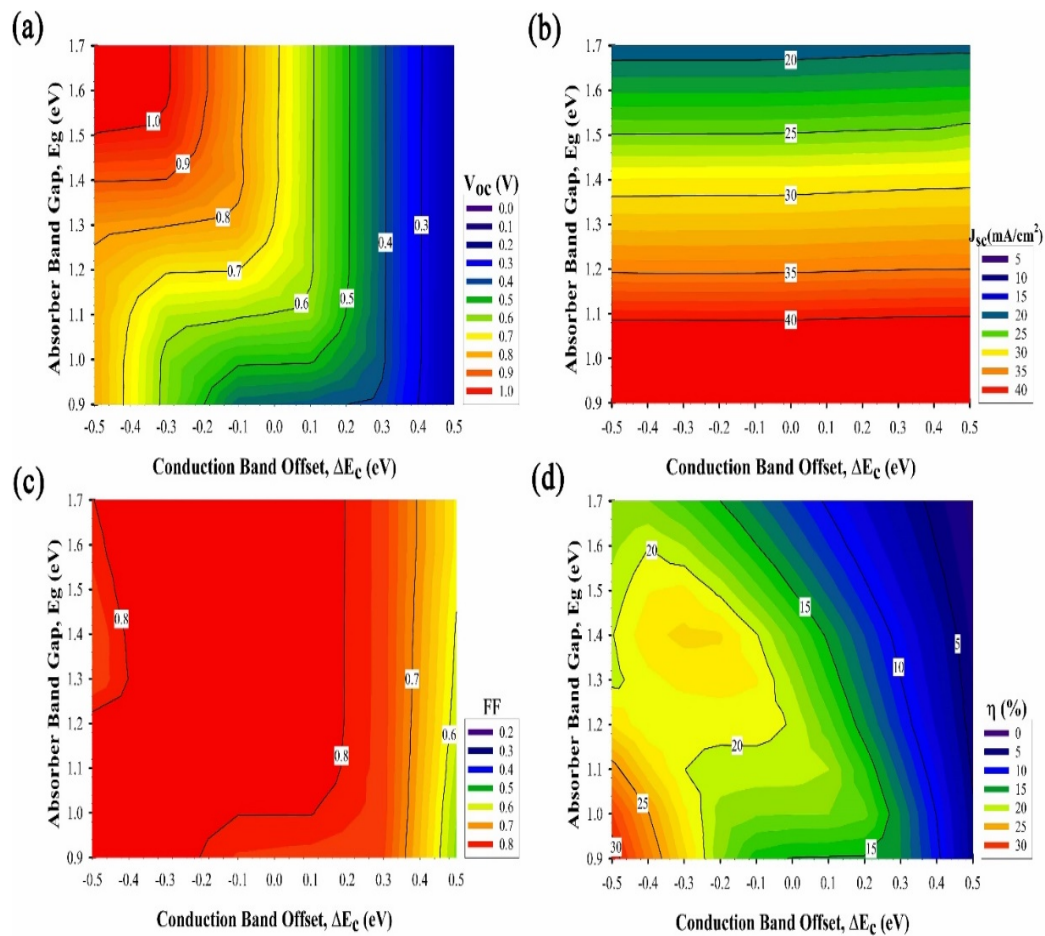


Figure 5. Photovoltaic performance parameters: (a) V_{oc} , (b) J_{sc} , (c) FF and (d) efficiency for an ideal p-absorber layer with a CdS buffer layer of Set D (μ : $100 \text{ cm}^2/\text{V}\cdot\text{s}$ and N_D : 10^{18} cm^{-3}).

By comparing Figures 4a and 5a, it can be seen that the V_{oc} parameter registers insignificant changes. In fact, similar V_{oc} plots were also observed for Figures S1a and S2a, indicating there is another variable that dictates the resulting V_{oc} , regardless of the electrical properties of the CdS buffer layer. We postulate that the back contact barrier height between Mo and p-absorber as depicted in Figure 2 in tandem with absorber band gap is accountable for the V_{oc} trend. It has been experimentally proven that when the back contact barrier height approaches a certain threshold value, V_{oc} is severely reduced under the reach through a diode regime [69,70]. From this simulation, we have found that for an absorber layer with a band gap of 0.9 eV, a back contact barrier height of more than 0.55 eV results in the V_{oc} value being pegged at 0.4 V or lower. As the band gap is increased linearly, a back contact barrier height with a similar incremental rate yields a similarly low V_{oc} in the region of 0.3 V to 0.4 eV for the entire investigated range of the absorber band gap. Hence, it can be said that for an ideal absorber layer (no defect), V_{oc} is predominantly influenced by the absorber layer band gap and back contact barrier height, rather than by the electrical properties of the CdS buffer layer. On the other hand, the J_{sc} parameter differs considerably as illustrated in Figures 4b and 5b, mainly in the high CBO region of $> 0.3 \text{ eV}$. CdS with higher electrical resistivity (Set A- Figure 4b) records an abrupt decline in the J_{sc} onset of an CBO value of 0.35 eV. A positive CBO represents a spike-like band edge, which causes an impediment to the transport of photogenerated carriers (electrons) with a low carrier mobility, and subsequently yields lower carrier collection at the front contact and thus a lower J_{sc} . However, CdS with a higher carrier mobility and carrier concentration (Set D- Figure 5b) could retain a high J_{sc} value in the same CBO region. This could be due

to the increased diffusivity (D_n) of carriers, induced by higher carrier mobility as governed by the equation shown below [71]:

$$D_n = \frac{\mu_n k_B T}{q} \quad (6)$$

where D_n , μ_n , k_B , T and q are the carrier diffusivity, electron mobility, Boltzmann constant, absolute temperature and the magnitude of charge of an electron, respectively. In return, increased diffusivity is responsible for a longer carrier diffusion length and subsequently for a higher photogenerated current, I_{ph} as evident in the following relationship shown in Equations (7) and (8) below [61]:

$$L_n = \sqrt{D_n \tau_n} \quad (7)$$

$$I_{ph} = qAG(L_n + W + L_p) \quad (8)$$

where $L_{n/p}$ is the diffusion length of the electron/hole, D_n is the carrier diffusivity and τ_n is the carrier lifetime, meanwhile A is the cross-sectional area, G is the carrier generation rate and W is the depletion width of the heterojunction. Based on Equation (9) below, we note that the depletion region width, W for a heterojunction consisting of CdS with a higher carrier concentration (Set D- N_D : 10^{18} cm^{-3}) should be lower compared to the depletion width for CdS with a lower carrier concentration (Set A- N_D : 10^{14} cm^{-3}) [72]:

$$W_d = \left[\frac{2\epsilon_1\epsilon_2(V_{bi} - V)(N_A^2 + N_D^2)}{q(\epsilon_1N_D + \epsilon_2N_A)N_DN_A} \right]^{1/2} \quad (9)$$

where q , ϵ_1 , ϵ_2 , V_{bi} , V , N_A , and N_D are the electric charge of an electron, dielectric permittivity of CdS, dielectric permittivity of p-absorber, built-in voltage, applied voltage, acceptor concentration in the p-absorber layer and donor concentration in a CdS buffer layer, respectively. However, a higher J_{sc} value for CBO > 0.3 eV was recorded for CdS of Set D (Figure 5b) despite the reduced depletion width, which was supposed to decrease the photogenerated current according to Equation (8). This could be due to beneficial synergistic effects of high carrier mobility and a narrower depletion region, which enables carriers to overcome a high CBO barrier. This is supported by the fact that only CdS of Set D, which represents a buffer layer with the highest carrier mobility and highest carrier concentration, exhibits a high J_{sc} across all investigated CBO values (please see Figures S1b and S2b in the supplementary data for the J_{sc} plot for CdS of Set B and Set C, respectively).

3.3. Case II: Absorber Layer with Variable Defect Density

In this section, the performance of thin film solar cells consisting of absorber layer with varying defect density is presented and discussed. Figure 6a–f below shows the conversion efficiency for a thin film device with the variable absorber layer bulk defect density and electrical properties of the CdS buffer layer (the corresponding V_{oc} , J_{sc} and FF plots for Figure 6 are given in supplementary data as Figures S3–S5, respectively). Again, with the aim to highlight the discernible role of carrier mobility and carrier concentration of the buffer layer, simulation outcomes for CdS of Set A (μ : $1 \text{ cm}^2/\text{V}\cdot\text{s}$ and N_D : 10^{14} cm^{-3}) and Set D (μ : $100 \text{ cm}^2/\text{V}\cdot\text{s}$ and N_D : 10^{18} cm^{-3}) have been selectively chosen for comparative analysis. Overall, as the defect density increased, efficiency decreased quite dramatically. This was not unexpected due to the fact that defect states act as detrimental recombination centers for photo-generated charge carriers [73]. It is also evident that an increase in the carrier mobility and carrier concentration of the CdS buffer layer yields higher efficiency and more importantly, enables realization of a functional device across a wider range of absorber band gaps and absorber electron affinities. As an example, for an absorber defect density of 10^{14} cm^{-3} (Figure 6a,b) and 10^{16} cm^{-3} (Figure 6c,d), by increasing the carrier mobility and carrier concentration of the CdS buffer layer, a functional device could be realized at CBO > 0.3 eV. This is due to the same reason as explained in the previous section, which is for the retention of high J_{sc} due to a higher carrier

diffusivity and efficient carrier transport across a spike-like CBO barrier, particularly for CBO > 0.3 eV (Please see Figure S3a–d).

As the absorber defect layer is increased to 10^{16} and 10^{18} cm^{-3} , one important finding is the shift of optimal E_g from lower values (0.9 eV), as observed in case of a defect free absorber to higher values (1.4 to 1.5 eV). This is probably due to a comparatively higher impact of defect states in a narrow band gap material than a wider band gap material [74]. This fact is further exemplified in the V_{oc} plot (Please see Figure S4), whereby a decrease in the V_{oc} parameter for the absorber layer with the highest defect density of 10^{18} cm^{-3} is unmistakably evident, particularly for an absorber band gap of 0.9 eV, regardless of the CBO value. An increase in the carrier mobility and carrier concentration of the CdS buffer layer shifts the efficiency sweet spot from a CBO of -0.2 to -0.1 and E_g of 1.2 to 1.4 eV to a slightly narrower region ranging from a lower CBO of -0.4 to -0.3 to a higher E_g of 1.45 to 1.6 eV, as depicted in Figure 6e,f.

Based on the results and discussion from the previous sub-sections, significant impacts of electrical properties of the CdS buffer layer on the development of substrate type configured thin film photovoltaic technology are emphasized as follows. A SLG/Mo/p-absorber/n-CdS/n-ZnO/Ag device configuration is conventionally adopted in the initial development of novel and emerging p-type photo-absorber material. The primary reason for this choice is mainly due to its efficacious implementation as a preliminary baseline recipe in CIGS based technology development, which eventually led to successful commercialization at the gigawatt level after various optimizations in material, process and device fabrication levels [75]. As a consequence, deposition of CdS thin film by the CBD method has been extensively studied and subsequently adopted as the preferred buffer layer material in various photovoltaic research laboratories worldwide. From the electrical properties of the CdS buffer layer perspective, high carrier mobility implies a CdS thin film with lesser structural imperfections (grain boundary, dislocation density and point defects), which eventually leads to reduced carrier scattering [76,77]. On the other hand, a high carrier concentration implies the existence of a suitable shallow donor level below the conduction band edge E_c either due to extrinsic doping or intrinsic native defects, which increases the free electron density in the conduction band through the thermal ionization process [71,78]. Therefore, to achieve the desired electrical property, the microstructural properties of CdS thin film and a doping mechanism which are at play need to be meticulously modulated through deposition, doping and post-deposition process optimizations. However, in the initial stage of explorative investigation of an emerging p-absorber thin film material, the central scope and effort are always focused on the absorber layer material development (material synthesis, deposition process, post-deposition treatment and thin film characterization). Due to this skewed focus, the buffer layer deposition process is usually treated as part of the device completion fabrication step, in which a routine CdS-CBD 'baseline' recipe is usually being utilized. This 'baseline' recipe typically originates from previous in-house optimization, which was used to deposit CdS as a heterojunction partner for different p-absorber material or was adapted from pertinent literature. We argue that if the electrical properties of the ensuing CdS buffer layer are not properly fine-tuned and characterized, it may lead to incorrect assumptions particularly on the true potential of the investigated p-absorber material. For example, let us say that a particular p-absorber material with band gap of 1.1 eV and CBO of 0.1 eV is being investigated. In the preliminary stage of development, it is highly likely for the absorber thin film to possess a high bulk defect density (i.e., 10^{18} cm^{-3}) due to its polycrystalline nature and non-optimized deposition process. If the deposited CdS buffer layer possesses low carrier mobility and a low carrier concentration, the corresponding device is predicted to yield efficiency below 5% (see Figure 6e). However, the device efficiency can be boosted above 5% by employing a CdS buffer layer with a higher carrier mobility and higher carrier concentration (see Figure 6f). Although the difference in conversion efficiency seems to be inconspicuously small, nevertheless the initial device performance of a new p-absorber material plays a paramount role in determining its subsequent progression trajectory, through further

systematic and sustained investigation. Therefore, there exists a substantial possibility for an emerging absorber material to be prematurely dismissed as a promising photovoltaic material, merely after a few experimental attempts, partially due to non-optimal electrical properties of its CdS buffer layer.

We also note that the electrical properties of CdS thin films, namely the carrier mobility, carrier concentration and resistivity which are reported across the present literature, are predominantly characterized by a ‘dark’ Hall measurement. At the same time, the photoconductivity phenomenon in CdS thin film has been well-documented [79]. Since the basis of thin film solar cell operation is converting light into electricity, understanding the complete charge carrier dynamics of a CdS buffer layer under illumination could be the key to unlocking pathways towards high efficiency thin film solar cells. With the recent advent of the carrier-resolved photo-Hall effect technique, which permits simultaneous measurement of mobility and concentration of both majority and minority carriers, as well as the recombination lifetime, diffusion length and recombination coefficient, we believe this method will shed more insights into the electrical properties of the CdS buffer layer in the near future [80].

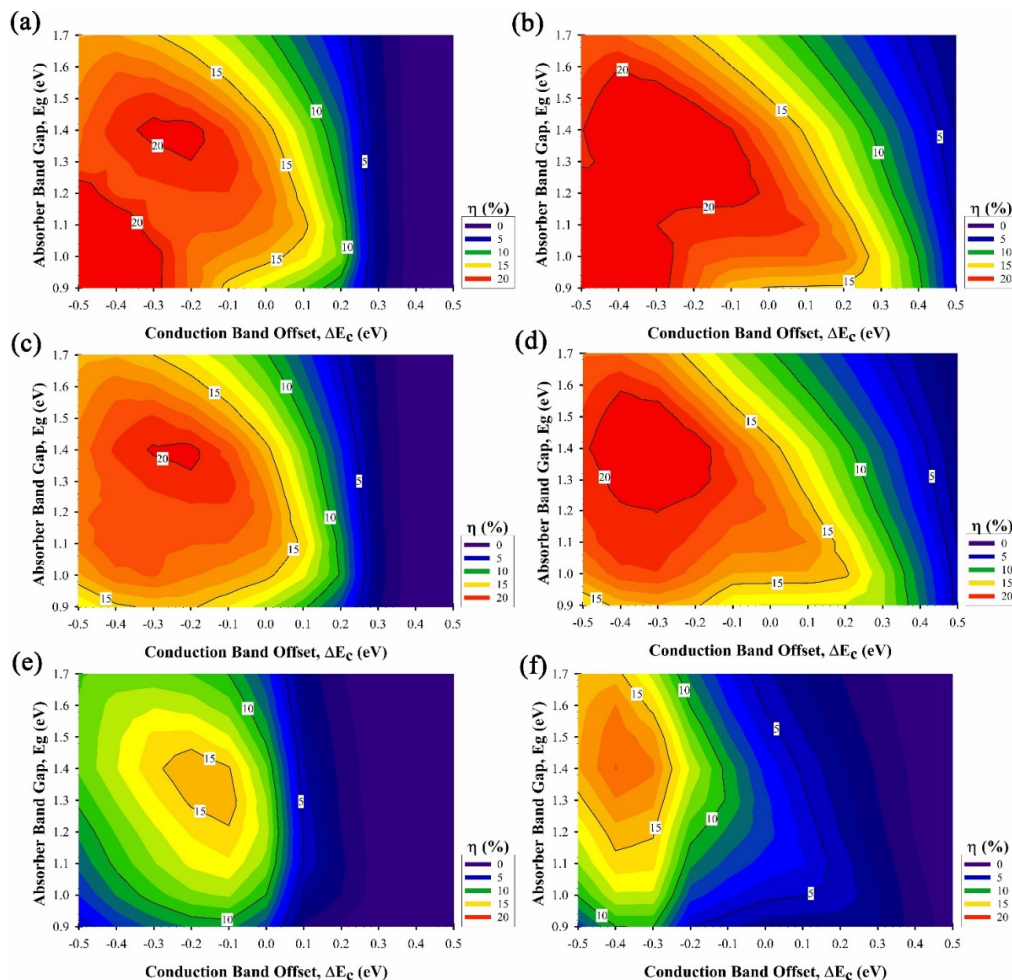


Figure 6. Effect of μ and N_D of the CdS buffer layer on the conversion efficiency of thin film solar cell with practical p-absorber layer having a different bulk defect density (BDD). (a) CdS-Set A and BDD: 10^{14} cm^{-3} , (b) CdS-Set D and BDD: 10^{14} cm^{-3} , (c) CdS-Set A and BDD: 10^{16} cm^{-3} , (d) CdS-Set D and BDD: 10^{16} cm^{-3} , (e) CdS-Set A and BDD: 10^{18} cm^{-3} and (f) CdS-Set D and BDD: 10^{18} cm^{-3} .

4. Conclusions

The numerical simulation works presented herein are primarily focused on assessing the impacts of the electrical properties of the CdS buffer layer, namely the carrier mobility and carrier concentration on the performance of SLG/Mo/p-Absorber/n-CdS/n-ZnO/Ag configured thin film photovoltaic devices. For an ideal absorber layer (no defect), the carrier mobility and carrier concentration of the CdS buffer layer do not significantly alter the maximum attainable efficiency. Generally, it was revealed that J_{sc} is strongly dependent on the carrier mobility and carrier concentration of the CdS buffer layer for absorber layer with a CBO of more than 0.3 eV, whereas V_{oc} is predominantly dependent on the back contact barrier height. In an ideal case (p-absorber layer with no defect), the highest conversion efficiency is achieved and it was found that the electrical properties of CdS have a less significant impact on the conversion efficiency. Generally, the conversion efficiency is reduced as the bulk defects are introduced in the absorber layer. However, as the bulk defect density of the absorber layer is increased from 10^{14} to 10^{18} cm^{-3} , the CdS buffer layer with a higher carrier mobility and carrier concentration yielded devices with a higher conversion efficiency and most importantly, a larger band gap-CBO window for the realization of functional devices. These observed outcomes were attributed to beneficial synergistic effects of high carrier mobility and a narrower depletion region, which enable carriers to overcome a high CBO barrier. By inference, we have also highlighted that a CdS buffer layer with a high carrier mobility and carrier concentration is an indispensable component in the development of any particular substrate type thin film photovoltaic technology.

Supplementary Materials: The following are available online at <https://www.mdpi.com/2079-6412/11/1/52/s1>, Figure S1: Photovoltaic performance parameters for an ideal p-absorber layer with a CdS buffer layer of Set B (μ : $100 \text{ cm}^2/\text{V}\cdot\text{s}$ and N_D : 10^{14} cm^{-3}); Figure S2: Photovoltaic performance parameters for an ideal p-absorber layer with a CdS buffer layer of Set D (μ : $1 \text{ cm}^2/\text{V}\cdot\text{s}$ and N_D : 10^{18} cm^{-3}); Figure S3: Effects of μ and N_D of a CdS buffer layer on the open circuit voltage of thin film solar cell with a practical p-absorber layers having a different bulk defect density (BDD); Figure S4: Effect of μ and N_D of a CdS buffer layer on the short circuit current density of a thin film solar cell with a practical p-absorber layer having a different bulk defect density (BDD); Figure S5: Effect of μ and N_D of a CdS buffer layer on the fill factor of thin film solar cell with a practical p-absorber layer having a different bulk defect density (BDD).

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