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Investigation of Electrochemical Oxidation Behaviors and Mechanism of Single-Crystal Silicon (100) Wafer under Potentiostatic Mode

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Abstract: Electrochemical oxidation (ECO) has been used widely to oxidize single crystal Si wafers. Aiming at optimizing the ECO assisted machining methods, the oxidation behaviors of single-crystal silicon (100) wafer under potentiostatic mode are experimentally investigated. It is shown that the Si wafer can be electrochemically oxidized and the oxidized film thickness reaches to 239.6 nanometers in 20 min. The hardness of the oxidized surface is reduced by more than 50 percent of the original surface. The results indicate that the oxide thickness and the hardness can be controlled by changing the voltage. Based on the experimental findings, a hypothesis on the ECO mechanism under potentiostatic mode was proposed to explain the fluctuations of current density under specific applied voltage. The occurrence of the multiple peaks in the current density curve during the oxidation process is due to the formation of discharge channels, which was initiated from the defects at the interface between the oxide bottom and the substrate. This breaks the electrical isolation and leads to the discontinuous growth of the electrochemical oxide layer. The present work contributes to the fundamental understanding of the ECO behaviors for the single-crystal Si (100) wafer under potentiostatic mode.

Keywords: silicon; potentiostatic mode; electrochemical oxidation; oxidation behaviour

1. Introduction

Chemical mechanical polishing (CMP) is one of the most commonly used polishing method for silicon wafers and it is a crucial step in the processing of silicon wafers in semiconductor manufacturing technology [1]. Despite its wide application, many problems still exist. Firstly, although a lot of process parameters have been proved to affect the polishing results of silicon wafers, controlling over the process variables within a narrow range is relatively hard [1,2]. In addition, CMP is a combination of both chemical and mechanical processes. New types of defects will be introduced from the CMP process and these defects are critical for some sub-micro meter features, which makes the development of additional processes required. Another problem of CMP is that both the equipment and consumables are expensive. The polishing slurry and all the other parts require a high maintenance and frequent replacement. The disposal of CMP chemicals also leads to severe environmental pollution [3]. On the other hand, because of the high hardness and strong chemical inertness, the material removal rate (MRR) of silicon wafer by CMP has reached its limit [4]. It is challenging to further improve the MMR and simultaneously minimize the subsurface damage (SSD). All the above-mentioned drawbacks and



the limitation of CMP makes it necessary to develop some new polishing methods for Si wafer, so that to avoid all the harmful effects [3,4].

Electro-chemical assisted hybrid polishing methods on SiC wafer have been developed and studied by many researchers, including electrochemical mechanical grinding [5], electrochemical mechanical polishing (ECMP) [4,6], and electrochemical-assisted multi-wire saw [7]. In these studies, the SiC surface was modified to oxide the layer and softened to realize easier material removal. At the same time, the sub-surface damage (SSD) layer would be removed due to the formation of oxide layer on the surface [4–8]. The surface structure development and the electrochemical oxidation (ECO) mechanism in SiC were investigated in detail. The generation of the oxide layer was also found to strongly affect its subsequent polishing or machining process, since the polishing and material removal is conducted on a softer oxide layer than the original surface [2,4]. Another important advantage of ECO is that it does not need any complex or expensive devices. The overall process can be done under low temperature and with low cost [9]. In addition, the ECO treatment can be especially involved to the applications that required incomplete oxidation of porous Si [10]. Although it has been reported that the oxidation reaction on the SiC is much slower than that of Si under the same oxidation conditions, which makes ECMP have a great potential to be applied on Si wafer [11,12]. Additionally, some papers have been published on the ECO treatment of porous silicon. The results illustrated that the electric parameters have great influence on the formation of the oxide [11,13,14]. Essentially, ECMP and CMP are chemical erosion processes, during which the electrochemical characteristic of the wafer also plays an important role [15]. To put the ECO technique into the application of ECO assisted polishing for Si wafer, it is necessary to learn more about its mechanism and include the electrochemical behavior of silicon wafer into the polishing study. The electrochemical oxidation of silicon has been studied since 1991 [16]. In this research, it is proved that the oxidation process is governed by the holes' supply on the Si- electrolyte interface. The formation of electrochemical oxide of Si in Acetonitrile has also been investigated [17] and several more related works have been done on the electrochemistry of Si and its oxide [18–20]. However, there is little research focused on its application on the single crystal Si wafer. The ECO mechanism of single crystal silicon wafer is also not fully understood and there is no research conducted that explains the details of the ECO behavior when the single crystal Si wafer is exposed to a neutral solution.

Therefore, in the present study, to obtain a better understanding of the ECO behavior and mechanism of single-crystal Silicon (100) wafer under potentiostatic mode, the ECO based on the different parameters including the applied voltage and exposed durations were carefully investigated. Based on the experiments' results, a hypothesis on the ECO mechanism is proposed. This can be a preliminarily evidence to verify the feasibility of ECO-assisted polishing, so as to improve the surface quality and the polishing process efficiency of the silicon wafer in the future.

2. Materials and Methods

In this work, single-side polished single crystal Si (100) wafer with 1–30 Ω ·cm and thickness of 400 µm were used. The Si wafer is p-type, which is randomly doped with Boron. In p-type wafer, the Si wafer is rich in holes as the charge carriers. All the experiments were carried out on the polished side, having a surface roughness of 392 nm. Each batch of the Si samples are cut from the same slice of wafer to keep consistent. Before the electrochemical oxidation experiments, all the wafers were cleaned with acetone and alcohol by ultrasonic cleaner (RS Components Ltd., Northants, UK) for 10 min at 30 °C, then rinsed with deionized water and finally dried by compressed nitrogen.

The experiment setup developed for this study is shown in Figure 1. It mainly consists of three parts: potentiostat, a PTFE-made electrolytic cell, and a personal computer (PC). The current and voltage are controlled by the potensiostat and the potensiostat is controlled by the PC. The experimental data is captured by the PC software (Kickstart). During electrochemical oxidation, the silicon wafer was attached to the working electrode and pressed against an O-ring with an exposure area of 1 cm² on the side wall of the electrolytic cell. A circular aperture (diameter: 10 mm) was utilized to realize this

contact between silicon wafer to the electrolyte. A platinum (Pt) mesh plays as the counter electrode and all the anodizing samples are prepared using a potentiostat (KEITHLEY 2280S-60-3, Solon, OH, USA) and two-electrode system. Potassium chloride (KCl) solution configured from 10 g reagent grade KCl powders (Sigma Aldrich) per 1 L Deionized (DI) water was used as electrolyte for our study. The experimental conditions are given in Table 1. External supply of voltage from 10 to 50 V is given to the system.



Figure 1. Schematic diagram of the experiment setup for electrochemical oxidation process.

Specimen	Single Crystal Si (100) Wafer, Polished on One Side
Electrolyte	Potassium chloride (KCl) solution (10 wt.%)
Anodizing mode	Potentiostatic polarization
Voltage	10 V, 20 V, 30 V, 40 V, 50 V

The surface morphology change of single crystal silicon wafer after anodizing was observed using Atomic Force Microscope (Bruker, Billerica, MA, USA) to confirm the change before and after the exposure to the electrolyte and the effect of different applied voltage. The thickness of the generated oxide layer was accurately measured using the Ellipsometer (nanofilm_ep4, Goettingen, Germany) to confirm the formation of the oxide. For each sample, three points were measured and an average of the oxide film thickness was taken. Nano indentation (Nanotest, Micro Materials Ltd., Wrexham, UK) was also conducted to compare the mechanical hardness change before and after the oxidation. The indenter used for the nano indentation is Berkovich, which has the same projected area-to-depth ratio as a Vickers indenter [21]. For each sample, three readings were taken and each reading was repeated three times to take the average value.

The surface topography observed by Atomic Force Microscope (AFM) has shown that the oxidized surface has a porous structure at the initial stage. With longer exposure time, uniform protrusions would gradually form a compact oxide layer. Although it is not a continuous growth, the hardness of the oxidized layer can be reduced 50% after 20 min with the external supplied voltage of 50 V, compared with the original mechanical hardness. This means that a thick softer oxide layer could form in a fast speed, which is beneficial for the further polishing or another mechanical removal process. Based on the experimental results and analysis, the formation of the oxide structure and the ECO mechanism for Si wafer under potentiostatic mode were proposed. This provides good evidence of the fluctuations of current density, as well as to prove the discontinuity of the oxide growth. The study of the ECO mechanism and the surface behavior during the ECO process potentially helps to verify the feasibility of its application to electrochemical assisted polishing on Si wafer.

3. Results

3.1. Effect of Current Density and Time on Si Wafer

During the anodizing process, the oxide film is grown on the Si wafer by passing a direct current through the electrolytic solution. The growth of the oxide is based on the movement of the charge carriers to the electrolyte/Si interface [22,23]. Therefore, the detailed plot of current density curve for Si wafer under different voltage is effective for predicting the formation of oxide layer [24]. The curves indicating the current density change for Si wafer under different applied voltage (10 V, 20 V, 30 V, 40 V, 50 V) is given as in Figure 2a. The current density vs. time curve under 10 V is enlarged in Figure 2b. From this figure, the anodization process is fast when higher potential is applied. As the oxide layer forms, the current density drops very fast at the initial stage, even under a low voltage of 10 V, as seen in Figure 2b. The current density drops swiftly at the early stage and continues to drop close to 0 V. However, when the applied potential is increased to more than 20 V, there are several fluctuations with multiple peaks, as seen in the curves under the applied voltage from 20 to 50 V. The fluctuations are more obvious in the curve under 40 and 50 V, compared with the lower voltages. As in Figure 2 at 50 V, the current density first drops to a local minimum value and then increases to a local peak value and repeats this trend for several times under high voltage during the further progression.

This current density fluctuation indicates that there must be a transition state during the formation of the oxide film process. Once the compact oxide layer is completely formed on the whole exposed surface, the discharge channel for electron pathways through the insulating film to the conductive Si substrates would be blocked. Such blocking leads to the local drop of the current density and it reaches the local minimum value [25]. After a short time, local pore would start to form and break the electric filed barrier, which is a crucial step that can provide channels for electrons and current to flow through. Subsequent current density drop is due to the same cycle of occurrence for several times, when the other high voltage is applied.



Figure 2. Current density versus time curve for Si wafer during the electrochemical oxidation (ECO) process (**a**) 10 V, 20 V, 30 V, 40 V, 50 V (**b**) Enlarged curve for 10 V.

3.2. Surface Morphology Observation

The optical photograph of the anodized Si-wafers under different applied voltage is shown in Figure 3. It can be seen that the oxidized surface show varied colors with different process parameters. The visual color difference indicates the properties of the porous oxide surface structure, which can reflect a specific wavelength of light [26]. As the voltage increased and the exposure time extended, the appearance of the oxide film changed with its oxide thickness, porosity, and surface structure [27–29]. The large difference of the reflections for different samples means that the surface structure and oxidation process are not the same under different experiment conditions.



Figure 3. The optical photograph of the anodized Si wafers under different applied voltage.

The surface morphology change of the Si wafer with exposure to KCl solution under different anodizing condition is shown in Figures 4 and 5. The figures are measured by AFM at a typical tapping mode with scan rate of 1.5 Hz, $3 \mu \text{m/s}$ (scan lines per second).

It can be seen that there are obvious changes in the surface morphology after anodizing with different voltages. Figure 4a is the AFM image for the as received wafer. Under low voltage, it is hard to observe the oxide layer on the surface, which corresponds to the current density curve with a relatively minor decrease, as in Figure 2b. As the anodizing potential increases to 40 V, uniform protrusions can be observed on the surface and the protrusions becomes denser with higher voltage. The height sensor also reveal that the height difference is more significant under higher voltage (50 V, 7.4 nm). Based on the AFM results in Figure 4, higher voltage is easier to contribute to the growth of oxide protrusions.

Figure 5 shows the AFM images and the three-dimensional topography for the oxidized wafers under 30 V after (a) 100 s, (b) 200 s, (c) 400 s, (d) 600 s, (e) 1200 s. At the initial stage, the oxide layer formation is randomly distributed locally, which means that there must be some locations that have the priority to be oxidized based on the surface characteristics. As the exposure duration increases, the density of the oxide protrusions gradually become higher and the exposed surface is oxidized to a thicker layer, as can be seen in the height sensor bar difference. It is revealed that the oxide formation progresses with the increase of oxidation duration, the same applied external voltage.

Figure 6 shows the three-dimensional AFM image under 50 V, with an exposure duration for 1200 s. From the surface topography in this figure, there is a compact oxide layer formed under this condition. Even though the current density curve shows it is not a monotonically growth process, the oxide layer seems to grow thicker with higher applied voltage (50 V). However, to further confirm that the oxide layer can grow faster with longer exposure or under higher applied voltage, the oxide film thicknesses were measured using the Ellipsometer.



Figure 4. Atomic Force Microscope (AFM) image under different conditions (**a**) as received wafer; (**b**) 10 V 100 s; (**c**) 20 V 100 s; (**d**) 30 V 100 s; (**e**) 40 V 100 s; (**f**) 50 V 100 s.



Figure 5. Cont.



Figure 5. AFM image under 30 V with different duration (a) 100 s; (b) 200 s; (c) 400 s; (d) 600 s; (e) 1200 s.



Figure 6. Three dimensional AFM image under 50 V with an exposure duration of 1200 s ($500 \times 500 \text{ nm}^2$).

3.3. Oxide Film Thickness

The oxide film thicknesses were obtained using the Ellipsometer (EP4 spectroscopic imaging) with high lateral resolution. For each sample, three measurement results were taken to obtain the average value. The measurement results of the electrochemically oxidized surface are shown as in Figure 7.

Although the oxide film thickness is not strictly proportional to the exposure time due to the effect of the initial surface, however, the thickness of the oxide layer increases with the applied voltage if applied with the same exposure duration and a stronger oxidation reaction, which would obviously happen under high voltage. Extended exposure time would reveal an obvious oxidation rate difference. It should also be noticed that there is a positive correlation between the oxide film thickness and the exposure time under certain voltage. This shows a good agreement with the descending current density versus time curve as given in Figure 2. In addition, the oxidation film growth also corresponds to the AFM topography evolution, as shown in Figure 5. Under specific voltage (50 V), the oxide protrusions gradually distribute on the whole surface. The thickness of the oxide can grow to 240 nm after 1200 s. To validate that the oxide layer contributes to a softer surface, the hardness of the processed surface must be measured.



Figure 7. Oxide film thickness obtained from the ellipsometric parameters.

3.4. Hardness Change

Nano indentation was used to measure the hardness and the elastic modulus of the surface layer before and after electrochemical oxidation. Two indentation depths of ~20 nm and ~30 nm were chosen to avoid any substrate effects.

In Figure 8, the results of the Nano indentation hardness test before and after anodizing at different conditions are given for the following: (1) as received Si wafer, (2) electrochemically oxidized surface (exposure time 600 s, voltage: 30 V), (3) electrochemically oxidized surface (exposure time 1200 s, voltage: 50 V). They reveal that after electrochemical oxidation, the surface hardness decreases significantly to 64% of the original and achieves a 2.98 GPa under (3) with indentation depth of ~30 nm. Based on the hardness test, a much softer layer can be formed on the surface under higher voltage (50 V), which is helpful for the following mechanical removal process.

The ECO process was designed to create low hardness oxides and realize easier removal by particle abrasion of the chemically passivated surface [28]. Electrochemical oxidation assisted polishing is a wear-based material removal process that combines electrochemical oxidation and mechanical removal by abrasive particles. The material removal is governed by Archard's law [29], as expressed in the followed Equation (1):

$$V(') = k(FL_{\rm s})/H \tag{1}$$

where *k* represents removal rate constant, *F* represents the normal force, L_s represents sliding distance, and *H* represents the hardness of the material, which is a material property. The material volume that would be removed denotes V(').

Based on this equation, it is generally concluded that a softer oxide layer is easier to be removed mechanically. Our investigation verified that the electrochemical oxidation for Si is effective to reduce the hardness, which has the potential to help the material removal in the polishing process. To find a balance between the oxide formation and mechanical removal, it is necessary to understand the mechanism during the electrochemical oxidation process.



Figure 8. Results of the nano-indentation hardness test before and after anodizing under different conditions (1) as-received surface; (2) 30 V 600 s; (3) 50 V 1200 s.

4. Discussion

From the experimental findings, the hypothesis for the mechanism of the electrochemical oxidation process of single crystal Si (p-type) wafer under potentiostatic mode is proposed below. The holes in Si wafer will be driven to the Si/electrolyte interface by the applied electric field. At the same time, electrons are channeled through the external circuit towards the cathode. Hydrogen molecules (H₂) are produced at the cathode with the flow of electrons. Simultaneously, the hydroxide ions (OH⁻) will be attracted to the Si/electrolyte interface by the mobile holes and reacts with the holes, generating hydroxyl radicals (OH⁻) [30,31], as expressed:

$$OH^- + h^+ \to OH^- \tag{2}$$

The hydroxyl radicals then combine and produce O₂ step-by-step and oxidize the Si surface by the following reactions:

$$OH' + OH' \to H_2O + O \tag{3}$$

$$2O \rightarrow O_2$$
 (4)

$$2Si + 4OH' + O_2 \rightarrow 2SiO_2 + 2H_2O \tag{5}$$

Based on Equations (1)–(4), the overall reaction at Si anode can be summarized as:

$$\mathrm{Si} + 4\mathrm{OH}^- + 4\mathrm{h}^+ \to \mathrm{SiO}_2 + 2\mathrm{H}_2\mathrm{O} \tag{6}$$

Combined with the above discussion, the electrochemical reactions during the ECO process of Si wafer in KCl solution, can be expressed as follows:

At the cathode (platinum electrode):

$$2H_2O + 2e^- \rightarrow 2OH^- + H_2 \tag{7}$$

For Si wafer (Anode):

$$\mathrm{Si} + 4\mathrm{OH}^{-} + 4\mathrm{h}^{+} \rightarrow \mathrm{SiO}_{2} + 2\mathrm{H}_{2}\mathrm{O} \tag{8}$$

From the chemical reactions, SiO₂ insulating layer is formed at the Si/electrolyte interface. The formation of the oxide layer depends on the charge carriers' density near the Si/electrolyte surface and the electrons transfer process in the external circuit. In the p-type Si wafer, the dopings are randomly distributed and the holes are the mobile charge carriers that will be directed to the Si/electrolyte interface by the applied voltage. Defects will also be charge carrier-rich areas, where possibly more holes will be gathered and the locally higher electric field will drive the occurrence of the oxidation process [32]. The oxidation results also clearly demonstrate that the increase of the applied voltage can contribute to a faster oxidation rate. Meanwhile, the current density change under the constant voltage mode also reveals that there are fluctuations with multiple peaks in the current density curve, due to the local block of the current. A possible model is proposed to explain the ECO mechanism of Si wafer (p-type), as shown in Figure 9.

Figure 9a shows the schematic diagram of the electrochemical oxidation cross-section. Inevitably, the crystal damage such as lattice disorders and dislocation defects from the previous course grinding cannot be completely removed even after fine polishing in the subsurface damage (SSD) layer [33,34], which would greatly affect the oxidation process. The doping sites are randomly distributed. Both the defect area and the doping sites can be considered as the charge carrier-rich areas.

As shown in Figure 9b, some oxide protrusions first build up in the damaged area. Along the locations with defects, the electric field will be locally higher and the holes are gathered, thus driving the oxidation nears these damage areas and form oxide preferentially [32,35]. As p-type Si is doping with Boron, when the boron atoms accept electron, holes will be left behind as mobile major charge carries. When the external supply of voltage is given to the p-type Si wafer, the majority carriers (holes) tends to move towards the Si/electrolyte interface. The hydroxide ions (OH⁻) will be attracted by the holes (h+) near the Si/electrolyte surface and facilitates the formation of discharge channels. Therefore, with the extension of anodizing duration, the area near the doping sites can also allow the holes to attract the hydroxide ions (OH⁻) and forms oxide protrusions in a faster speed than the locations without doping. Gradually, the oxidation happens on the whole exposed surface, as shown in Figure 9c.

However, when the oxide forms to a critical thickness, the electric field across the oxide layer would drop to a threshold value, which is too weak to allow the current to flow through. The anodization current would drop as the oxide protrusions grow. The decrease of current density, given in Figure 2, also indicates that the oxide would be a barrier and block the discharge channels for ions to flow through. Nevertheless, due to the swallowed defects and doping sites underlying the oxide, some pores would start to form again at the interface between the oxide bottom and the substrate, which will break the barrier of oxide locally and allow some local transfer of the hydroxide ions as indicated in the enlarged portion in Figure 9d. This provides discharge channels for the current to flow through and at the same time leads to the fluctuations of current density, corresponding to the repeated current density peaks in Figure 2.

The formation of the local discharge channels is a necessary step to realize the continuous growth of anodic oxide and it will further grow into a thick layer on the surface, as in Figure 9e. Once a compact oxide layer completely forms, the electrical contact between Si and the electrolyte will be blocked, as shown in Figure 9f. The limitation of the particles that take part in the ECO reaction and their transportation tend to stabilize the electric field and the current density would gradually decline to near zero, as given in Figure 2 (10 V). It would take a longer time if the applied voltage is higher, with the formation of a thicker oxide film.



Figure 9. The hypothesis of the electrochemical oxidation mechanism under potentiostatic mode. (a) schematic diagram of the electrochemical oxidation cross-section; (b) oxide protrusions first build up in the damaged area; (c) the extension of oxidation process; (d) pores formation between the oxide bottom and the substrate; (e) oxidation on the whole surface; (f) oxidation progresses to the end.

5. Conclusions

Based on the experimental investigation on the electrochemical oxidation of Si (100) wafer under potentiostatic mode, the electrochemical oxidation behavior and a hypothesis of the ECO mechanism were proposed. The experimental results clearly indicate that the applied voltage has significant influence on the oxidation rate and the oxidation behavior. The exposed Si surface under high voltage is easier to obtain a thicker oxide layer and the mechanical hardness can be greatly reduced to more than 50 percent. However, due to the breakdown of the insulating oxide, which initiated from the defects at the interface between the oxide bottom and the substrate, discharge channels would form simultaneously during the ECO progression process. This allows the ions that will take part in the ECO reactions flow through and leads to the local increase of current density. The formation of the discharge channels also contributes to the progression of the oxide from local protrusions to a compact layer. This work provides a basic understanding of the ECO mechanism and surface behavior for Si (100) wafer during the process. This would also promote the application of ECO to polishing and other machining process for single crystal Si wafer.

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