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Electrical Characteristics and Stability Improvement of Top-Gate In-Ga-Zn-O Thin-Film Transistors with Al_2O_3/TEOS Oxide Gate Dielectrics

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Abstract: In this work, two stacked gate dielectrics of Al_2O_3/tetraethyl-orthosilicate (TEOS) oxide were deposited by using the equivalent capacitance with 100-nm thick TEOS oxide on the patterned InGaZnO layers to evaluate the electrical characteristics and stability improvement of amorphous indium gallium zinc oxide (a-IGZO) thin-film transistors (TFTs) devices, including positive bias stress (PBS) and negative bias stress (NBS) tests. Three different kinds of gate dielectrics (Al_2O_3, TEOS, Al_2O_3/TEOS) were used to fabricate four types of devices, differing by the gate dielectric, as well as its thickness. As the Al_2O_3 thickness of Al_2O_3/TEOS oxide dielectric stacks increased, both the on-current and off-current decreased, and the transfer curves shifted to larger voltages. The lowest ΔV_{th} of 0.68 V and ΔS.S. of −0.03 V/decade from hysteresis characteristics indicate that the increase of interface traps and charge trapping between the IGZO channel and gate dielectrics is effectively inhibited by using two stacked dielectrics with 10-nm thick Al_2O_3 and 96-nm thick TEOS oxide. The lowest ΔV_{th} and ΔS.S. values of a-IGZO TFTs with 10-nm thick Al_2O_3 and 96-nm thick TEOS oxide gate dielectrics according to the PBS and NBS tests were shown to have the best electrical stability in comparison to those with the Al_2O_3 or TEOS oxide single-layer dielectrics.

Keywords: top-gate a-IGZO thin-film transistors; gate dielectrics; electrical characteristics; stability; hysteresis

1. Introduction

Amorphous oxide semiconductors (AOSs) are promising for channel materials of thin-film transistors [1,2] (TFTs) and are feasible for driving TFTs in organic light-emitting diode displays due to their large carrier mobility (>10 $cm^2\ V^{-1}\ s^{-1}$) and low process temperatures. The conventional bottom-gate structure has been widely studied for amorphous indium gallium zinc oxide (a-IGZO) TFTs [3,4]. However, this structure is unsuitable for integration onto the glass of peripheral circuits for the system and for the realization of high-resolution, high-quality active-matrix organic light-emitting diode (AMOLED) displays due to the high parasitic capacitance and poor scalability. Therefore, the development of self-aligned top-gate oxide TFTs with good performance and high stability is necessary for AMOLED display applications [5,6]. A constant positive V_{G_STRESS} is known to induce a rigid, positive shift in the transfer characteristics of a-IGZO TFTs [7–10]. The voltage shift is attributed to the trapping of carriers (electrons) at the active-layer/gate-insulator interface and/or in

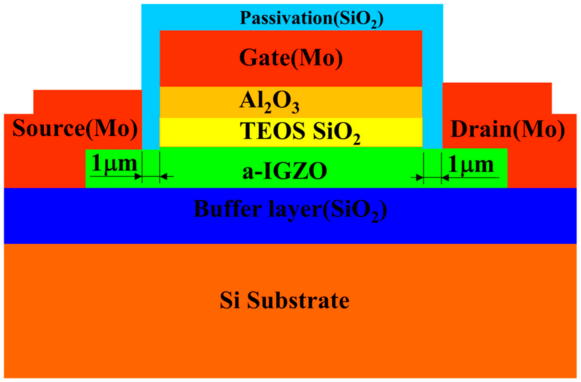
the gate-insulator without the generation of new trap sites or defects. This trapped charge screens the applied electric field, resulting in the reduction of the effective applied V_G and in the positive threshold voltage shift of V_{th}. Similarly, a constant negative gate bias-stress (V_{G_STRESS}) is known to induce hole trapping and/or the generation of doubly ionized oxygen-vacancies (V_O^{2+}), which donate two electrons to the semiconductor conduction band. Either one or both of these events lead to the negative threshold voltage shift of V_{th} [7,11,12]. However, these mechanisms are valid for a-IGZO TFTs without source and drain-offsets, such as the conventional bottom-gate inverted-staggered structures. Mativenga et al. [13] showed the reason why the gate dielectric SiO_2 layer is applied to the various gate bias-stresses (V_{G_STRESS}) of the top-gate structure and why the bias voltage (bias stress) is used in detail. The migration of positive charges towards the offsets lowers the local resistance of the offsets, resulting in an abnormal negative V_{th} under positive V_{G_STRESS}. The negative threshold voltage shift (ΔV_{th}) suggests the induction of excess electrons in the channel, which can only be explained by the bias-induced generation of donor states, such as H^+ or ionized oxygen vacancies. Negative V_{G_STRESS} induces the migration of positive charges from the offsets and towards the region of the channel that is located underneath the gate metal. Consequently, the reduction in on-current under negative V_{G_STRESS} is due to the increase in resistance of the offsets when positive charges migrate away from the offsets. However, oxide-based TFTs typically require large operating voltages (V_G) to achieve high mobility and high on-off current ratios. In addition to using high-mobility semiconductors, operating voltages can be reduced by developing gate dielectric materials capable of large capacitance densities with low leakage currents that have good compatibility for the growth of the semiconductor channel, leading to low trap densities at the semiconductor-gate dielectric interface [14]. With a high dielectric constant (high-k) of 9 and a large band gap of 8 eV, Al_2O_3 is a good candidate to produce gate dielectrics with low leakage and high capacitance density. However, the electrical stability of the a-IGZO TFT with a high-k gate dielectric layer is one of the critical issues, especially under the positive bias stress (PBS) [15,16]. Chang et al. reported the stability of low-temperature a-IGZO thin-film transistors (TFTs), which was evaluated using gate stress voltages of 10 V and −10 V (3.3 MV/cm) for PBS and negative bias stress (NBS), respectively, at room temperature. The initial positive ΔV_{th} was explained by the electron trapping in Al_2O_3, which was also evident in an a-IGZO TFT with a high-temperature atomic layer deposition (ALD) Al_2O_3 dielectric deposited at 250 °C [17]. With the same temperature used for depositing the Al_2O_3 gate dielectric as that in this paper, the electron trapping in traps located at the interface and bulk Al_2O_3 layers was responsible for the initial positive ΔV_{th}.

In this work, top-gate a-IGZO TFT devices with two stacked Al_2O_3/tetraethyl-orthosilicate (TEOS) gate dielectrics were fabricated on silicon wafers, then electrical characteristics and instability, including PBS and NBS tests were measured. Moreover, two stacked dielectrics of Al_2O_3/ TEOS oxide were deposited by using the equivalent capacitance with 100-nm thick TEOS oxide on the patterned IGZO layers to evaluate the electrical characteristics and stability improvement of the a-IGZO TFT devices. By using two stacked dielectrics with 10-nm thick Al_2O_3 and 96-nm thick TEOS oxide can effectively inhibit the increase of interface traps and charge trapping between the IGZO channel and gate dielectrics. In addition, in order to compare the effect of the thickness of Al_2O_3, the deposit of a 20-nm thick Al_2O_3 gate dielectric on the patterned IGZO layers was prepared.

2. Experimental Methods

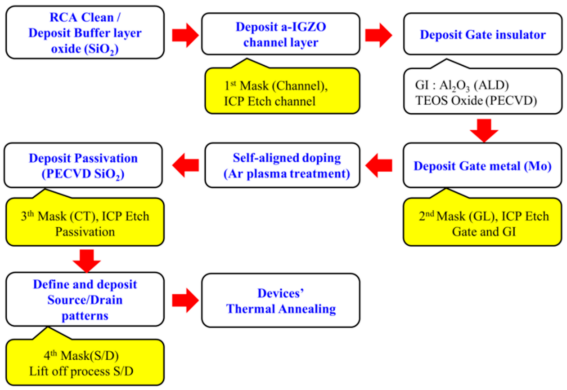
Figure 1a shows the cross-sectional diagram of the top-gate a-IGZO TFT structure used in this study. The devices were fabricated on a 101.6 mm in diameter silicon wafer capped with 500-nm thick thermally grown silicon dioxide (SiO_2) as a buffer layer. First, a-IGZO films with a thickness of 40 nm were deposited through radio frequency (RF) magnetron sputtering by using an IGZO target with an atomic ratio of In:Ga:Zn:O = 1:1:1:4 at room temperature under a fixed deposited power of 100 W. The system based and working pressures were 3×10^{-6} Torr and 5 m Torr, respectively. During sputter, the flow rates of Ar/O_2 were fixed at 50/1 standard cubic centimeters per minute (sccm). The a-IGZO channel layer was patterned to define the channel width by photolithography. Subsequently, dry

etching using inductively coupled plasma (ICP) of a Nasca-20 Plus dry etching system with a mixed gas of Cl_2/Ar = 45/9 sccm was performed under a top electrode's power of 300 W and a bottom electrode's power of 30 W. Then, two stacked dielectrics of Al_2O_3/TEOS oxide were deposited by using the equivalent capacitance with 100-nm thick TEOS oxide on the patterned IGZO layers. First, Oxford plasma-enhanced chemical vapor deposition (PECVD) system was applied to deposit a predetermined TEOS oxide thickness as the first layer of gate dielectrics at 350 °C under a fixed deposited power of 40 W. The system working pressure was 700 m Torr by using a mixed gas of Ar-TEOS/O_2 = 50/300 sccm as the precursors. Subsequently, Ultratech Fiji G2 atomic layer deposition (ALD) system was applied to deposit a predetermined Al_2O_3 thickness as the second layer of gate dielectrics at 250 °C at a deposition rate of approximately 10 nm/1 hr by using $Al(CH_3)_3$ (trimethylaluminum, TMA) and H_2O as sources for Al and O, respectively. In order to compare the effect of the thickness of Al_2O_3, the deposit of a 20-nm thick Al_2O_3 gate dielectric on the patterned IGZO layers was prepared. A 50-nm thick molybdenum (Mo) gate metal was deposited using RF magnetron sputtering at room temperature under a fixed deposited power of 100 W with an Ar gas flow of 20 sccm. The system based and working pressures were 2×10^{-6} Torr and 3 m Torr, respectively. The Mo gate metal was patterned to define the channel length by photolithography. Subsequently, dry etching of the gate metal was performed by using ICP with the same etching condition of the a-IGZO channel layer, followed by gate dielectrics etching with a mixed gas of CF_4 (tetrafluoromethane)/O_2 = 100/5 scan was performed under a top electrode's power of 250 W and a bottom electrode's power of 20 W. After gate etching, argon plasma treatment was performed by using the ICP system to activate the exposed surfaces of the a-IGZO channel layer under a top electrode's power of 300 W and working pressure of 50 mTorr with an Ar gas flow of 150 sccm. A 100-nm thick SiO_2 passivation was deposited using the PECVD system at 300 °C under a fixed deposited power of 20 W. The system working pressure was 1 Torr by using a mixed gas of $SiH_4/N_2O/N_2$ = 8.5/710/161.5 sccm as the precursors. Afterwards, a lithographic step was performed to define the contact area; subsequently, dry etching was performed for SiO_2 by using ICP with the same etching condition of the gate dielectrics etching. Finally, a 100-nm thick Mo source-drain metal using RF magnetron sputtering at room temperature was then formed by a lift-off process in contact with the exposed area of a-IGZO channels. After complete deposition, all the IGZO TFTs samples used in this study were annealed at 300 °C at a working pressure of 5 m Torr for 1 h in an N_2 ambient atmosphere of 40 sccm to form an ohmic contact before electrical measurement. Process charts for each step of top-gate a-IGZO TFTs used in this study are summarized in Figure 1b.



(**a**)

Figure 1. *Cont.*



(**b**)

Figure 1. (**a**) Cross-sectional diagram of a top-gate amorphous indium gallium zinc oxide (a-IGZO) thin-film transistor (TFT) structure. (Source and drain-offsets = 1 μm); (**b**) Process charts for each step of top-gate a-IGZO TFTs used in this study.

I_{DS}–V_{GS} transfer characteristics, which V_{GS} varies from −15 V to +15 V in 0.3 V steps for V_{DS} = 0.1 V, of all devices were executed using an Agilent 4156A precision semiconductor parameter analyzer, and the measurement temperature was maintained at 25 °C.

Devices with a channel width W of 100 μm and channel length L of 5 μm were selected for this experiment. The source and drain-offsets were designed at 1 μm and shown in Figure 1a. The field effect mobility (μ_{FE}) was calculated using

$$\mu_{FE} = \frac{L \times G_{m(max)}}{W \times C_{ox} \times V_{DS}} \quad (1)$$

where C_{ox} is the capacitance per unit area of the TEOS oxide, the transconductance (G_M) = $\partial\, I_{DS}/\partial\, V_{GS}$, and V_{DS} = 0.1 V. The subthreshold swing (S.S.) was taken as the value of $(dlog\ (I_{DS})/dV_{GS})^{-1}$ when the I_{DS} was in the range from 10^{-10} A to 10^{-9} A.

3. Results and Discussions

3.1. Electrical Characteristics of IGZO TFTs with Al_2O_3, Al_2O_3/TEOS Oxide, and TEOS Oxide Gate Dielectrics

Figure 2 shows the representative I_{DS}-V_{GS} transfer characteristics and extracted electrical parameters of a-IGZO TFTs at V_{DS} = 0.1 V and W/L = 100/5 μm with Al_2O_3 (20 nm), Al_2O_3 (10 nm)/TEOS oxide (96 nm), Al_2O_3 (5 nm)/TEOS oxide (98 nm) and TEOS oxide (100 nm) gate dielectrics, respectively. The threshold voltage (V_{th}) is defined as the gate voltage (V_{GS}) when the drain current (I_{DS}) is a constant (10^{-9} × (W/L) A). The measurements were made with more than three samples in each device. The measured gate capacitance per unit area (C_{ox}) of a 100 nm-TEOS oxide was 4.98 × 10^{-8} F/cm^2. Table 1 shows the average values and standard variations of the extracted electrical parameters of a-IGZO TFTs with the investigated gate dielectric conditions, respectively. It is clearly confirmed in Figure 2 that the transfer curves shift positively with increasing Al_2O_3 gate dielectric thickness as a result of the low on-current (I_{on}) within the channel of a-IGZO TFTs with a thicker Al_2O_3 gate dielectric. Park et al. [18] reported that the presence of ALD-based Al_2O_3 increased the turn-on voltage and slightly and adversely decreased the mobility of bottom-gate a-IGZO TFTs with Al_2O_3/SiO_2 double-layered dielectrics. From the summary in Table 1, the TEOS oxide dielectric possessed the largest on/off ratio of > 10^7, a S.S. slope of 1.08 V/decade, a V_{th} of −4.8 V and a μ_{FE} of 4.01 cm^2 V^{-1} s^{-1}. As the Al_2O_3 thickness of Al_2O_3/TEOS oxide dielectric stack increases, both the on-current and off-current decrease, and the transfer curves shift further to larger voltages. However, the S.S. values of top-gate a-IGZO TFTs with two stacked Al_2O_3/TEOS oxide gate dielectrics are larger than the values

of the Al_2O_3 or TEOS oxide single-layer dielectric. The results indicate that two stacked Al_2O_3/TEOS oxide gate dielectrics have more interfacial states than the single-layer dielectric, whether Al_2O_3 or TEOS oxide. For the comparison of the effect of Al_2O_3 thickness, the 20-nm thick Al_2O_3 gate dielectric revealed an on/off ratio of around 10^7, a S.S. slope of 0.49 V/decade, a V_{th} of 1.6 V, and a μ_{FE} of 0.35 cm^2 V^{-1} s^{-1}. The results obviously indicate that the electrical characteristics of a-IGZO TFTs had more positive V_{th}, less S.S., and μ_{FE} corresponding to the increasing Al_2O_3 thickness.

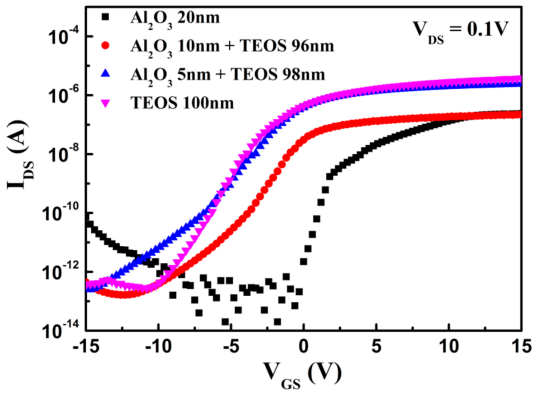


Figure 2. Representative transfer characteristics of a-IGZO TFTs at W/L = 100/5 μm with four kinds of gate dielectrics.

Table 1. The extracted electrical parameters of a-IGZO TFTs at V_{DS} = 0.1 V and W/L = 100/5 μm with four kinds of gate dielectrics. S.S.: subthreshold swing.

Gate Insulator (Thickness)	V_{th} (V)	S.S. (V/Decade)	μ_{FE} (cm^2 V^{-1} s^{-1})	I_{on} (A)	I_{off} (A)
Al_2O_3 (20 nm)	1.6 ± 0.4	0.49 ± 0.07	0.35 ± 0.06	2.40×10^{-7}	2.00×10^{-14}
Al_2O_3 (10 nm)/TEOS (96 nm)	−2.19 ± 0.05	1.37 ± 0.03	0.42 ± 0.04	2.20×10^{-7}	1.65×10^{-13}
Al_2O_3 (5 nm)/TEOS (98 nm)	−3.64 ± 0.14	1.55 ± 0.03	2.47 ± 0.85	2.40×10^{-6}	2.51×10^{-13}
TEOS (100 nm)	−4.8 ± 1.13	1.08 ± 0.09	4.01 ± 1.46	3.80×10^{-6}	2.78×10^{-13}

3.2. Electrical Instabilities of IGZO TFTs with Al_2O_3, Al_2O_3/TEOS Oxide, and TEOS Oxide Gate Dielectrics

Figure 3 show the I_{DS}-V_{GS} transfer characteristics of a-IGZO TFTs at V_{DS} = 0.1 V and W/L = 100/5 μm with the four kinds of gate dielectrics as a function of stress over time under a positive bias-stress of 20 V [19]. The threshold voltage shift (ΔV_{th}), the variety of the sub-threshold swing (ΔS.S.), and the variance ratio of the on-current ($\Delta I_{on}/I_{on}$) of a-IGZO TFTs with four kinds of gate dielectrics after PBS stress for 6400 s are summarized in Table 2. After PBS, the transfer curves of the a-IGZO TFT with the Al_2O_3 (20 nm) dielectric were shifted positively, and the V_{th} was positively increased, as shown in Figure 3a. The increase of V_{th} has been frequently attributed to the charge trapping of accumulated electrons in the channel region at the gate dielectrics. Suresh et al. [20] demonstrated that the application of a gate bias stress to IGZO transparent TFTs with ALD AlO*x* and TiO*x* (ATO) gate dielectrics was found to induce a parallel threshold voltage shift without changing the field effect mobility or the subthreshold gate voltage swing. Table 2 shows the ΔV_{th} of a-IGZO TFTs with the two stacked Al_2O_3/TEOS oxide gate dielectrics are obviously lower than those with the Al_2O_3 or TEOS oxide single-layer dielectric. In addition, by increasing the Al_2O_3 thickness from 0 to 20 nm, the ΔS.S. decreases from 11.32 V/decade to 0.034 V/decade and $\Delta I_{on}/I_{on}$ decreases from −93% to −2.8% after a PBS stress of 6400 s, as shown in Figure 4b,c, respectively. The result of the variability of S.S. shows the increase of the interface traps between the channel and gate dielectrics is obviously inhibited by increasing the Al_2O_3 thickness in the application of top-gate a-IGZO TFTs devices. This is ascribed to the fact that the increase of the Al_2O_3 thickness of Al_2O_3/TEOS oxide dielectric stacks

results in the decrease of excess electrons in the a-IGZO channel and the prohibition of electron traps in the gate dielectric stacks. Therefore, the on-current of a-IGZO TFTs is sustained by increasing the Al_2O_3 thickness of Al_2O_3/TEOS oxide dielectric stacks, as shown in Table 1. However, the PBS results of a-IGZO TFTs with the 20 nm Al_2O_3 gate dielectric show that the largest positive ΔV_{th} is +5.75 V. The positive ΔV_{th} is explained by the electron trapping in Al_2O_3, which was also evident in the a-IGZO TFT with a high-temperature ALD Al_2O_3 dielectric deposited at 250 °C [17]. Electron traps in gate dielectrics result in fewer electrons inside the IGZO channel; therefore, a more positive gate voltage will be applied to accumulate the necessary electrons for conductance in the channel. It is noticeable that the off-current of a-IGZO TFTs with a 20 nm Al_2O_3 gate dielectric is sustained at lower values of around 10^{-13} A after the PBS test for 6400 s. In addition, the PBS results of a-IGZO TFTs with the 100 nm TEOS oxide gate dielectric showed the largest negative ΔV_{th} of −8.8 V, suggesting the induction of excess electrons in the channel, which can only be explained by the bias-induced generation of donor states such as H^+ or ionized oxygen vacancies [12]. However, the lowest ΔV_{th} of −0.42 V of a-IGZO TFTs with 10-nm thick Al_2O_3 and 96-nm thick TEOS oxide shows that the increase of interface traps and charge trapping between the IGZO channel and gate dielectrics is obviously inhibited by using two stacked dielectrics.

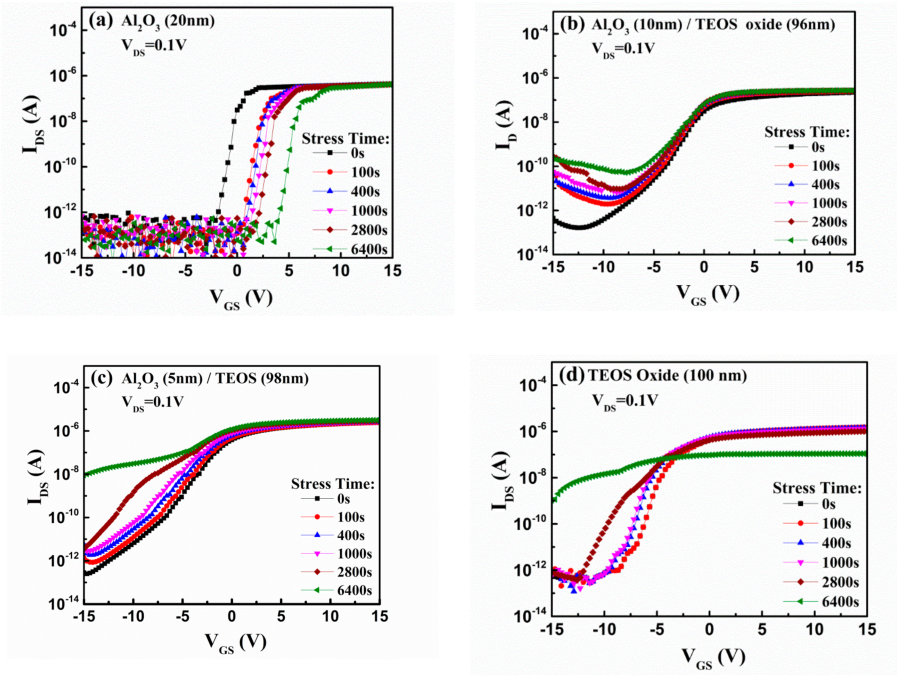


Figure 3. Representative transfer characteristics of a-IGZO TFTs with (**a**) Al_2O_3 (20 nm), (**b**) Al_2O_3 (10 nm)/TEOS oxide (96 nm), (**c**) Al_2O_3 (5 nm)/TEOS oxide (98 nm), and (**d**) TEOS oxide (100 nm) gate dielectrics, respectively, as a function of stress time under a positive bias stress (PBS) (V_{GS} = +20 V).

Table 2. Variations of extracted electrical parameters of a-IGZO TFTs with four kinds of gate dielectrics after PBS stress for 6400 s (V_{GS} = +20 V).

Gate Insulator (Thickness)	ΔV_{th} (V)	ΔS.S.(V/Decade)	$\Delta I_{on}/I_{on}$
Al_2O_3 (20 nm)	+5.75	0.034	−2.8%
Al_2O_3 (10 nm)/TEOS (96 nm)	−0.42	0.41	+25%
Al_2O_3 (5 nm)/TEOS (98 nm)	−2.92	5.53	+33%
TEOS (100 nm)	−8.8	11.32	−93%

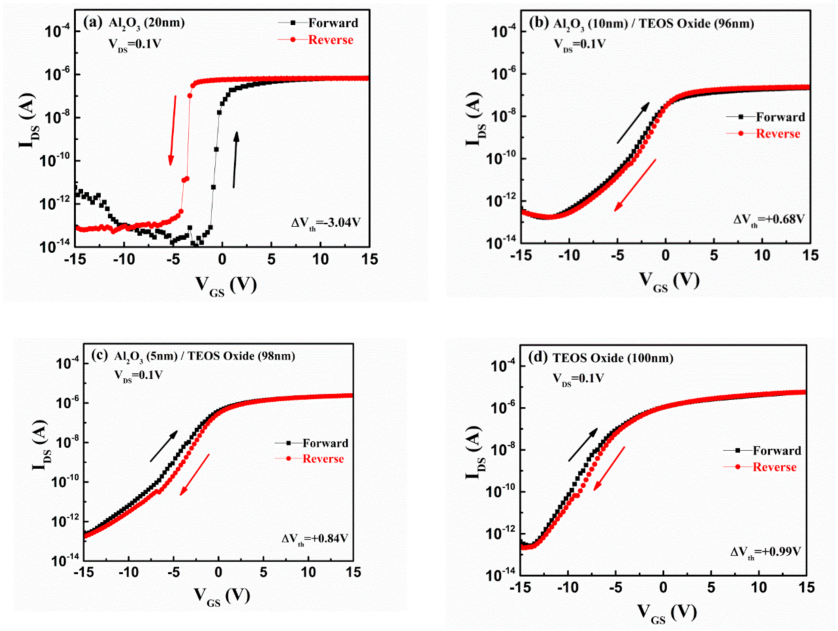


Figure 4. Hysteresis characteristics of a-IGZO TFTs with the respective (**a**) Al_2O_3 (20 nm), (**b**) Al_2O_3 (10 nm)/TEOS oxide (96 nm), (**c**) Al_2O_3 (5 nm)/TEOS oxide (98 nm) and (**d**) TEOS oxide (100 nm) gate dielectrics.

To investigate the effects of the Al_2O_3 and TEOS oxide gate dielectrics and their interface with the a-IGZO active layer, hysteresis sweeps of a-IGZO TFTs with four kinds of gate dielectrics were examined. Figure 4a shows the hysteresis characteristics of the a-IGZO TFT with the 20 nm Al_2O_3 gate dielectric as a function of the gate voltage (V_{GS}) ranging from −15 V to +15 V. The largest threshold voltage shift (ΔV_{th} = −3.04 V) and degradation of subthreshold swing (ΔS.S. = +0.23 V/decade) from the hysteresis loop indicated that more electrons were trapped at or near the Al_2O_3/a-IGZO interface or within the a-IGZO channel layer. Fran et al. reported that the hysteresis voltage abnormally shifted towards the negative direction, and the negative V_{th} shift is due to the carrier creation in the IGZO film, which is mainly from the enhanced control and from using the high-k HfO_2 as the gate insulator [15,21]. In addition, Figure 4b–d show the hysteresis characteristics of a-IGZO TFTs with the Al_2O_3 (10 nm)/TEOS oxide (96 nm), Al_2O_3 (5 nm)/TEOS oxide (98 nm), and TEOS oxide (100 nm) gate dielectrics, respectively. The lower threshold voltage shifts (ΔV_{th}= 0.68 V, 0.84 V, and 0.99 V) and degradation of subthreshold swing (ΔS.S. = −0.03, −0.18, and −0.02 V/decade) calculated from the respective hysteresis loops in Figure 4b–d indicated that few electrons were trapped at or near the TEOS oxide/a-IGZO interface or within the a-IGZO channel layer. The lowest ΔV_{th} of 0.68 V and ΔS.S. of −0.03 V/decade from the hysteresis loop in Figure 4b show that the increase of interface traps and charge trapping between the IGZO channel and gate dielectrics is effectively inhibited by using two stacked dielectrics with 10-nm thick Al_2O_3 and 96-nm thick TEOS oxide. Carlos et al. mentioned that the Si–OH absorbance band was not detected in a typical Fourier transform infrared spectroscopy (FTIRS) study of the deposited TEOS oxide [22]. In general, the effect of hydroxyl (OH) groups in polymeric dielectrics on the organic transistor's hysteresis performance is a strongly proportional relationship [23]. Moreover, Jeon et al. showed that in order to utilize an Al_2O_3 high-k layer in IGZO TFTs, the interfacial SiO_2 layer is crucial to lower both the interface state density and charge trapping by studying the conductance loss versus gate voltage and hysteresis sweep of the metal-oxide-semiconductor (MOS) capacitors with an Al_2O_3 single gate dielectric and Al_2O_3/SiO_2 gate dielectrics [24]. The reasons why the lower ΔV_{th} of a-IGZO TFTS with two stacked Al_2O_3/TEOS oxide gate dielectrics after PBS tests can be explained.

Figure 5 show the transfer characteristics a-IGZO TFTs with the four kinds of gate dielectrics as a function of stress over time under a negative bias-stress of 20 V. ΔV_{th}, ΔS.S., and $\Delta I_{on}/I_{on}$ of a-IGZO

TFTs with the four kinds of gate dielectrics after NBS stress for 6400 s are summarized in Table 3. After NBS test, the transfer curves were shifted negatively, and the V_{th} was decreased. A negative shift of transfer curves was observed due to the hole trapping at either the gate dielectrics or at the IGZO interfaces [12,25]. Table 3 shows that the respective ΔV_{th} and ΔS.S. of a-IGZO TFTs with two stacked Al_2O_3/TEOS oxide gate dielectrics are obviously lower than those with the Al_2O_3 or TEOS oxide single-layer dielectric under the same NBS test. This clearly confirms that the increase of interface traps and charge trapping between the IGZO channel and gate dielectrics is inhibited by adopting two stacked gate dielectrics of Al_2O_3/TEOS oxide on the application of top-gate a-IGZO TFTs devices. The same interpretations were mentioned in the previous PBS stress test. Moreover, $\Delta I_{on}/I_{on}$ decreases by almost 100% for the various gate dielectrics after an NBS of V_{GS} = −20 V for 6400 s. Mativenga et al. [13] mentioned that negative V_{G_STRESS} induces the migration of the positive charges from the offsets and towards the region of the channel that is located underneath the gate metal. The migration of this positive charge from the offset regions significantly reduces the conductivity of the offset regions. This explains the obvious reduction in the on-current of the transfer characteristics in Figure 5a–d. In summary, a-IGZO top gate TFTs with 10-nm thick Al_2O_3 and 96-nm thick TEOS oxide gate dielectrics according to the PBS and NBS tests were shown to have the best electrical stability in comparison to those with the Al_2O_3 or TEOS oxide single-layer dielectrics.

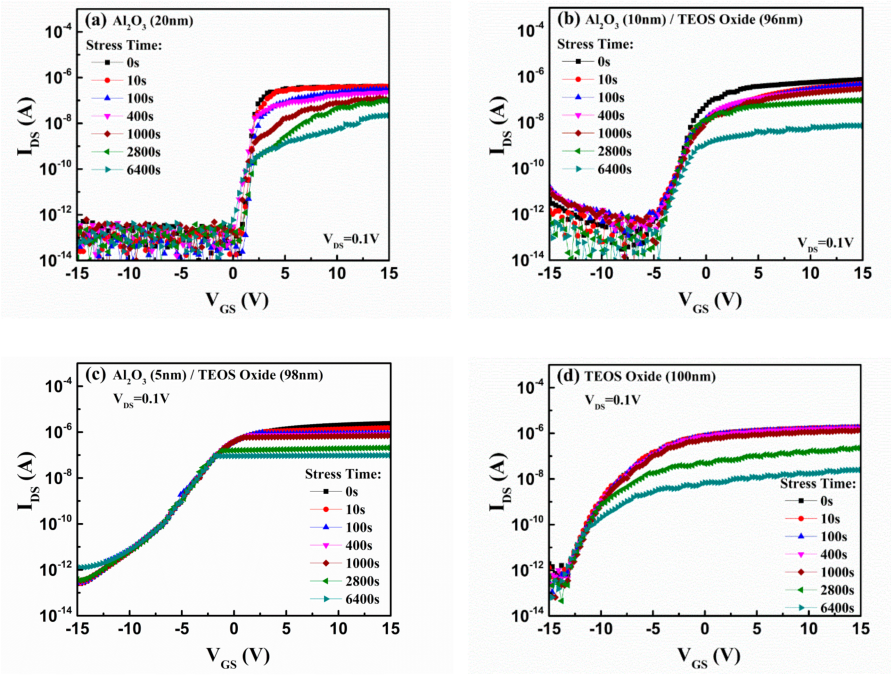


Figure 5. Representative transfer characteristics of a-IGZO TFTs with (**a**) Al_2O_3 (20 nm), (**b**) Al_2O_3 (10 nm)/TEOS oxide (96 nm), (**c**) Al_2O_3 (5 nm)/TEOS oxide (98 nm) and (**d**) TEOS oxide (100 nm) gate dielectrics, respectively, as a function of stress over time under a negative bias stress (NBS) (V_{GS} = −20 V).

Table 3. Variations of extracted electrical parameters of a-IGZO TFTs with four kinds of gate dielectrics after NBS stress for 6400 s (V_{GS} = −20 V).

Gate Insulator (Thickness)	ΔV_{th} (V)	ΔS.S.(V/Decade)	$\Delta I_{on}/I_{on}$
Al_2O_3 (20 nm)	−0.70	1.598	−94.8%
Al_2O_3 (10 nm)/TEOS (96 nm)	−0.14	0.002	−99.1%
Al_2O_3 (5 nm)/TEOS (98 nm)	−0.17	0.007	−96.0%
TEOS (100 nm)	−1.23	1.89	−98.7%

4. Conclusions

Two stacked gate dielectrics of Al_2O_3/TEOS oxide were deposited by using the equivalent capacitance with 100-nm thick TEOS oxide on the patterned IGZO layers to evaluate the electrical characteristics and stability improvement of a-IGZO TFT devices, including PBS and NBS tests. As the Al_2O_3 thickness of Al_2O_3/TEOS oxide dielectric stacks increased, both the on-current and off-current decreased, and the transfer curves shifted to larger voltages. The ΔV_{th} decreased from −8.8 V to −0.42 V after PBS test for 6400 s, which is ascribed to the fact that the increase of the Al_2O_3 thickness on Al_2O_3/TEOS oxide dielectric stacks results in the decrease of excess electrons in the channel and the prohibition of electron traps in gate dielectric stacks. The ΔS.S. decreased from 11.32 V/decade to 0.41 V/decade. Moreover, the lowest ΔV_{th} of 0.68 V and ΔS.S. of −0.03 V/decade from the hysteresis characteristics indicate that the increase of interface traps and charge trapping between the IGZO channel and gate dielectrics is effectively inhibited by using two stacked dielectrics with 10-nm thick Al_2O_3 and 96-nm thick TEOS oxide. Finally, the ΔV_{th} and ΔS.S. values of a-IGZO TFTs with two stacked Al_2O_3/TEOS oxide gate dielectrics were obviously lower than those with the Al_2O_3 or TEOS oxide single-layer dielectrics under the same NBS test. It is believed that top-gate IGZO TFTs by using two stacked dielectrics with 10-nm thick Al_2O_3 and 96-nm thick TEOS oxide dielectrics were verified in peripheral circuits for display applications according to their high stabilities under the PBS and NBS tests.

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