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# New Low-Voltage Driving Compensating Pixel Circuit Based on High-Mobility Amorphous Indium-Zinc-Tin-Oxide Thin-Film Transistors for High-Resolution Portable Active-Matrix OLED Displays

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Abstract: In recent years, active-matrix organic light-emitting diodes (AMOLEDs) has been the most popular display for portable application. To satisfy the requirement for the application of the portable display, the design of the compensating pixel circuit with the low-voltage driving and low-power consumption will be requested. In addition to the circuit with the design of the low-voltage driving, high-mobility thin-film transistors as driving device will be also necessary in order to supply larger driving current at low-voltage driving. Therefore, the study presents a new low-voltage driving AMOLED pixel circuit with high-mobility amorphous indium–zinc–tin–oxide (a-IZTO) thin-film transistors (TFTs) as driving device for portable displays with high resolution. The proposed pixel circuit can simultaneously compensate for the threshold voltage variation of driving TFT ( $\Delta V_{TH_TFT}$ ), OLED degradation ( $\Delta V_{TH_OLED}$ ), and the *I-R* drop of a power line ( $\Delta V_{DD}$ ). By using AIM-Spice for simulation based on fabricated a-IZTO TFTs with mobility of 70 cm<sup>2</sup>V<sup>-1</sup>S<sup>-1</sup> as driving devices, we discovered that the error rates of the driving current were all lower than 5.71% for all input data when  $\Delta V_{TH_TFT} = \pm 1$  V,  $\Delta V_{DD} = 0.5$  V, and  $\Delta V_{TH_OLED} = 0.5$  V were all considered simultaneously. We revealed that the proposed 5T2C pixel circuit containing a high-mobility a-IZTO TFT as a driving device was suitable for high-resolution portable displays.

**Keywords:** active-matrix organic light-emitting diode (AMOLED); amorphous indium–zinc–tin oxide (a-IZTO); compensating pixel circuit; low-voltage driving; portable displays

# 1. Introduction

Active-matrix organic light-emitting diodes (AMOLEDs) have attracted attention in recent years because they have various advantages over conventional liquid crystal displays (LCDs), such as a higher contrast ratio, shorter response time, and wider viewing angles [1,2]. In recent years, low-temperature polycrystalline silicon (LTPS) thin-film transistors (TFTs) have been used in pixel circuits as a backplane technology for AMOLEDs because of their high current driving capability and favorable electrical characteristics [3–5]. However, they have many shortcomings, such as non-uniformity in threshold voltage ( $V_{TH}$ ) and high manufacturing cost [6,7]. Compared with LTPS TFTs, amorphous indium–gallium–zinc oxide (a-IGZO) TFTs have many advantages—including excellent uniformity, favorable stability, and low cost—and have been used as driving devices in



AMOLEDs [8,9]. However, the mobility of a-IGZO TFTs is not sufficiently high for high-resolution and low-voltage driving portable applications [10]. Accordingly, Song et al. [11] exhibited high-mobility amorphous indium–zinc–tin oxide (a-IZTO) TFTs and also reported that the electron transport in a-IZTO channel layer is conducted through extensive s-orbital overlap between metal element of In and Sn, which can provide perfect conductivity path to result in high carrier mobility. Thus, compared with a-IGZO TFTs, a-IZTO TFTs with a-IZTO as active channel are expected to be high-mobility oxide TFTs [12]. The deposition of a-IZTO had been reported by solution or sputtering process [13–15]. Although solution process is a low-cost and large-area process, many defects will be produced in the a-IZTO film due to the solution process, resulting in the decreased mobility. In generally, the sputtering process will be the suitable candidate in order to achieve high carrier mobility [15]. The use of high-mobility TFTs in pixel circuit can supply high driving current. This implies that a smaller device and lower driving voltage can be achieved using a-IZTO TFTs. However, few studies have investigated the use of a-IZTO TFTs as driving devices in AMOLED pixel circuits.

The conventional AMOLED pixel circuit with two transistors and one capacitor suffer from threshold voltage shifts of driving TFT and OLED after a long-term electrical operation, which leads to significant non-uniformity of driving current in each pixel. The current-resistance (*I-R*) drop of power lines generated from each pixel in varying location also causes image degradation [16]. Several pixel circuits that use LTPS TFTs or a-IGZO TFTs as driving devices have been proposed to overcome these problems, including  $V_{\text{TH}}$  variation of the driving TFT, OLED degradation, and the *I-R* drop of power lines ( $V_{\text{DD}}$ ) [17–20]. Kim et al. [17] presented a 5T1C pixel circuit with the enhanced reliability, but it can't compensate the OLED degradation. D. Kim et al. [18] proposed a 4T1C compensation pixel circuit for high resolution display, which is applied to large-size display with high-voltage driving from –5 to 15 V. Nevertheless, the driving voltage of most reported pixel circuits that use a-IGZO TFTs as driving devices is too high to be used in real high-resolution portable applications. Low-voltage driving for the pixel circuit becomes more necessary because the AMOLED display may be used in portable applications.

This study proposed a low-voltage (<5 V) driving pixel circuit with high-mobility a-IZTO TFTs as active driving device to simultaneously compensate for the  $V_{\text{TH}}$  variation of the driving TFTs ( $\Delta V_{\text{TH}_{TFT}}$ ), *I-R* drop of  $V_{\text{DD}}$  ( $\Delta V_{\text{DD}}$ ), and OLED degradation ( $\Delta V_{\text{TH}_{OLED}}$ ). The simulation results revealed that the error rates of the driving current were less than 5.71% in the worst cases, including the  $\Delta V_{\text{TH}_{TFT}}$  of ±1 V,  $\Delta V_{\text{DD}}$  of 0.5 V, and  $\Delta V_{\text{TH}_{OLED}}$  of 0.5 V. With low-voltage driving below 5 V, the proposed 5T2C pixel circuit is suitable for portable applications. To our knowledge, this is the first report in which a high-mobility a-IZTO TFT was used as a driving device in an AMOLED pixel circuit for low-voltage driving and high-resolution portable applications.

#### 2. TFT Fabrication and Characterization

Figure 1a shows the cross section of the BG-TC n-channel a-IZTO TFTs that were fabricated on glass substrate according to the following procedures. At first, a 250 nm thick ITO was deposited by radio frequency (RF) magnetron sputtering with the power of 30 watt at the base pressure of  $5 \times 10^{-6}$  torr and the sheet resistivity of the ITO is 7~10 ohm/square and then ITO film was patterned by photolithography and wet etching to form the gate electrode. Then a 180-nm-thick hafnium dioxide (HfO<sub>2</sub>) was used as the dielectric layer by RF magnetron sputtering in the mixed gas oxygen/argon (O<sub>2</sub>/Ar) = 40% at room temperature. To enhance the quality of dielectric layer and the bulk defects can be obviously decreased, a post deposition annealing at 250 °C for 1 h by the vacuum oven after the dielectric layer deposition. The contact holes were patterned by photolithography. Then a 90-nm-thick a-IZTO was prepared as channel layer by RF magnetron sputtering process using a target with the atomic ratio of In:Zn:Sn = 1:2:2 at room temperature and patterned by wet etching. Afterward, the source and drain electrodes of the 160-nm-thick titanium (Ti) metal was deposited and patterned by thermal evaporation. Finally, the device was annealed by the vacuum oven at 250 °C for 1 h. In this process, the dimension length [width (*W*)/length (*L*)] of all devices are 50/5 µm. The transfer

characteristics of the fabricated devices were measured by using an HP4145B semiconductor parameter analyzer and were shown in Figure 1b. Various device parameters, including the threshold voltage ( $V_{\text{TH}}$ ), the subthreshold swing (S.S.), the maximum on-current ( $I_{\text{ON}}$ ), and the minimum off-current ( $I_{\text{OFF}}$ ) were measured at a drain voltage of  $V_{\text{DS}} = 3$  respectively. The field-effect mobility ( $\mu_{\text{FE}}$ ) is calculated from the maximum value of the transconductance at  $V_{\text{DS}} = 0.1$  V. The fabricated a-IZTO TFT device exhibits a  $\mu_{\text{FE}}$  of 70 cm<sup>2</sup>V<sup>-1</sup>S<sup>-1</sup>, S.S. of 0.18 V/decade,  $I_{\text{ON}}/I_{\text{OFF}}$  of 5.32 × 10<sup>7</sup> and  $V_{\text{TH}}$  of 1.5 V.



**Figure 1.** (a) Schematic cross-sectional diagram and (b) measured transfer characteristics of the a-IZTO TFT.

## 3. Proposed Pixel Circuit Operation

Figure 2a shows the proposed pixel circuit, which comprises four switching TFTs (T1–T4), one driving TFT (T5), and two storage capacitors (C1 and C2). The dimension length [width (*W*)/length (*L*)] of the driving TFT is set to 3  $\mu$ m/10  $\mu$ m, and those of all switching TFTs are set to 3  $\mu$ m/3  $\mu$ m. The capacitances of C1 and C2 are both 0.3 pF. The voltage range of SCAN1, SCAN2, and SCAN3 are from –2 to 5 V. *V*<sub>Ctrl</sub> is set from –3 to 4 V. *V*<sub>DD</sub> and *V*<sub>SS</sub> are set to 4.5 and 0 V, respectively. The *V*<sub>TH</sub> of the OLED is 1.2 V, and the capacitance in the equivalent circuit of the OLED (*C*<sub>OLED</sub>) is 0.3 pF. Figure 2b displays the timing diagram of the control signals. The operating period is divided into four periods: reset, compensation, data input, and emission. The operation of the proposed pixel circuit is demonstrated in detail, as shown in Figure 3.



Figure 2. Proposed pixel circuit. (a) Circuit schematic. (b) Timing diagram.



Figure 3. Cont.



Figure 3. Schematic of circuit operation in various periods with (a) reset (b) compensation (c) data input (d) emission period.

#### 3.1. Reset

In the reset period, all TFTs are turned on by high voltage of all scan lines. The reference voltage,  $V_{\text{REF}}$  (0 V), is provided to Node A by data line. Node B is reset to  $V_{\text{SS}}$  (0 V). Thus, the driving TFT is turned off with the gate-to-source voltages of T5 ( $V_{\text{GS TFT}}$ ) at 0 V.

#### 3.2. Compensation

During the compensation period, T3 is turned off by low voltage of SCAN3, and T1, T2 and T5 are turned on by high voltage of SCAN1 and SCAN2. Because  $V_{\text{Ctrl}}$  switches from  $V_{\text{H}}$  to  $V_{\text{L}}$ , the voltage of Node B ( $V_{\text{B}}$ ) is reduced to below zero to make it start charging by T5 until T5 is turned off, and  $V_{\text{B}}$  turns into  $-V_{\text{TH}_{\text{TFT}}}$ . Thus, the storage voltage of  $C_1$  is the voltage between  $V_{\text{A}}$  and  $V_{\text{B}}$ , which is given by

$$V_{\rm C1} = V_{\rm A} - V_{\rm B} = V_{\rm TH_{\rm T5}} \tag{1}$$

#### 3.3. Data Input

In the data input period, T2 is turn off by the low voltage of SCAN2. The data voltage ( $V_{DATA}$ ) is given to Node A through T1. With effect of coupling capacitors,  $V_B$  is varied as shown in the following equation:

$$V_{\rm B} = -V_{\rm TH\_T5} + V_{\rm DATA} \times \frac{C_1}{C_1 + C_2}$$
(2)

As the result, the storage voltage of  $C_1$  is given by

$$V_{C1} = V_{TH_{T5}} + V_{DATA} \times \frac{C_2}{C_1 + C_2}$$
(3)

Notably, T4 is continuously on during this period to avoid flowing current passing the OLED.

#### 3.4. Emission

During the emission period, T1 and T5 are turned off by low voltage of SCAN1. T2 and T3 are turned on by high voltage of SCAN2 and SCAN3. The OLED current ( $I_{OLED}$ ) can be expressed as the follows [21]:

$$I_{\text{OLED}} = \frac{1}{2}k(V_{\text{GS}} - V_{\text{TH}_{-}\text{T5}})^{2}$$
  
=  $\frac{1}{2}k(V_{\text{TH}_{-}\text{T5}} + V_{\text{DATA}} \times \frac{C_{2}}{C_{1} + C_{2}} - V_{\text{TH}_{-}\text{T5}})^{2}$   
=  $\frac{1}{2}k(V_{\text{DATA}} \times \frac{C_{2}}{C_{1} + C_{2}})^{2}$  (4)

where k is  $\mu \times C_{OX} \times W/L$ . By (4), the OLED current is not dependent of the  $V_{TH}$  of T5/OLED voltage/voltage of power line ( $V_{DD}$ ). Thus, the drop in  $V_{DD}$ , OLED degradation, and  $V_{TH}$  shift of the driving TFT are compensated simultaneously. Besides, the use of high-mobility a-IZTO TFTs in pixel circuit can supply high driving current at low driving voltage. This implies that the same output current of driving TFT can be provided with lower driving voltage. It believes that the circuit can compensate well against  $V_{TH}$  shifts of driving TFT, OLED degradation and *I-R* drop and be driven in low voltage at the same time.

## 4. Results and Discussion

To verify its feasibility, the proposed circuit was simulated using AIM-SPICE and the transfer curve of the TFT were measured and fitted, as presented in Figure 4a. The mobility and  $V_{\text{TH}}$  of the device were 70 cm<sup>2</sup>V<sup>-1</sup>S<sup>-1</sup> and 1.5 V, respectively. Herein, the time taken to input data in each row was set to 3 µs when used for Full-HD+ (2400 × 1080) at the frame rate 120 Hz. Figure 4b plots the simulated transient waveforms of Node A ( $V_A$ ) of the pixels from 1st to 4th rows with different data voltage ( $V_{\text{DATA}} = 0.5, 1, 1.5$  and 2 V) to ensure that the  $V_A$  receive the signals correctly. Figure 4c shows the simulated transient waveforms of  $V_A$  with the same data voltage ( $V_{\text{DATA}} = 1$  V) is put into the pixels for the 1st and 3rd row, a different  $V_{\text{DATA}}$  of 2 V is put into the pixels for the 2nd and 4th rows in data input period. As a result, the data voltage of the 1st row is equal to the 3rd row one and the same result is also gotten for the pixels of the 2nd and 4th row. Thus, Figure 4b,c show this proposed pixel circuit operates correctly in each row. Figure 4d shows the simulated transient waveforms of  $V_{\text{TH}}$  and 4th rows the simulated transient waveforms of the 2nd and 4th row. Thus, Figure 4b,c show this proposed pixel circuit operates correctly in each row. Figure 4d shows the simulated transient waveforms of Node B for this proposed 5T2C pixel circuit when the voltage of the driving TFT ( $V_{\text{TH}}$ -TFT) was varied by ±1 V. As displayed in Figure 4d, the shifted  $V_{\text{TH}}$ -TFT was sensed and stored by this proposed pixel circuit successfully.





**Figure 4.** (a) Measured and simulated transfer curves of the a-IZTO TFT. (b) Transient waveforms of  $V_A$  with first to fourth rows in different  $V_{DATA}$ . (c) Transient waveforms of  $V_A$  with  $V_{DATA} = 1$  V for Row1 and Row3,  $V_{DATA} = 3$  V for Row2 and Row4. (d) Transient waveforms of  $V_B$  of the proposed pixel circuit with ±1 V variation in  $V_{TH_TFT}$ .

Figure 5a plots OLED currents with different  $V_{DATA}$  when  $V_{TH}$  of driving TFT was shifted by ±1 V. Figure 5b shows the current error rates at different gray levels with  $\Delta V_{TH_TFT} = \pm 1$  V. All error rates were lower than 4.97% under different  $V_{DATA}$ , which indicated high immunity against  $V_{TH}$  variation of the driving TFT.



**Figure 5.** (a) Driving currents versus data voltage with  $\pm 1$  V variation in  $V_{\text{TH}_{\text{TFT}}}$ . (b) OLED current error rates with  $\pm 1$  V variation in  $V_{\text{TH}_{\text{TFT}}}$ .

Moreover, the  $V_{\text{TH}}$  of OLED increases when it is operated for a long period [22]. To verify the ability of this proposed circuit to compensate for OLED degradation ( $V_{\text{TH}_OLED}$ ), the  $V_{\text{TH}}$  of the OLED was degraded from 0 to 0.5 V. As illustrated in Figure 6a, when the  $V_{\text{TH}}$  of OLED was increased at high, middle, and low gray levels, the maximum OLED current variation of this proposed pixel circuit was significantly low as 0.1%, 0.18%, and 0.16%, respectively. Therefore, we confirmed that the proposed pixel circuit effectively compensates for OLED degradation. Figure 6b shows the OLED current versus the  $V_{\text{DD}}$  drop. Different  $V_{\text{DATA}}$  were given to observe this influence when  $V_{\text{DD}}$  dropped at different voltages. The maximum current errors at the high, middle, and low gray level were 0.09%, 0.11%, and 0.19% respectively, which revealed the effective suppression of current fluctuation. Figure 7a presents the driving currents versus input data voltages of  $\Delta V_{TH_{TFT}} = \pm 1 \text{ V}, \Delta V_{DD} = 0.5 \text{ V},$ and  $\Delta V_{\text{TH}_{\text{OLED}}}$  = 0.5 V. The maximum current error rate was 5.71%. Therefore, the 5T2C pixel circuit was confirmed to simultaneously compensate for V<sub>TH</sub> variation in the driving TFT, OLED degradation, and *I-R* drops of  $V_{DD}$ . Figure 7b shows the layout of a sub-pixel of this proposed pixel circuit. It satisfied the requirement of 6.6-inch Full-HD + (2400  $\times$  1080) displays with layout area of 32  $\mu$ m  $\times$ 64 μm.



Figure 6. (a) OLED currents of different  $V_{DATA}$  when  $V_{TH_OLED}$  shifts from 0 to 0.5 V. (b) OLED currents of different data voltages when  $V_{\rm DD}$  drops by 0.5 V.

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Figure 7. (a) OLED current versus data voltage with  $V_{\rm TH}$  shift of the driving TFT,  $V_{\rm TH}$  oleD shift of OLED degradation, and I-R drop of V<sub>DD</sub>. (b) Layout of the proposed 5T2C pixel circuit.

The results are presented and compared with the reported AMOLED pixel circuits in Table 1, where circle and cross show the circuits with and without the compensation ability, respectively. Y. Kim et al. [17] presented a 5T1C pixel circuit with the enhanced reliability, but it can't compensate the OLED degradation. Although other reported circuits [18–20] could compensate  $V_{\text{TH}}$  variation of the TFT, OLED degradation, and *I*-*R* drop of  $V_{\text{DD}}$ , only the proposed pixel circuit could operate with low driving voltage (<5 V). The proposed pixel circuit using a-IZTO TFT as a driving device is thus a favorable candidate to simultaneously compensate for  $V_{\text{TH}}$ , *I*-*R* drop, and OLED degradation problems in portable displays with high resolution.

Reference	Driving Voltage (V <sub>DD</sub> & V <sub>SS</sub> )	V <sub>TH_DTFT</sub> Variation Error Rate	OLED Compensation	Eliminate in <i>I-R</i> Drop of V <sub>DD</sub>
This study	$V_{\rm DD} = 4.5 \text{ V}$ $V_{\rm SS} = 0 \text{ V}$	4.97% ( $\Delta V_{\rm TH} = \pm 1$ V)	0	0
[17]	$V_{\text{DD}} = 15 \text{ V}$ $V_{\text{SS}} = 0 \text{ V}$	7% ( $\Delta V_{\rm TH} = \pm 2$ V)	Х	О
[18]	$V_{\text{DD}} = 15 \sim -5 \text{ V}$ $V_{\text{SS}} = 0 \text{ V}$	9.4% ( $\Delta V_{\rm TH} = \pm 2$ V)	О	О
[19]	$V_{\rm DD} = 9.75 \text{ V}$ $V_{\rm SS} = -7 \text{ V}$	$4.14\%(\Delta V_{\rm TH}=+1~{\rm V})$	О	О
[20]	$V_{\rm DD} = 13 \text{ V}$ $V_{\rm SS} = -7 \text{ V}$	4.42% ( $\Delta V_{\rm TH} = \pm 2$ V)	О	О

Table 1. Comparison of proposed and prior pixel circuits.

## 5. Conclusions

A low-voltage driving pixel circuit (<5 V) with high-mobility a-IZTO TFT was proposed for use in AMOLED displays for high-resolution portable applications. The non-uniformity in the display image generated by  $V_{\text{TH}}$  shifts in the driving TFT, *I-R* drops of the power line, and OLED degradation could all be compensated with this proposed pixel circuit. The compensated OLED current error rates were lower than 5.71% for all input data when  $\Delta V_{\text{TH}_{TFT}}$  of ±1 V,  $\Delta V_{\text{DD}}$  of 0.5 V, and  $\Delta V_{\text{TH}_{OLED}}$  of 0.5 V were all considered. Accordingly, we expect the circuit to be highly suitable for high-resolution portable applications with high-mobility a-IZTO TFTs as driving devices.

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