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A 512-Ch Dual-Mode Microchip for Simultaneous Measurements of Electrophysiological and Neurochemical Activities

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Abstract: In the study of the brain, large and high-density microelectrode arrays have been widely used to study the behavior of neurotransmission. CMOS technology has facilitated these devices by enabling the integration of high-performance amplifiers directly on-chip. Usually, these large arrays measure only the voltage spikes resulting from action potentials traveling along firing neuronal cells. However, at synapses, communication between neurons occurs by the release of neurotransmitters, which cannot be measured on typical CMOS electrophysiology devices. Development of electrochemical amplifiers has resulted in the measurement of neurotransmitter exocytosis down to the level of a single vesicle. To effectively monitor the complete picture of neurotransmission, measurement of both action potentials and neurotransmitter activity is needed. Current efforts have not resulted in a device that is capable of the simultaneous measurement of action potential and neurotransmitter release at the same spatiotemporal resolution needed for a comprehensive study of neurotransmission. In this paper, we present a true dual-mode CMOS device that fully integrates 256-ch electrophysiology amplifiers and 256-ch electrochemical amplifiers, along with an on-chip 512 electrode microelectrode array capable of simultaneous measurement from all 512 channels.

Keywords: neurochemical recordings; amperometry; dual-mode amplifier; electrophysiology; fast-scan cyclic voltammetry; microelectrode array; neural interface

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Citation: Mulberry, G.; White, K.A.; Crocker, M.A.; Kim, B.N. A 512-Ch Dual-Mode Microchip for Simultaneous Measurements of Electrophysiological and Neurochemical Activities. *Biosensors* **2023**, *13*, 502. https://doi.org/10.3390/bios13050502

Received: 10 March 2023
Revised: 22 April 2023
Accepted: 25 April 2023
Published: 26 April 2023

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1. Introduction

The detailed study of synaptic function is of paramount importance for a better understanding of neurodegenerative diseases. Many diseases involving motor function, sensory, and cognitive impairments such as Parkinson's Disease, Huntington's Disease, and Alzheimer's Disease are speculated to be caused by dysfunction of the synapses [1–5]. Alzheimer's has been shown to develop in patients with an abnormal buildup and accumulation of amyloid-beta and tau oligomer proteins, which have been shown to harm the communication between synapses as well as neuronal loss [1,6,7]. Parkinson's and another neurodegenerative disease, Lewy Body Dementia, are thought to develop from a similar underlying process through the buildup of alpha-synuclein and/or tau oligomers [8–10]. This degradation in synaptic function is common to all of these neurodegenerative diseases and is even noticed in many preclinical cases, suggesting the need for early detection of degradation [4,11,12].

There are primarily two types of electrical measurement used when studying neuronal activity: electrophysiology and amperometry. Electrophysiology is a broader term but within the study of the brain, it generally refers to measurements of voltage, particularly the measurement of Action Potentials (AP) and local field potential (LFP). An AP is also known as a "spike" or a "nerve impulse" and is caused when a neuron "fires" and causes a depolarization and repolarization to travel along the neuron's axon. Amperometry involves the measurement of electrical current by fixing the potential of an electrode held near an active cell and measuring the current produced by the oxidation of neurotransmitters with

a transimpedance amplifier (TIA). The process of secretion of neurotransmitters is known as exocytosis and is heavily studied using amperometry. Traditionally, researchers in a typical study perform either amperometry measurements or electrophysiology measurements, seldom both simultaneously. Additionally, these measurements are typically low throughput, involving in many cases only single electrodes.

Recent developments in the field have begun to use CMOS technology to integrate large numbers of amplifiers and microelectrode arrays (MEA) onto a single chip for high throughput electrochemical measurements [13,14]. Presently, there is no current technology that exists at microscopic scales to measure both modes of electrical activity involved in neurotransmission. Without this dual-mode capability, it is difficult to accurately monitor the dynamics of neuronal degradation. Most current studies are relying on measurements using microelectrode arrays to measure action potentials as they travel along axons to synapses. However, when studying Parkinson's disease (PD), synapse disfunction has been seen to precede the common features of PD, such as complete synapse failure and neuronal loss, suggesting a need for the measurement of neurochemical activity when studying neurodegenerative diseases [15–18]. Furthermore, action potentials themselves are caused by secretions of neurotransmitters near the synapses of the neurons [19–21]. Thus, measuring action potentials alone, as is commonly done, is an indirect measurement which is not seeing the complete picture. If a complete understanding of the normal and dysfunctional neurotransmission is to be developed, a technology is needed that can measure neurotransmitter release and action potentials simultaneously and at a small enough scale to actually capture relevant information at a statistically significant quantity. The integrated circuit presented in this work is the first of its kind being presented to solve these problems.

Many CMOS chips have been presented that focus on providing a high-density MEA capable of performing electrophysiology [13,22–28]. Unfortunately, since they are performing electrophysiology, typically using a transconductance amplifier (TCA), they are incapable of measuring neurotransmitter release. However, there has been at least one recently-reported high-density CMOS MEA device that includes a small number of electrochemical amplifiers to measure neurotransmitter release in addition to typical electrophysiology measurements [29]. This device has a large number of electrodes (59,760), but can only measure from a selected portion of them (2048) at a time. Additionally, it only contains 28 amplifiers which have a noise performance on the order of 100 s of pA_{RMS} for measuring neurotransmitter release. The low amplifier count and poor noise performance make this device incapable of measuring neurotransmitter release at a similar spatiotemporal resolution as its electrophysiology capability.

In this paper, we present a new dual-mode chip that expands on the commonly studied high-density CMOS MEA by treating neurochemical detectors with the same importance as electrophysiological detectors in an effort to provide a useful tool for the study of neurochemical effects in parallel with traditional electrophysiology effects so the interrelatedness can be better understood. The presented chip can simultaneously measure action potential propagations and neurochemical secretions at the synapses. Neurons can be measured using the dual-mode chip as demonstrated in Figure 1, which shows a cross-sectional view of a pair of neurons sitting above the surface of the device. By integrating both neurochemical and action potential amplifiers onto a single chip, presynaptic action potentials, neurotransmitter release at the synapse, and postsynaptic action potentials can be observed simultaneously. If a large quantity of both modalities of amplifier are arranged into a large array, then the flow of action potentials and neurotransmitters across complex neuronal networks can be studied (Figure 1). The dual-mode device presented in this paper is capable of measuring both neurotransmitter release and action potentials from 512 on-chip electrodes simultaneously and at the same spatiotemporal resolution. This device enables the study of the dynamic relationship between neurotransmission and action potential propagation using a single CMOS chip and MEA. Expanding on our previous work with high-density CMOS electrochemical MEAs [14,30], we also add

additional functionality to enable on-chip fast-scan cyclic voltammetry (FSCV). In Section 2 we describe the overall concept and design of the dual-mode chip. Next, details of the circuitry used in the electrochemical amplifier as well as its performance will be discussed in Section 3. The design and function of the electrophysiology amplifier are presented in Section 4. In Section 5, information about the dual-mode CMOS chip's layout and fabrication are provided. Finally, conclusions and discussions related to the dual-mode chip will be given in Section 6.

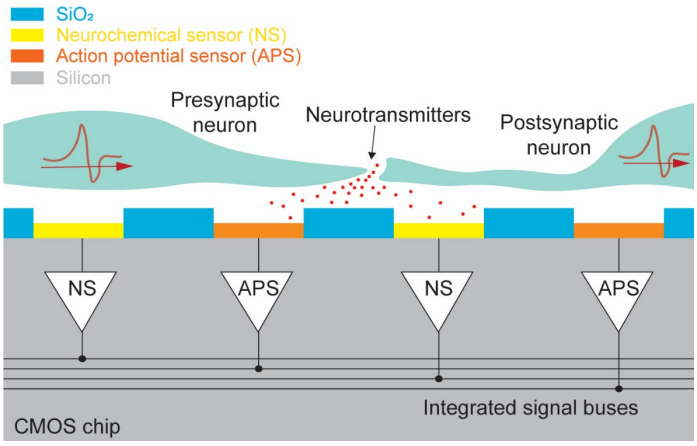


Figure 1. Conceptual view of the dual-mode device. Cross-section showing simultaneous measurement of presynaptic action potential, neurotransmitter release at synapse, and postsynaptic action potential using dual-mode CMOS chip.

2. Dual-Mode Chip Concept

The dual-mode concept is to simultaneously record neurotransmitter release and action potentials with a high electrode count, and high-density array. To create a large array of amplifiers, their design must be compact and scalable. This section describes simplified models of the electrochemical and electrophysiology amplifiers used in the dual-mode chip to achieve the goals of measurement of both signal modalities while enabling a high electrode count without sacrificing performance. More detail about the actual amplifier designs used on the fabricated dual-mode chip as well as their measured performance will be provided in the subsequent sections.

2.1. System Design

The dual-mode chip integrates three main functional blocks: a microelectrode array, 256 TIA neurochemical amplifiers, and 256 TCA electrophysiology amplifiers (Figure 2). Each and every electrode on the MEA is connected to its own dedicated amplifier. The approach of having dedicated amplifiers for each electrode has several benefits over multiplexed electrodes at the input of the amplifiers. The main benefit is that the bandwidth requirements of the amplifiers are greatly reduced. For example, if a hypothetical system were to be made using amplifiers each measuring 16 electrodes, then for the same per electrode sample rate, the required bandwidth of such an amplifier must be at least 16 times higher than a system using 16 separate amplifiers with much narrower bandwidth. The relatively small bandwidth needed for measuring neural signals is straightforward to obtain with smaller low power amplifiers. Additionally, good noise performance is much simpler to achieve in the lower bandwidth amplifiers than in amplifiers which must run at high speed. Using multiplexing, all 512 amplifiers are fed to class AB output buffers for simultaneous parallel measurement using an off-chip data acquisition system [31]. The chip also contains additional circuitry for controlling the time-division multiplexing scheme, programming of SRAMs for gain control and testing modes, as well as on-chip current sources for electroplating of the electrodes with a suitable electrode material such as platinum black for potential measurements.

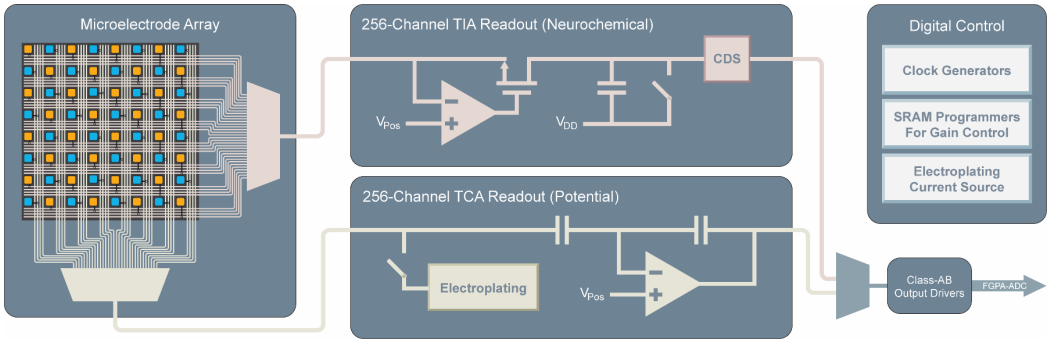


Figure 2. Block diagram of the dual-mode chip. Simultaneous measurement is enabled by multiplexing 256 parallel channels of neurochemical amplifiers and 256 parallel channels of electrophysiology amplifiers each of which is connected to its own electrode on a high-density microelectrode array. Additional on-chip circuitry controls the multiplexing, allows for electroplating of the electrodes, programs amplifier gain settings, and drives the off-chip ADCs.

2.2. Fundamental Transimpedance Amplifier Concept

The dual-mode chip's electrochemical amplifier is based on our half-shared TIA design (Figure 3) [32]. This circuit converts electrode current by clamping the electrode voltage at a known level, V_{pos}, and integrating the current onto a capacitor. Before reaching C_{int}, the current must pass through the cascode transistor M_2 and the current mirror formed by M_3 and M_4. The current mirror is designed so that the W/L ratio of M_3 can be changed which causes more or less current to flow in C_{int} for the same electrode current, thus providing multiple transimpedance gain settings. The transistor M_4 is part of a current mirror that serves two purposes. The first is to add an offset current to the measurement so that both oxidation and reduction currents can be measured by the amplifier while maintaining the same direction of current flowing through M_2 and C_{int}. The second is to enable accurate calibration of TIAs. A multiplexer (M_6 and M_7) is used to read out the integrated voltage. At the sample rate (f_s), the integration capacitor is reset using M_5 by discharging the capacitor to V_{reset}. The gain can be determined by the following expression:

$$Gain\ [A/V] = \frac{C_{int}}{t_{int} \times div} \tag{1}$$

where C_{int} is the value of the integration capacitor, t_{int} is the integration period ($1/f_s$) and *div* is the current mirror divider ratio. Because of the integration and sampling, the expected frequency response will correspond to the *sinc()* function [32].

2.3. Fundamental Transconductance Amplifier Concept

The electrophysiology amplifier (Figure 3) is based on a neural amplifier design that is commonly used with some simplifications [33]. It uses capacitors C_i and C_f to AC couple the electrode and to set the gain of the amplifier. Resistor R_f is a high-value resistance to provide DC stability for the amplifier. The output of the TCA drives a load capacitor C_L to produce an output voltage. Some important design equations for this amplifier are given below for the gain and bandwidth:

$$Gain\ [V/V] = \frac{C_i}{C_f} \tag{2}$$

$$BW \propto \frac{1}{Gain \cdot C_L} \tag{3}$$

Like the TIA, an output multiplexer (M_9 and M_{10}) and an electroplating current mirror (M_8) is included in the design.

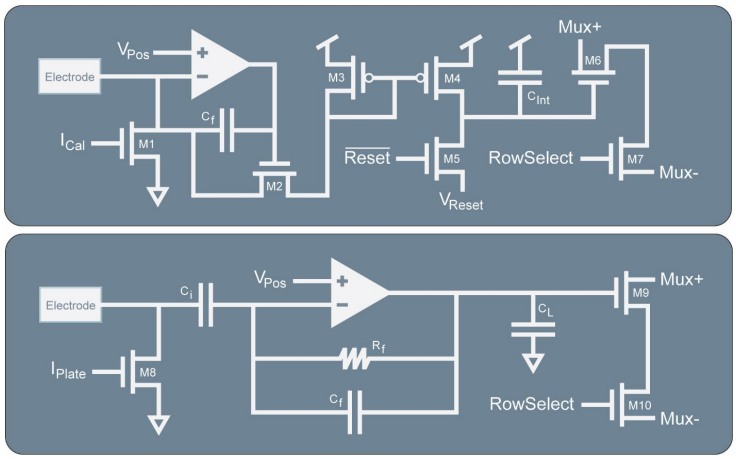


Figure 3. Simplified schematics of the TIA and TCA. The integrating TIA is based on a regulated cascode amplifier that integrates electrode current onto C_{int} through the adjustable ratioed current mirror formed by M_3 and M_4 to enable different gain settings. The TCA is a capacitive feedback design to measure electrode potential. The output current is passed to C_L to produce a voltage. Both the TIA and TCA include output multiplexing circuitry and current mirrors on the electrodes to enable electroplating of suitable electrode materials such as gold, platinum black, or Ag/AgCl.

3. Electrochemical Amplifier

The electrochemical amplifier that is used in the dual-mode chip builds on our previously published amplifier design which is one of the highest performing transimpedance amplifier arrays published [14,30–32,34]. This topology is designed specifically for high-density applications with low-noise requirement, and it showed no crosstalk between the amplifiers [32]. Also, the noise for this topology has been thoroughly characterized and tested [32]. For the dual-mode chip, the electrochemical amplifier can operate two modes of operation, amperometry and cyclic voltammetry. Cyclic voltammetry (CV) is a method to study neurotransmitters as well as other electroactive molecules. FSCV or fast-scan cyclic voltammetry can achieve higher temporal resolution and sensitivity compared to slow-scan CV [35–38]. We have been able to successfully perform traditional slow-scan CV using our previous device [34] however, to implement FSCV, a wide dynamic range and flexible gain settings are added to the dual-mode chip's electrochemical amplifiers. This section will describe the circuitry used in the electrochemical amplifiers, how FSCV is implemented, and give some performance results from the fabricated device.

3.1. Amperometry Mode

Amperometry mode for the electrochemical amplifier is implemented using a design that we have previously reported [14,30–32,34]. The portion of the schematic to the left of the dashed line in Figure 4a shows the reused elements of the electrochemical sensor. Briefly, this circuit is an integrating transimpedance amplifier comprised of a half-shared op-amp [32] with a cascode transistor M_9, where electrode current is integrated onto C_{LoG}, or onto the parasitic capacitance of the node at the drain of M_9, depending on the amperometry gain setting (changed by M_8 and LoG). The potential of the electrode is maintained at V_{pos} due to the op-amp's feedback through the cascode transistor. The addition of M_{10}, M_{12}, and M_{15} allows disconnection of the reset transistor M_4, disconnection of the output multiplexer circuitry, and connection to the additional FSCV mode circuitry to the right of the dashed line. More information on the multiplexing operation is presented in Section 3.4.

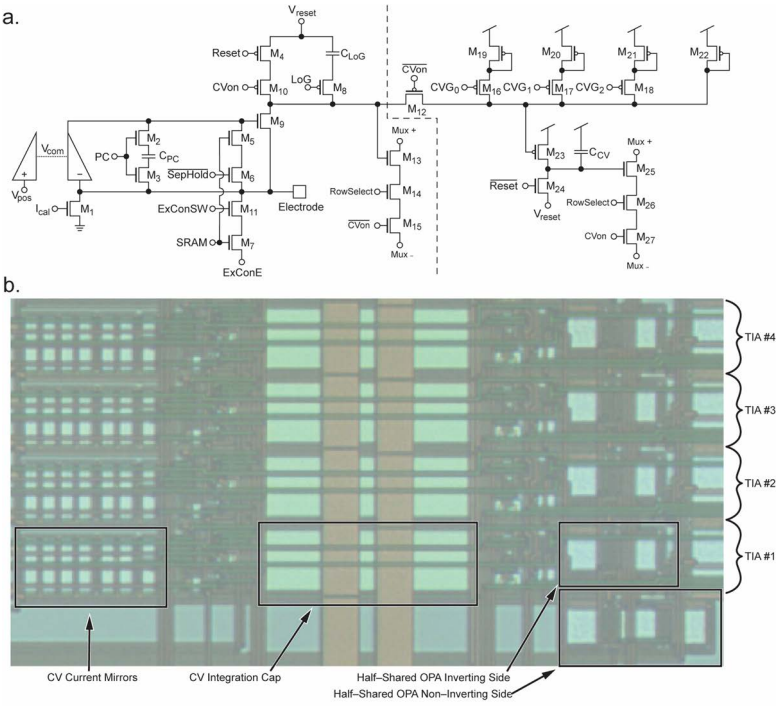


Figure 4. Details of the TIA's design. (**a**) Schematic of the TIA. To the left of the dashed line, the schematic is similar to our previously reported TIA design and is used for amperometry. The circuitry to the right of the dashed line implements FSCV functionality using the current mirrors formed by M_{19}–M_{22} and M_{23} with integration cap C_{CV}. Switches M_{16}–M_{17} enable multiple gain settings for FSCV mode. (**b**) Image of a group of 4 half-shared TIAs on the fabricated chip. Four amplifiers share the non-inverting side of the OPA to conserve space [32]. The CV integration cap and CV current mirrors occupy a considerable die area.

3.2. Fast Scan Cyclic Voltammetry Mode

FSCV measurements require a wide dynamic range in the range of µA rather than pA to nA seen in amperometry, because of the large displacement current coming from the double-layer capacitance of the electrode-electrolyte interface. In the dual-mode chip, adjustable ratio current mirrors and a larger integration capacitor are included to provide a significantly higher dynamic range which corresponds to lower gain settings. These changes are shown in Figure 4a to the right of the dashed line. M_{10} is added to enable switching to CV mode when CV_{on} is set high. This disables the reset signal from resetting the capacitance at the drain node of M_9. M_{12} is enabled when CV_{on} is high, connecting the original circuit to the new additional CV mode circuity. Conceptually, M_{19}–M_{22} form a ratioed current mirror with M_{23} whose ratio is programmable by enabling or disabling the signals CVG_0–CVG_2. The current is then integrated onto the capacitor C_{CV} which is reset by M_{24}. The output is sent to the output buffers through output mux transistors M_{25}–M_{27}. This configuration allows for the two original TIA's gain settings set by the parasitic capacitance at the drain node of M_9 or the integration capacitor C_{LoG}, as well as new lower gain settings for FSCV. With these current mirrors and larger integration capacitor, FSCV mode allows for gain settings in the range of ~0.48 to 1.6 V/µA which greatly extends the range into levels more suitable for FSCV, where signals typically have amplitudes in the range of a few microamperes. A photomicrograph of a group of four TIAs fabricated on-chip is shown in Figure 4b. Four amplifiers are shown to demonstrate the space-saving half-shared structure of the op-amps along the right side of the layout. The large C_{CV} integration cap is seen in the middle of the layout. This capacitor would need to be made considerably larger to achieve the same gains if not for the next largest group of components, the current mirrors for FSCV mode, which can be seen on the left. The total size of an individual amplifier is 180.15 µm by 20.45 µm, or ~3070 μm^2.

3.3. Electrochemical Amplifier Performance

The transimpedance gain of individual TIAs can be directly measured by injecting known currents into the built-in I_{cal} current mirrors (M_1) and plotting the difference in output voltage against the input currents. For amperometry mode, current was input ranging from 0 to 9 nanoamperes, resulting in a voltage difference ranging from 0 to ~1 volt (Figure 5a). The measurements of the entire collection of 256 amplifiers are plotted in blue with dots for the mean and error bars showing the standard deviation. A linear fit is performed to show the gain of the TIA (red line, excluding the last three data points where the gain starts to taper off due to the TIA's dynamic range), resulting in a transimpedance gain of 150 mV/pA at a sample rate of 40 kHz. Notice that the gain tapers off at currents above ~7 nA, this is caused by limitations of the output buffers. Data points above this level are excluded from the linear fit.

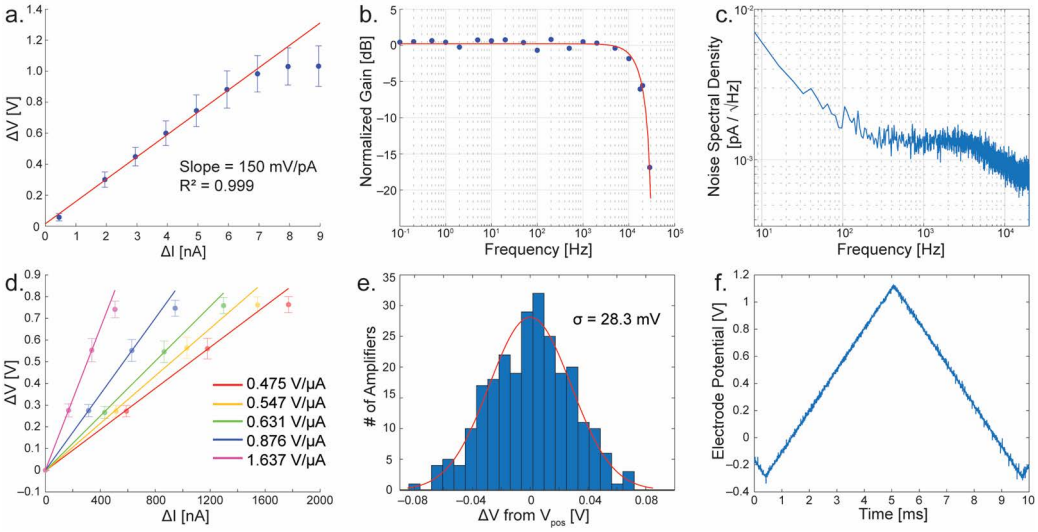


Figure 5. Measurements of the TIA with amperometry and FSCV modes. (**a**) Gain calibration in amperometry mode ($p = 2.6 \times 10^{-7}$, $R^2 = 0.999$). (**b**) Frequency response at measured points (blue) with *sinc()* response best fit (red). (**c**) Noise spectral density of a typical TIA. (**d**) Gain calibration of the multiple FSCV gain settings (1.637 V/μA, $p = 1.22 \times 10^{-3}$, $R^2 = 0.999$; 0.876 V/μA, $p = 1.46 \times 10^{-3}$, $R^2 = 0.999$; 0.631 V/μA, $p = 9.23 \times 10^{-3}$, $R^2 = 0.999$; 0.547 V/μA, $p = 1.23 \times 10^{-2}$, $R^2 = 0.999$; 0.475 V/μA, $p = 1.05 \times 10^{-2}$, $R^2 = 0.999$). (**e**) Histogram showing the mismatch distribution between all 256 TIAs in FSCV mode. (**f**) Measured electrode potential of an amplifier in FSCV mode. The scan rate is 300 V/s. Error bars are all in standard deviations.

The frequency domain characteristics of the TIA are also studied (Figure 5b,c). A frequency response was obtained by enabling the external electrode connection to an amplifier and injecting a small sine wave into the electrode through a resistor to produce a known AC current. In Figure 5b, the result of this measurement is shown. Blue points are the measurements at test frequencies ranging from 0.1 Hz to 30 kHz. The response of the integrating amplifier is known to correspond to a *sinc()* function [32], and by fitting to this response produces a cutoff frequency of ~10.3 kHz. A noise spectral density is presented in Figure 5c. Integrating under this curve yields a total noise of 4.51 pA_{RMS}. Among the current-based amplifiers, the TIA design based on the current integration achieved one of the best noise performances [32]. The noise analysis on a non-stationary circuit, such as the one shown here, cannot be done with conventional frequency-domain noise analysis since the simulator assumes stationary behavior. We have previously developed an approach to convert the non-stationary circuit (current integrating circuit) into a stationary circuit, and subsequently apply the reflection of the integrating effect in the frequency domain [32]. To do this, the circuit's integrating capacitor was first converted to a resistor with the identical transimpedance value ($R = C/t_{int}$) and the noise analysis was performed on the resistive

TIA. Once the noise characteristic in the frequency-domain is acquired, we apply the integrating effect. Since the integration is a rectangular function with a window of period t_{int}, the Fourier transformation of the rectangular function is given as a *sinc()* function. Therefore, the combined noise characteristic was the resistive TIA's noise multiplied by the the *sinc()* function in the frequency domain. The resulting noise of this integrating TIA is consistent with Figure 5c in which the corner frequency is mainly governed by the *sinc()* function [32].

For FSCV mode, there are five distinct gain settings. Each of these was measured in the same way as previously mentioned for amperometry mode. In Figure 5d these measurements are shown where each setting is plotted as its own colored points and fit line. The resulting gain settings range from ~0.48 to 1.6 V/µA when sampled at 40 kHz. To determine the matching characteristics of the current mirrors, I_{cal} is grounded to ensure zero input current, and the resulting output voltage is subtracted from the V_{pos} level, a histogram is plotted and shown in Figure 5e. By fitting the data of all 256 channels, the standard deviation of this mismatch is 28.3 mV. Because the measurements are calibrated to a zero current input (Figure 5d), the voltage mismatch between channels does not harm the performance of the amplifier until the mismatch becomes so great as to limit the dynamic range of the circuit. To implement FSCV, it is necessary to stimulate the electrode potential. Typically, this is performed using a triangular-shaped pulse with a ramp rate of 300 V/s with an amplitude range up to 1.7 V [35,36]. To ensure that the amplifier is indeed capable of driving the electrode at such speeds, a triangle wave with a ramp rate of 300 V/s and amplitude of 1.4 V was applied to V_{pos} while the electrode potential was measured using ExConE. The result is shown in Figure 5f. The amplifier shows no distortion of the triangular shape at these speeds and amplitude ranges. A comparison of the TIA to other reported designs is presented in Table 1. Compared to other designs, the TIAs presented in the dual-mode chip have one of the highest number or parallel channels versus the number of on-chip electrodes. Half of the MEA's electrodes are dedicated to the TIAs and each electrode is measured at the full sample rate, enabling a high spaciotemporal measurement from a large neuronal network.

3.4. Multiplexing

To facilitate the integration of hundreds of amplifiers onto a single chip the outputs of the amplifiers are multiplexed together. The multiplexing circuitry in the circuit consists of M_6–M_7 and M_9–M_{10} (Figure 3), M_{13}–M_{15} and M_{25}–M_{27} (Figure 4a), and the circuit shown in Figure 6a. Focusing on the simplified schematics in Figure 3, the multiplexing circuit works by mirroring the gate voltage at M_6 or M_9 when the corresponding switch (M_7 or M_{10} respectively) is turned on. In Figure 4a, the schematic of the multiplexer circuit is shown. Here, M_9 and M_{10} represent the M_9 and M_{10} seen in Figure 3b. Assuming that the RowSelect signal on the gate of M_{10} is set to high, current can flow from the node labeled Mux+ to Mux−. Effectively, a basic unity-gain op-amp structure is created with M_1–M_5 and M_9–M_{10}. The input pair is M_3 and M_9 where M_3 is the inverting input and M_9 is the noninverting input. Because the gate of M_3 is tied to the output, a unity gain is achieved. M_4 is included to balance the effect of M_{10} (or any M_k.) A different amplifier can be selected for readout by any number of M_j and M_k devices, in the dual-mode chip there are 16 of these shared in each output multiplexer. In the electrochemical amplifiers there are two possible output nodes depending on the mode of operation (amperometry or FSCV mode.) The corresponding switch is turned on (M_{15} or M_{27} from Figure 4a) to select the desired mode.

Table 1. Comparison to similar amplifiers.

Chip									Current Amplifiers							Voltage Amplifiers					
Reference	Year	Dual-Mode	Process Node	Die Size	Voltage	Total Power	Electrodes	Electrode Pitch	Parallel Channels	Size/Ch	Sample Rate	Bandwidth	Noise (RMS)	Current	Power/Ch	Parallel Channels	Size/Ch	Sample Rate	Bandwidth	Noise (RMS)	Current	Power/Ch
[33]	2003	No	1.5 µm	2.2 × 2.2 mm	5 V	-	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	6	160,000 µm^2	-	7.5 kHz	2.2 µV	8 µA	40 µW
[39]	2016	No	0.13 µm	9 × 5 mm	1.8 V	-	966	~70 µm	N/A	N/A	N/A	N/A	N/A	N/A	N/A	384	-	30 kHz	10 kHz	6.4 µV	-	49.1 µW
[40]	2017	No	0.35 µm	-	-	-	36	25 µm	N/A	N/A	N/A	N/A	N/A	N/A	N/A	36	70,000 µm^2	25 kHz	300 Hz–10 kHz	2.2 µV	-	30 µW
[41]	2020	No	90 nm	32.5 × 25.1 mm	-	4420 mW	236,880	11.72 µm	N/A	N/A	N/A	N/A	N/A	N/A	N/A	33,840	-	10 kHz	10 kHz	5.5 µV	-	-
[42]	2020	No	0.18 µm	5.6 × 5.6 mm	-	-	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	32	245,000 µm^2	-	200 Hz	1.49 µV	-	-
[43]	2021	No	0.18 µm	6 × 9 mm	-	-	19,584	18.0 µm	N/A	N/A	N/A	N/A	N/A	N/A	N/A	19,584	-	11.6 kHz	5 kHz	10.4 µV	-	5.9 µW
[44]	2022	No	-	5.9 × 5.24 mm	-	30.7 mW	24,320	17.7 µm	N/A	N/A	N/A	N/A	N/A	N/A	N/A	380	-	20 kHz	300 Hz–10 kHz	5.4 µV	-	-
[23]	2015	Yes	0.18 µm	5 × 2.65 mm	1.8 V	3.21 mW	200 *	200 µm *	100	30,000 µm^2	20 kHz	110 Hz–10 kHz	480 fA **	-	12.1 µW	100	30,000 µm^2	20 kHz	10 kHz	4.07 µV	N/A	9.1 µW
[29]	2017	Yes	0.18 µm	12 × 8.9 mm	-	86 mW	59,760	13.5 µm	28	40,000 µm^2	20 kHz	16 kHz	120 pA	-	178 µW	2048	-	20 kHz	300 Hz–10 kHz	5.4 µV	-	16 µW
[24]	2017	Yes	0.13 µm	3 × 1.85 mm	-	-	1024	58 µm	4	8000 µm^2	-	700 Hz	56 pA	-	-	1024	-	-	300 Hz–6 kHz	7.1 µV	~3–30 µA	-
[45]	2020	Yes	0.18 µm	~10 × 20 mm	-	-	4096	20 µm	4096 ***	25,000 µm2	9.4 kHz	4.7 kHz	~1 pA	-	-	4096 ***	25,000 µm^2	9.415 kHz	4.7 kHz	20 µV	-	-
This Work	2022	Yes	0.35 µm	5 × 5 mm	3.3 V	11.5 mW	512	16 µm	256	3070 µm^2	40 kHz	10.3 kHz	4.51 pA	4.8 µA	16 µW	256	11,000 µm^2	40 kHz	0.2 Hz–10 kHz	24.9 µV	8 µA	26 µW
[46]	2006	No	0.5 µm	-	5 V	-	25	15 µm	25	525 µm^2	-	2 kHz	~110 fA	-	1 µW	N/A	N/A	N/A	N/A	N/A	N/A	N/A
[13]	2012	No	0.5 µm	3 × 3 mm	5 V	-	100	~50 µm	100	900 µm^2	2 kHz	~1 kHz	~100 fA	-	-	N/A	N/A	N/A	N/A	N/A	N/A	N/A
[47]	2015	No	0.6 µm	-	-	-	1,048,576	3.6 × 4.45 µm	-	-	-	10 kHz	21.8 pA	-	-	N/A	N/A	N/A	N/A	N/A	N/A	N/A
[48]	2018	No	0.5 µm	2.5 × 2.5 mm	-	2.1 mW	100	-	25	60,000 µm^2	-	11.5 kHz	7.2 pA	-	-	N/A	N/A	N/A	N/A	N/A	N/A	N/A
[35]	2018	No	0.5 µm	-	5 V	4.85 mW	64	-	64	1350 µm^2	10 kHz	10 kHz	443 fA	-	13.5 µW	N/A	N/A	N/A	N/A	N/A	N/A	N/A
[32]	2019	No	0.35 µm	5 × 5 mm	-	12.5 mW	1024	-	1024	90 µm^2	10 kHz	4.4 kHz	415 fA	-	-	N/A	N/A	N/A	N/A	N/A	N/A	N/A
[49]	2022	No	0.18 µm	25 mm^2	-	58.8 mW	131,072	10 µm	131,072	-	0.062 Hz	-	-	-	-	N/A	N/A	N/A	N/A	N/A	N/A	N/A

* Electrodes are off-chip; ** noise is filtered to <110 Hz; *** amplifiers are configurable for either current or voltage.

In the multiplexers, the schematic is identical to that shown in Figure 6a except for an additional M_4 device to balance the effect of the additional CV mode switches (M_{15} and M_{27}.) For the neurochemical amplifiers, the outputs are also passed through correlated double sampling circuitry (CDS.) The resulting output waveforms are shown in Figure 6. The multiplexing is digitally controlled using on-chip circuitry. One of the important signals is TimingD, which is shown in Figure 6a. This signal has a period of 40 kHz (equivalent to the sample rate.) When TimingD goes low, the multiplexing logic is reset, so that the readout of the 16 amplifiers returns to the first amplifier. Output waveforms are shown in Figure 6b,c. The y-axis is the voltage difference between V_{clamp} and the amount of voltage integrated on the capacitor. In Figure 6b, the amplifier is in FSCV mode, so the amount of charge on the capacitor is subtracted from V_{clamp}. The output is sampled at the points shown by the red dots. This point is centered on the negative pulse produced by the CDS and is sampled at a rate that is 16× faster than the sample rate (640 kHz for a 40 kHz sample rate). In Figure 6c, the amplifier is in amperometry mode, and therefore the amount of charge on the capacitor is added to V_{clamp}. In this case, although the samples happen at the same time with respect to the TimingD pulse, the samples are now on the positive side of the output pulse.

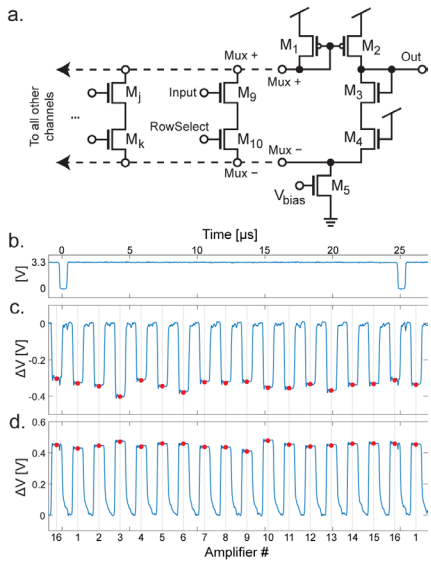


Figure 6. Detail of multiplexing scheme. (**a**) Schematic of the multiplexer circuit. (**b**) The TimingD signal, for resetting the multiplexers during the low period. (**c**) Signal from output buffer in FSCV mode. The red dots are the points where the output is sampled. (**d**) In amperometry mode, the polarity is reversed, and the signal is sampled from the peaks of the output waveform.

4. Electrophysiology Amplifier

In order to create a dense amplifier array, the design and performance of an electrophysiology amplifier must be compact while still providing low noise and high performance to be effective at measuring neuronal signals. In on-CMOS electrophysiology, measurement of action potential and local field potentials is often achieved using transconductance amplifiers which are usually based on a design originally published in [33]. This design also provides the basis for the electrophysiology amplifier used in the dual-mode chip. This section will describe the circuit design and modifications to the common design, as well as the performance of amplifiers on the fabricated dual-mode chip.

4.1. Transconductance Amplifier Design

Miniaturization has been made to facilitate high-density integration and scalability. The noise characteristics of the TCA topology has been discussed [33] that guided the optimization of the transistor size for noise and power consumption. The circuit topology

of the miniaturized TCA design is shown in Figure 7. Unlike the common design, the noninverting feedback capacitors are removed to greatly reduce the required die area consumption. To allow this modification, the noninverting input of the TCA is tied to a stable reference voltage known as V_{pos}. The TCA stabilizes its inverting input by negative feedback through R_F, which is implemented as a MOS-bipolar pseudoresistor (Figure 7a). Perturbations in the voltage at the electrode are amplified by the TCA at a ratio defined by the ratio of C_i/C_f, including the parasitic capacitance. The TCA's output current is converted to voltage by feeding the output to the load capacitance C_L which is implemented as a MOS capacitor (M_L) to further minimize the required die area (Figure 7b). Some ancillary circuitry is also contained in each TCA for the output multiplexing and electroplating of the electrode surface. M_{plate} forms half of a current mirror which enables electroplating when current is forced into I_{plate} and the global current mirror transistor. M_{out} acts as an output buffer when RowSelect is high and the switch M_{sel} is activated similarly to what is described in Section 3.4. This allows for a current path to flow between Mux+ and Mux– which are connected to the output multiplexer.

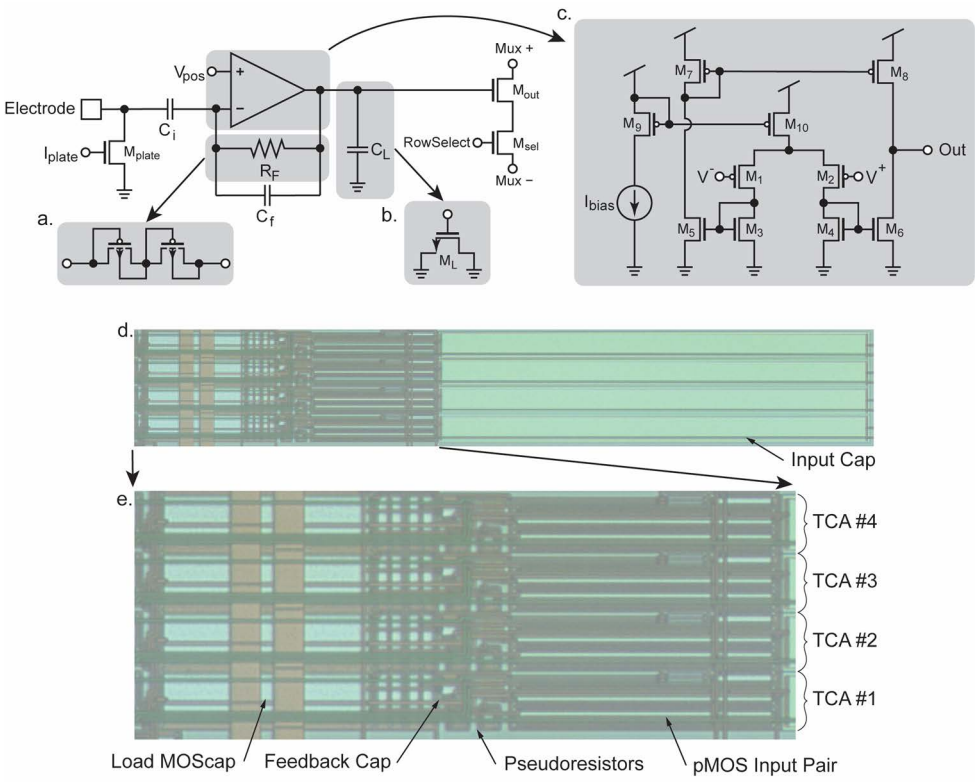


Figure 7. Details of the TCA's design. The TCA uses capacitive feedback providing a gain of roughly C_i/C_f. (**a**) DC stability is provided by a pseudoresistor R_F which is implemented as a pair of diode-connected pMOS devices to conserve die area. (**b**) The load capacitor C_L is implemented as a MOScap for compactness. (**c**) The internal schematic of the multiple current mirror TCA. (**d**) Layout image of a group of four TCAs as fabricated. The input capacitors consume ~60% of the die area. (**e**) Zoomed-in image of the active area of the TCAs. The largest components are the pMOS input devices M_1 and M_2 to minimize their noise contribution. The MOScap C_L also consumes a significant area. Comparatively, the feedback cap C_f and the pseudoresistors R_F are relatively small.

The TCA design is scaled down dramatically and adapted for the 0.35 µm process while maintaining the ideal operating regimes of the transistors (Figure 7c) [50]. The capacitors dominate area consumption even more than the transistors. Careful consideration was taken to reduce the needed area while still yielding an effective gain, bandwidth, and noise performance of the TCA. Overall, the reduction in die area using these optimizations results in dimensions of 541.9 × 20.45 µm and a total area of 0.011 mm^2 per amplifier which

is one of the smallest reported to date. A photomicrograph of a group of fabricated TCAs is shown in Figure 7d. Most of the area, approximately 60%, is consumed by the ~10 pF input capacitor, emphasizing the importance of capacitor dimension optimization. Because of the large size of the input capacitor (Figure 7e) is also presented, which shows only the active area of the TCAs. The large input pair, M_1 and M_2 can be seen with their extreme *W/L* ratio enabling their operation in moderate-to-weak inversion for better noise performance. The load capacitor C_L is the next largest component in terms of die area. Also shown are the relatively small pseudoresistors and feedback capacitor. All other components consume negligible area compared to those already mentioned.

4.2. Transconductance Amplifier Performance

The gain and bandwidth of each TCA are obtained by injecting a small sine wave into the ExConE connection (Figure 4a M_7 and M_{11} and similar in the TCA). A signal is generated using a National Instruments USB-6363 interface while the output amplitude is recorded using the FPGA-based data acquisition system. The response of a typical amplifier is presented in Figure 8a. The passband gain is 37.5 dB, about 75 V/V. The bandwidth is from ~0.2 Hz to ~10 kHz which is sufficient to measure signals in both the local field potential (LFP) band (<300 Hz) and in the action potential (AP) band (300 Hz–7.5 kHz) [51,52]. Since APs are very low amplitude signals, the noise performance of the amplifier must be low. Figure 8b shows a measured noise spectral density of a TCA. Integrating this noise in the AP band yields an input-referred noise of 24.9 μV_{RMS}. To show the transient performance of the TCA, a measurement of a synthetic neural spike is performed at two different amplitudes (~1 mV and 4 mV, peak-to-peak). The spikes are generated using a common scheme [53] and fed into the amplifier. Figure 8c shows the resulting signal of a synthetic neural spike with a peak-to-peak amplitude of ~1 mV. The signal is also shown filtered to the AP band, and a closer view of a single spike is also shown. Similarly, another measurement was performed with spikes of ~4 mV amplitude (Figure 8d). In this testing mode in which the synthesized signal is fed directly into the front-end of the amplifier, the noise is superimposed from the long line and extra-switches that enable this mode. Therefore, the noise in the baseline appears larger than the typical intrinsic noise without the testing mode. The signal-to-noise ratios (V/V) for the presented data are 11.6 and 33.4, respectively. However, if the additional noise introduced from this testing mode is absent, the realistic signal-to-noise ratios are 43.4 and 125.1. These measurements show that neural spikes of approximately 1 mV or more are easily discerned from the random spikes occurring in the noise, and the amplifiers would therefore be capable of measuring actual spikes from live neurons in an in vitro experiment. Because of the noise introduced by the additional circuitry of the testing mode to the front-end of the amplifier, we elected to use 1 mV and 4 mV for the visual representation. However, in realistic neuronal measurements, the 20 μV_{RMS} noise level allows for a reliable measurement of typical action potentials with over 10 V/V signal-to-noise ratio. Table 1 shows detailed specifications to compare the TCA's performance with other presented designs.

The crosstalk between adjacent TCAs is tested (Figure 9). While a voltage spike measured from one amplifier (Amplifier 1), physically adjacent amplifiers' outputs (Amplifier 2–4) without any input are recorded. The adjacent amplifiers do not show any observable signal concurrent with the timing of the spike proving full isolation between amplifiers.

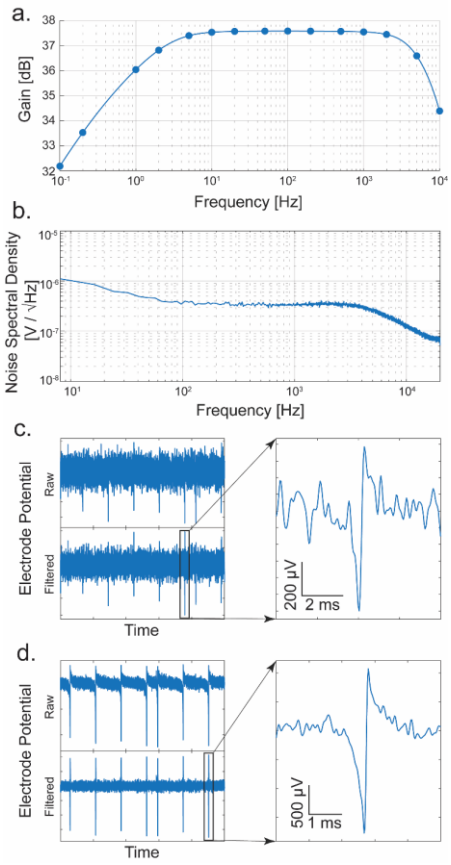


Figure 8. Performance of the TCA. (**a**) Frequency response of a typical amplifier. (**b**) Noise spectral density of a typical amplifier. (**c**) On-chip measurement of a synthesized neural spike of 1 mV amplitude (S/N = 11.6). The raw and filtered frequencies from 300 to 7000 Hz as well as a close-up of a selected spike are shown. (**d**) Measurement of a ~4 mV amplitude synthetic neural spike (S/N = 33.4).

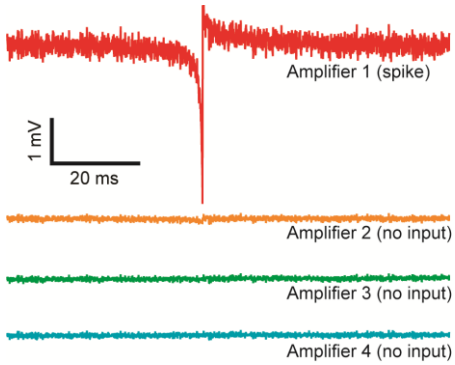


Figure 9. Crosstalk between the TCAs. Amplifier 1–4 are physically adjacent channels. With Amplifier 1 measuring a spike, Amplifier 2–4 without any inputs do not measure any observable crosstalk.

5. CMOS Implementation

The dual-mode CMOS chip is designed and fabricated using a typical 0.35 µm 4 metal 2 poly N-well CMOS process. The technology has a wide dynamic range (3.3 V) and affordable silicon cost that is useful in producing high-density biosensors. For this initial concept device, a die size of 5 mm × 5 mm is used (Figure 10), resulting in 512 fully parallel channels, with 256 dedicated to electrochemical measurements and 256 to electrophysiology measurements. The total power consumed by the dual-mode chip by all 512 amplifiers,

multiplexers, and output buffers is 11.5 mW. This section describes considerations made in the layout of the device, as well as details of the on-chip microelectrode array.

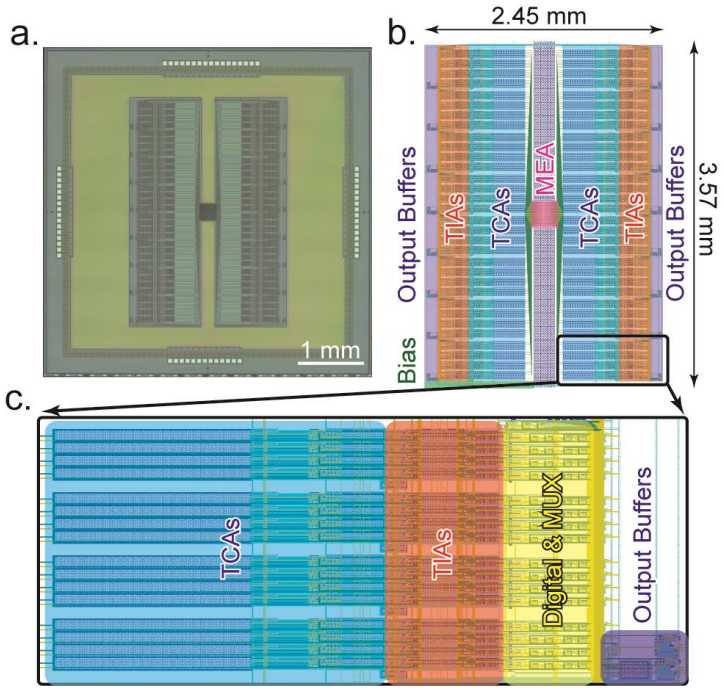


Figure 10. Layout information of the dual-mode chip. (**a**) Photomicrograph of the fabricated dual-mode chip using 0.35 µm CMOS technology. The total size is 5 × 5 mm. (**b**) Location of various structures on the chip. Amplifiers are mirrored on both sides of the centrally located microelectrode array. The active area is 2.45 × 3.57 mm. (**c**) Close-up view of a "pseudocolumn" showing how each group of 16 amplifiers is arranged to enable multiplexing into a single output buffer.

5.1. Chip Layout

The microelectrode array is placed at the center of the die (Figure 10a). In Figure 10b an annotated view of the layout's active area is shown. Wiring from the electrodes fans out to both sides of the array to connect to the amplifiers. On the left and right sides of the MEA, the amplifiers, digital circuitry, output multiplexing, output buffers, and biasing circuitry are mirrored. This arrangement gives a compact use of space and simplifies the electrode interconnection wiring. The dual-mode chip is designed to be interfaced with a custom-designed data acquisition system, so the 512 amplifier channels are multiplexed into 32 output channels [31]. To accomplish this, the outputs are grouped into 16 current channels and 16 voltage channels. These are then split into 8 and 8 on each side of the chip. Thus, each dedicated output serves groups of 16 amplifiers. In the close-up section of Figure 10c, this grouping of 16 amplifiers can be seen. Each of these groups of 16 contains 16 TIAs, 16 TCAs, and 2 output buffers. They are multiplexed together using digital control circuitry and the signals are buffered by the output buffers which are then connected to wire bonding pads to drive the off-chip ADCs. Within the group of 16 amplifiers, the TIAs are grouped in groups of 4 for half sharing. This is clearly seen in both Figure 10c and Figure 4b with the gaps between the groups of 4 amplifiers. For future designs, further space optimization could be obtained, for example, by rearranging the TCA input capacitors to use this empty space. For this initial design, this was not done to simplify the layout and ensure that all amplifiers are as identical as possible to minimize any potential peculiarities caused by nonidentical layout.

5.2. Microelectrode Array

The microelectrode array is a critical part of the dual-mode chip since it is the source of the signals that we are aiming to measure. It must have a high enough spatial resolution to resolve fine details between neurons. To determine a reasonable pitch, we examined other literature and chose a value on a similar scale. In other MEAs some typical ranges are from 13.5 µm [29], 18 µm [54], to 42 µm [22] and even wider. For this design, the value was chosen to be 16 µm between electrodes. This value was chosen to stay closer to the smallest pitch reported in the literature, while giving sufficient space for the routing of the wiring out from the electrodes to the amplifiers as well as potential post processing that may take place. The resulting electrode array is shown in Figure 11. In Figure 11a, the layout is shown. The routing of the wiring fanning out from the center to the left and right sides, where they run out to connect to the amplifiers. The overall size of the MEA is 255.4 µm on each side. A closer view is shown in Figure 11b. The opening in the top glass passivation layer is 5 µm which is seen as an orange-colored square in the opening. This is the exposed area of AlCu where signals will enter the chip. Between similar mode electrodes, the spacing is 16 µm and between differing mode electrodes, the pitch is 8 µm. The array is effectively two separate arrays with a pitch of 16 µm between adjacent electrodes. One for the voltage channels and one for the current channels. Each array is interdigitated at an 8 µm pitch to produce a checkerboard pattern that can be seen in Figure 11c. Finally, a fabricated MEA is shown in Figure 11d. The density of the MEA is close to the limit of what can practically be fabricated in 0.35 µm technology without deliberately violating design rules which would potentially result in shorted electrodes or non-exposed electrodes on the chip's surface. For effectiveness in practical measurements, the electroplating circuitry within the amplifiers can be used to deposit a suitable and biocompatible electrode surface such as gold, platinum black, or Ag/AgCl. Additionally, our previously reported post-CMOS processing can be performed to create high quality electrodes and interelectrode isolation by the metal deposition and lift-off technique [14].

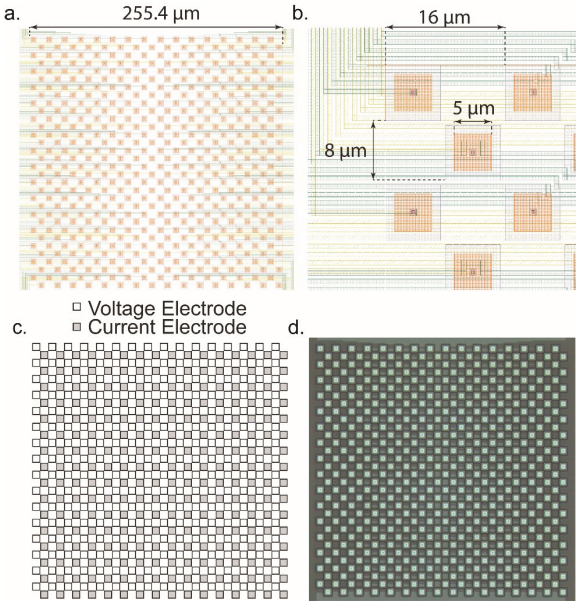


Figure 11. Design of the microelectrode array. (**a**) Layout image of the MEA. The MEA is 512 electrodes with 256 dedicated to voltage measurement and 256 dedicated to current measurement. The total size is ~250 × 250 µm. (**b**) Detail of the individual electrodes. The pitch between electrodes is 16 µm, the glass opening is 5 µm, and between rows the pitch is 8 µm. Each row is staggered, forming the checkerboard pattern. The yellow and green layers are the metal interconnects that connect the electrodes to the amplifiers. (**c**) Arrangement of the voltage and current electrodes. Each row serves a different modality amplifier. (**d**) Photomicrograph of the MEA as fabricated on-chip.

6. Conclusions and Discussion

We present a CMOS chip that is capable of fully parallel and simultaneous measurement of 512 channels from an on-chip microelectrode array with 256 neurochemical and 256 electrophysiology amplifiers. Since the amplifiers are compact and scalable, a larger array with 1000 s of amplifiers could easily be integrated into a chip that would fit within a commonly used silicon reticle. This proof-of-concept design fits 512 amplifiers and an electrode array into a total active area of only 2.45 mm × 3.57 mm. This dual-mode technology allows the simultaneous study of the interactions between neurotransmission, synaptic function, and action potential propagation. As a tool, this technology could provide a means for neuroscientists to study the mechanisms of neuronal degradation and synaptic dysfunction seen in cases of many neurodegenerative disorders. We plan to implement the packaging strategy based on our previous in vitro neurochemical sensor array [14]. The silicon die will be attached to a PCB die holder and wire bonded for electrical connectivity. A 3D printed well will be attached directly to the silicon die using PDMS to protect the wire bonds from any electrolytic solution and confine the solution to the electrode array. Heating of the chip must be carefully considered to limit their influence on the cell culture. Given that the power consumption of this chip is 11.5 mW from 2.45 mm × 3.57 mm silicon area, the rate of heat transfer is 1.3 mW/mm^2. Given that the free convection of electrolyte is between 0.5–10 $mW/mm^2 \cdot K$, the heating of the chip is unlikely. Also, during a typical measurement, perfusion is used to exchange and supply the recording and stimulation solutions. The forced convection significantly elevates the heat transfer rate allowing the heat to be taken away more efficiently.

The amplifier is designed with a focus on scalability, thus introducing a considerable tradeoff between the amplifier's silicon footprint and its noise performance. Depending on the application, adequate noise levels for electrophysiological recording systems vary (below 10 μV_{RMS} for in vivo applications and below 30 μV_{RMS} for in vitro applications). Contrary to in vivo applications, cells become well attached to the surface of the electrodes in in vitro studies and therefore the electrode can measure larger signal, relaxing the noise requirement. To maximize the throughput in in vitro applications, this work optimized the area each TCA is occupying while achieving comparable noise level to commercial MEA systems (Multiwell-MEA: ~20 μV_{RMS}, CMOS-MEA5000: 300–400 μV_{RMS}). Depending on the application, the area of the amplifiers can be optimized to achieve better noise performance at the expense of a larger footprint that results in a lower channel count.

For future implementations, an increase in electrode count would be desired to enable measurements of larger physical areas. Additionally, a potential improvement to this design applies specifically to the design of MEA itself. The soma of a neuron is roughly equivalent in size to our MEA's electrode pitch, but a neuron will typically have multiple dendrites for receiving neurotransmitters from presynaptic neurons. This fact would suggest that if a more complete analysis of the interactions between neurotransmission and action potentials is desired, then an optimal MEA would have more neurochemical electrodes than electrophysiology electrodes. However, the dual-mode device in its current form is still the first device reported that is capable of measuring neurochemical signals at a similar spatial resolution as action potentials, and the design of a dual-mode chip with an improved MEA would be simple as the amplifier designs are compact and scalable.

High-density neural probes have been developed by monolithically integrating the neural electrodes and the processing circuitry [55]. In the future, the presented dual-mode amplifier design can be applied to develop monolithic dual-mode neural probes for in vivo recordings where both the neurochemicals and the electrical activities are monitored simultaneously in the brain.

Author Contributions: Conceptualization, G.M., K.A.W. and B.N.K.; methodology, G.M., K.A.W. and B.N.K.; software, G.M., K.A.W. and B.N.K.; validation, G.M., K.A.W. and B.N.K.; formal analysis, G.M. and B.N.K.; investigation, G.M., K.A.W. and B.N.K.; resources, B.N.K.; data curation, G.M. and B.N.K.; writing—original draft preparation, G.M. and B.N.K.; writing—review and editing, G.M., M.A.C.

and B.N.K.; visualization, G.M., M.A.C. and B.N.K.; supervision, B.N.K.; project administration, B.N.K.; funding acquisition, B.N.K. All authors have read and agreed to the published version of the manuscript.

Funding: This work was supported by the National Science Foundation (NSF) under grants #2133225 and #2143140, and the United States Air Force Office of Scientific Research (AFOSR) under grant #FA9550-21-1-0117.

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Data Availability Statement: Data is not available.

Conflicts of Interest: The authors declare no conflict of interest.

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