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Barrier Height, Ideality Factor and Role of Inhomogeneities at the AlGaN/GaN Interface in GaN Nanowire Wrap-Gate Transistor

Siva Pratap Reddy Mallem [1,†], Peddathimula Puneetha [2,†], Yeojin Choi [3], Seung Mun Baek [3], Dong-Yeon Lee [2], Ki-Sik Im [4,*] and Sung Jin An [3,*]

[1] Advanced Material Research Center, Kumoh National Institute of Technology, Gumi 39177, Republic of Korea; drmspreddy@kumoh.ac.kr
[2] Department of Robotics and Intelligent Machine Engineering, College of Mechanical and IT Engineering, Yeungnam University, Gyeongsan 38541, Republic of Korea; puneethaphd@gmail.com (P.P.); dylee@ynu.ac.kr (D.-Y.L.)
[3] Department of Materials Science and Engineering, Kumoh National Institute of Technology, Gumi 39177, Republic of Korea; dota23@kumoh.ac.kr (Y.C.); monndal980@kumoh.ac.kr (S.M.B.)
[4] Department of Green Semiconductor System, Daegu Campus, Korea Polytechnics, Daegu 41765, Republic of Korea
* Correspondence: ksim3492@gmail.com (K.-S.I.); sungjinan@kumoh.ac.kr (S.J.A.)
† These authors contribute to equally to this work.

Abstract: It is essential to understand the barrier height, ideality factor, and role of inhomogeneities at the metal/semiconductor interfaces in nanowires for the development of next generation nanoscale devices. Here, we investigate the drain current (I_{ds})–gate voltage (V_{gs}) characteristics of GaN nanowire wrap-gate transistors (WGTs) for various gate potentials in the wide temperature range of 130–310 K. An anomalous reduction in the experimental barrier height and rise in the ideality factor with reducing the temperature have been perceived. It is noteworthy that the variations in barrier height and ideality factor are attributed to the spatial barrier inhomogeneities at the AlGaN/GaN interface in the GaN nanowire WGTs by assuming a double Gaussian distribution of barrier heights at 310–190 K (distribution 1) and 190–130 K (distribution 2). The standard deviation for distribution 2 is lower than that of distribution 1, which suggests that distribution 2 reflects more homogeneity at the AlGaN/GaN interface in the transistor's source/drain regions than distribution 1.

Keywords: wrap-gate transistor; nanowire; GaN; barrier height; inhomogeneities

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1. Introduction

Nano-based field-effect transistors (FET) are involved with replacing existing conventional technology and have surged to be one of the potential solutions towards continuous complementary metal-oxide-semiconductor (CMOS) scaling. The semiconductor-based nanowires have been significantly explored because of their most promising applications for next-generation high-quality optoelectronic/electronic devices [1–3]. The scaling of numerous transistor types is based on geometries as in Fin-FET, omega gate, tri-gate, and wrap-gate (WG) or gate-all-around (GAA) devices [4–11]. WG-based devices contribute particularly remarkable performance advantages over other geometries because of their extreme electrostatic controls. During recent years, WG-based devices fabricated by bottom-up techniques have been intensively studied as the fundamental building block for nano-electronic devices and circuit technologies. The top-down fabrication of nanowire WG transistors (WGTs) based on a sacrificial layer has many advantages in contrast to a bottom-up approach: reduced device size, large-scale feasibility with high yield, and an orderly alignment of parallel nanowires. It has already been reported that GaN-based nanowires have made significant progress. GaN-based devices have attractive features for great device performance such as high-speed, high-power, high-frequency, and high-temperature operations. A GaN nanowire-based device can control its normally off state

with a high I_{on}/I_{off} ratio, a low gate leakage current, and a high conductance. For this paper, we fabricated a device using the top-down process and investigated the electrical transport properties in a GaN nanowire WGT on a GaN-on-insulator (GaNOI) substrate.

Knowledge of nanowire device operation at cryogenic temperatures is of special interest because, at room temperature, nanowire devices do not yield broad information about their carrier transport characteristics. The current–voltage (*I*–*V*) properties of nanowires as a function of temperature allows the identification of various current flow mechanisms and additional significant electrical transport across the metal/semiconductor interface (i.e., source/drain regions) [12,13]. A good understanding of barrier heights, ideality factor, and the role of inhomogeneities at the metal/semiconductor interface in nanowires led to the concept of the thermionic emission (TE) mechanism by assuming the coexistence of a double Gaussian distribution.

The metal/semiconductor interface is characterized by a certain work function. The fact it is Ohmic or Schottky depends on the boundary conditions at the interface which depends on a few variables, including the semiconductor doping concertation near the interface. High doping allows the tuning of the carriers across the barriers, reducing the contact resistance. Usually, after the preparation of Ohmic contacts for the fabrication of FETs in their source and drain regions, certain semiconductor contacts appear to have Ohmic behavior, but in truth, they are Schottky in nature. In experiments, a FET with two identical source and drain regions can be seen to have back-to-back Schottky contacts.

Here, we have studied the electrical transport mechanism in the GaN nanowire WGT as a function of temperature with variable gate bias. The temperature dependence of the barrier height (Φ_{b0}) and the ideality factor (η) values are found at the interface of AlGaN/GaN in the source/drain regions of the GaN nanowire WGT. Finally, we showed that the two linear regions in the variation of Φ_{b0} versus 1/2 kT could be explained with the help of a double Gaussian distribution.

2. Materials and Methods

For the GaN nanowire WGT architecture, we used a GaNOI substrate based on Smart Cut^{TM} technology from the SOITEC Company by the dual-wafer transfer method [7]. A 4-inch diameter GaNOI substrate consists of 150 nm thick GaN film and 800 nm thick silicon-dioxide (SiO_2) on a 0.65 mm thick sapphire wafer. Initially, the ‹11-20› phase was aligned by electron beam (e-beam) lithography on the GaNOI substrate with the help of poly(methyl methacrylate) (PMMA) resist. Using an inductively coupled plasma (ICP) dry etching process, the GaN film was selectively etched, and after this, the aligned film was dipped in 5% of tetramethylammonium hydroxide (i.e., TMAH was purchased from Transene company, Inc., Danvers, MA, USA) etchant solution at 90 °C for 10 min. The TMAH etchant solution entirely etches in the sideways direction instead of perpendicular *c*-plane (0001) direction. This etchant solution reduced the GaN film width along the ‹11-00› phase, giving 83 nm heights with similar triangular-shaped sidewall ‹11-01› phases. Next, the film was treated with a buffer-oxide etchant (BOE) solution to effectively remove the SiO_2 layer under the structure of the GaN nanowires.

Next, selectively re-grow 50 nm and 20 nm thicknesses of undoped GaN and AlGaN films on the aligned GaN surface using a sophisticated metal-organic chemical vapor deposition (MOCVD) instrument. Here, a self-limiting re-growth in the ‹11-01› phase acted as an *r*-plane on the aligned GaN film. At this viewpoint, the surface of the *r*-plane consisted of nitrogen (N) atoms that were easily impelled by hydrogen (H) atoms in the MOCVD instrument and produced N-H bonds that limited growth and added stability in the plane direction. Hence, AlGaN/GaN films were not re-grown on the GaN nanowire but easily re-grown only on the source and drain regions. As a result of this procedure, the GaN nanowire's area has not changed. In fact, the significance of re-grown AlGaN/GaN films on the source and drain regions decreases the series resistance through two-dimensional electron gas (2DEG) at the junction.

For WGT device fabrication, 10 nm and 20 nm thicknesses of gate-metal (TiN) and high-*k* gate oxide (Al_2O_3) were coated using plasma-enhanced atomic layer deposition (PE-ALD) method. The thicknesses of the coated materials are confirmed by the number of PE-ALD cycles, a deposition rate (growth per cycle) of ~0.1 nm/cycle was determined by an ellipsometry. Here, 100 and 200 PE-ALD cycles are relatively equal to ~10 nm and ~20 nm thickness of TiN and Al_2O_3 layers. Accordingly, metal layers (Ti/Al//Ni/Au) were coated as source and drain regions with an e-beam technique and followed by rapid thermal process at 850 °C for 30 s in N_2 atmosphere. Finally, gate metal (Ni/Au) was coated as an outer contact for device measurements. The re-grown AlGaN film mobility (μ_d, 1630 $cm^2/V{\cdot}s$) and concentration (N_S, 9.75 × 10^{12} cm^{-2}) were confirmed using Hall-effect examination (Nanometrics, HL5500PC, Kanata, ON, Canada). The device architecture was examined with a field-emission tunneling electron microscope (FE-TEM, 200 kV FE, JEM-2100F, Tokyo, Japan). The temperature-dependent *I*–*V* characteristics of the device were measured with a Keithley source unit (SCS-4200, Cleveland, OH, USA) connected to vacuum chamber (MST-6VC) with a low-temperature regulate system. The sensitivity of the temperature control system is ±1 K.

3. Results

Figure 1a (on the left side) illustrates the schematic architecture of the studied GaN nanowire WGT device. It has a 2 μm gate length consisting of 64 triangular-shaped one-dimensional nanowires, each having two similar ‹1-101› crystal facets. On the right side of Figure 1a, an FE-TEM (i.e., dark field mode) image clearly shows a triangular-shaped GaN nanowire core surrounded by gate-oxide and gate-metal. Figure 1b shows the drain current (I_{ds}) versus gate voltage (V_{gs}) curves of the AlGaN/GaN-based GaN nanowire WGT as a function of temperature ranging from 130 to 310 K in steps of 30 K at a drain voltage of V_{ds} = 0.1 V. The drain leakage current (I_{ds}) clearly increases with temperature from 1.12 × 10^{-13} (at 130 K) to 2.15 × 10^{-12} A (at 310 K) at a V_{gs} of −2 V. The increase in drain leakage current may be due to the surface-related traps and temperature-assisted tunneling mechanisms [14,15]. The inset of Figure 1b shows a simplified diagram of the fabricated device with a back-to-back Schottky configuration composed of two (source/drain) contacts in series with GaN nanowires.

The current across the barrier mainly consists of three types of electron transport mechanisms: thermionic emission (TE), thermionic field emission (TFE), and field emission (FE). The dominant mode of carrier transport can be determined from the characteristics of the tunneling parameter E_{00}; $E_{00} \ll kT$ for TE, $E_{00} \approx kT$ for TFE, and $E_{00} \gg kT$ for FE. E_{00} is evaluated from the doping concentration (N_d) of the measured semiconductor as in [16]:

$$E_{00} = \left(\frac{qh}{kT}\right)\sqrt{\frac{N_d}{m^*\varepsilon_S}} \quad (1)$$

where *h* is Planck's constant, *q* is the charge, *T* is the absolute temperature, *k* is the Boltzmann constant, ε_S is the permittivity of the GaN (i.e., $\varepsilon_S = 9.2\varepsilon_0$), m^* is effective mass ($m^* = 0.3\ m_0$ [17], where m_0 is mass of electron), and the value of N_d in the present work is ~5 × 10^{16} cm^{-3}. E_{00} is calculated to be about 8 meV from Equation (1), which is smaller than the value of kT at room temperature. This means that TE is the dominant carrier transport mechanism in the GaN nanowire at room temperature.

To investigate the effect of the GaN nanowire structure on the device characteristics at the AlGaN/GaN interface, we further analyzed the temperature dependence of effective barrier height (Φ_{b0}) and ideality factor (η) at the interface for different gate potentials. A GaN nanowire WGT with two similar metal contacts at the AlGaN/GaN (source and drain) regions can be regarded as back-to-back Schottky diodes. In this device architecture, most of the voltage drop happens in the reverse-biased side [18,19]. The Φ_{b0} and η parameters are extracted by using the following relations [13]:

$$I = I_0 exp\left(\frac{qV}{\eta kT}\right)\left[1 - exp\left(-\frac{qV}{\eta kT}\right)\right] \quad (2)$$

where $I_0 = A^*T^2A\ exp\left(\frac{-q\Phi_{b0}}{kT}\right)$, V is the gate bias, A is the contact area, and A^* is the effective Richardson's constant. The theoretical value of A^* is ~35.8 $Acm^{-2}K^{-2}$ based on the effective mass of AlGaN [17] and is used for the calculation of Φ_{b0}. Equation (1) is modified as follows:

$$\ln\left[\frac{I\exp(qV/kT)}{\exp(qV/kT) - 1}\right] = \ln I_0 + \frac{qV}{\eta kT} \quad (3)$$

where V is the voltage drop across the junction, $V = V_{ds} - IR$, and here, R is the series resistance. The values of I_0 at different gate potentials were obtained from the I–V measurements (Figure 2a–d) in the plot of $\ln[I\ \exp(qV/kT/(\exp(qV/kT) - 1)]$ versus V for the reverse bias at each temperature. The values of η and Φ_{b0} are extracted from the slope and y intercept using Equation (3).

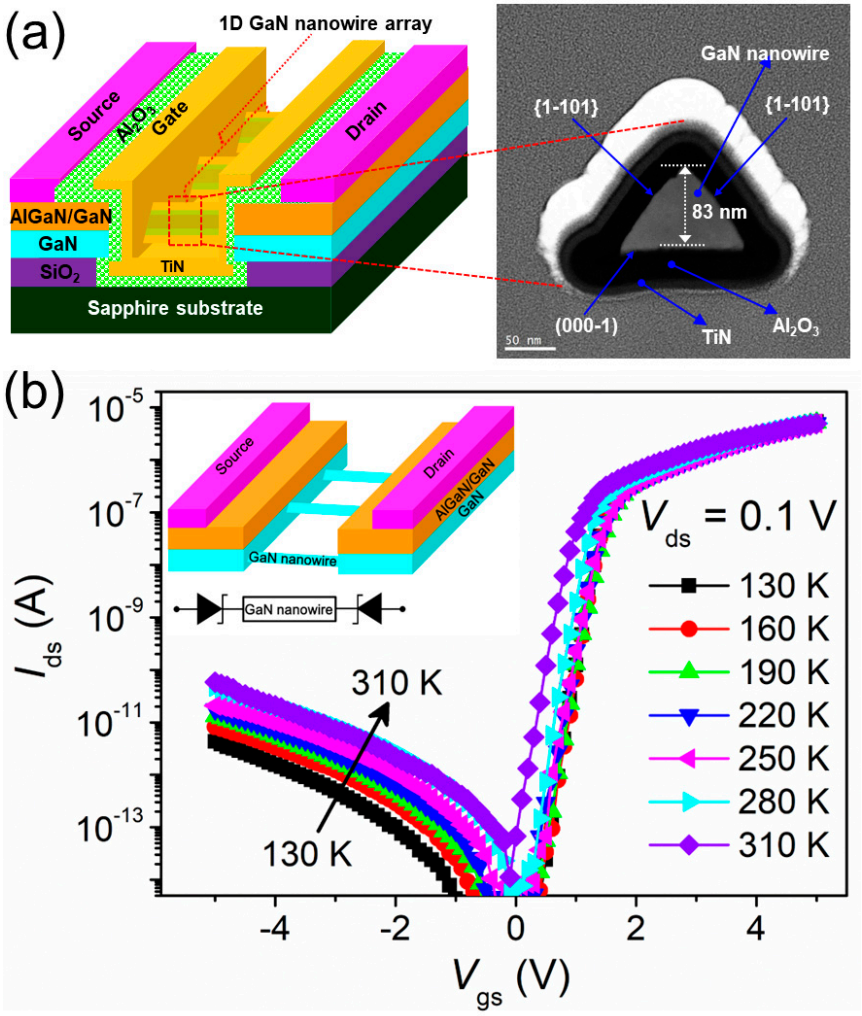

Figure 1. (**a**) Schematic device architecture of the fabricated GaN nanowire WGT with a high-resolution FE-TEM cross-section image of a triangular-shaped GaN nanowire. (**b**) Logarithmic plots of drain-current (I_{ds}) versus gate-voltage (V_{gs}) at V_{ds} = 0.1 V as a function of temperature, and inset figure shows back-to-back GaN nanowire WGT with a simplified circuit diagram.

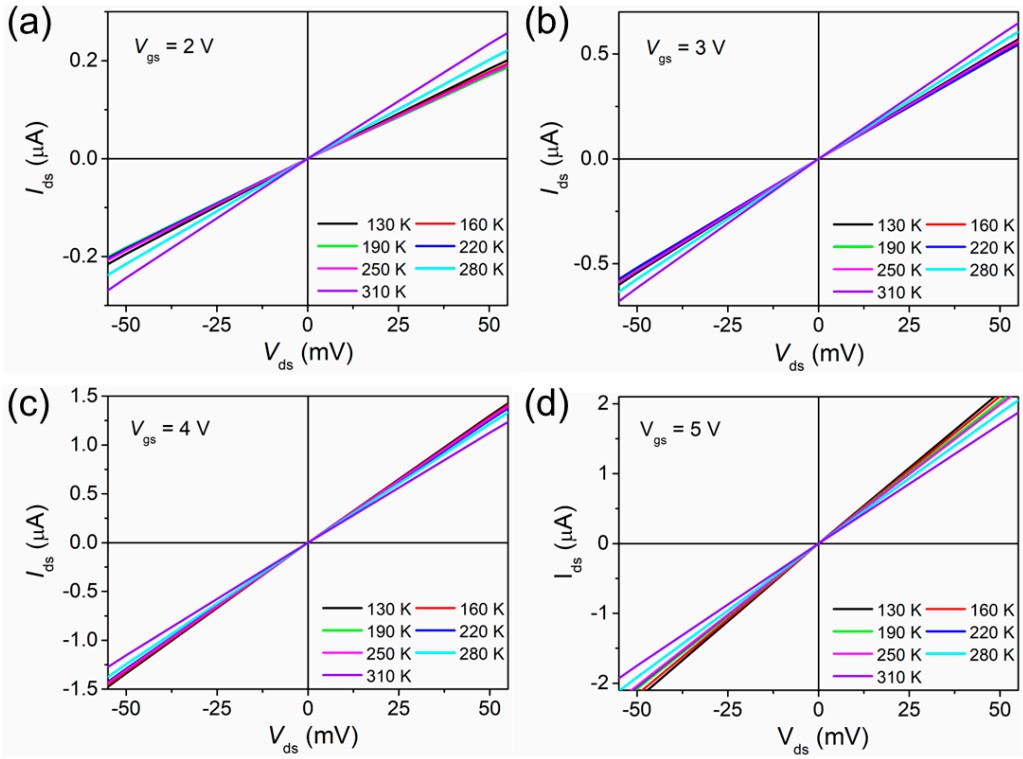

Figure 2. Drain-current (I_{ds}) versus drain-voltage (V_{ds}) plots of the GaN nanowire WGT as a function of temperature at gate biases of (**a**) 2 V, (**b**) 3 V, (**c**) 4 V, and (**d**) 5 V.

At temperature of 310 K, the values of Φ_{b0} (Figure 3a) and η (Figure 3b) for different gate voltages were, respectively, found to be 0.41 eV and 1.22 at 2 V, 0.39 eV and 1.45 at 3 V, 0.37 eV and 1.54 at 4 V, and 0.36 and 1.65 at 5 V. These values confirm that TE is the dominant current conduction mechanism in GaN nanowire-based devices at room temperature. It is clearly shown that Φ_{b0} (Figure 3a) increases and η (Figure 3b) decreases with increasing temperature at a range of gate voltages. At 130 K, the values of Φ_{b0} and η for various voltages were, respectively, found to be 0.15 eV and 4.4 at 2 V, 0.14 eV and 4.6 at 3 V, 0.12 eV and 4.8 at 4 V, and 0.11 eV and 4.9 at 5 V. It is worthwhile to note that these values of η are much better than found in previous studies of GaN-based nanowires and nano-rods [20–23]. This may be due to the low semiconductor doping concentration or influence of surface states at the interface compared to previous studies. These η values are higher than unity, however, indicating that TE is not the entire conduction mechanism. This typical signature may be the result of tunneling, interface states, electrical dipole formation, or barrier inhomogeneities [24,25]. Tunneling current is significant in nanoscale devices compared to bulk devices because the device size is comparable to or less than the zero bias depletion width [W_d]. W_d can be expressed as follows [24,25]:

$$W_d = \left(\frac{2\varepsilon_S(\Phi_{b0} - V_n)}{q^2 N_d} \right)^{\frac{1}{2}} \quad (4)$$

where $V_n = kT\ln(N_C/N_d)$ is the position of the conduction band (E_C) edge with respect to the Fermi level position (E_F) in a GaN nanowire. N_C is the density of states in the conduction band minimum as given by $N_C = 2(2\pi m^* kT/h^2)^{3/2}$. Its values were ~$9 \times 10^{17}$ and 3.1×10^{18} cm^{-3} [24] at 130 K and 300 K. From Equation (4), the value of W_d varies in the range of 25–90 nm for all temperature barrier heights. These varied W_d values are comparable to a GaN nanowire height of ~83 nm, and hence, the tunneling current could be a major factor at the metal/AlGaN/GaN interface in GaN nanowires for all temperatures that drive the ideality factor above the unit value.

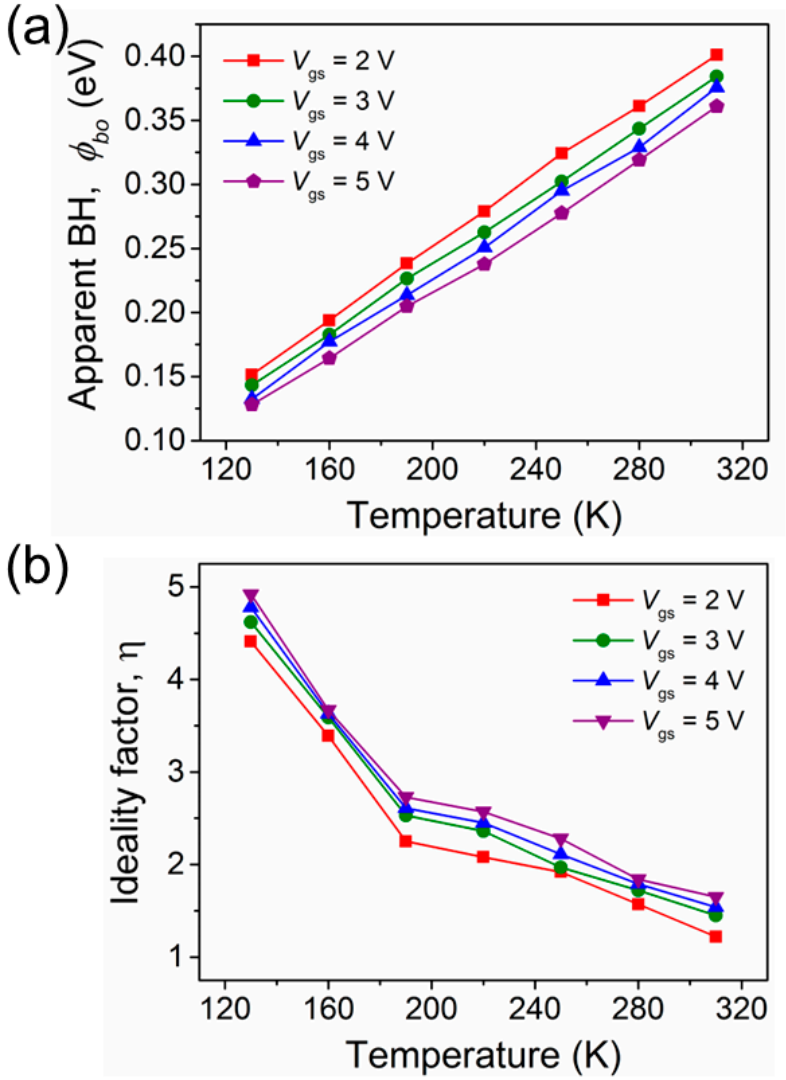

Figure 3. Variation in (**a**) Φ_{b0} and (**b**) η with temperature for different gate biases.

To further understand the nature of carrier transport in a GaN nanowire, we view an inhomogeneous metal contact at the AlGaN/GaN interface as a distribution of local high and low barrier height patches with nanoscale geometry. Here, electrical transport at low temperatures is dominated by low barrier height patches with a higher ideality factor as the carrier passes through the patches. At high temperatures, the carrier flows through high barrier patches causing the barrier height to increase and the ideality factor to decrease. Consequently, the barrier height at the AlGaN/GaN interface of the source/drain region is not constant but follows a Gaussian distribution due to the barrier inhomogeneities as in [26]:

$$P(\Phi_{b0}) = \frac{1}{\sigma_S\sqrt{2\pi}}\exp\left[-\frac{\left(\overline{\Phi_{b0}} - \Phi_{b0}\right)^2}{2\sigma_S^2}\right] \quad (5)$$

Here, $1/\sigma_S\sqrt{2\pi}$ is the normalized distribution constant, and $\overline{\Phi_{b0}}$ and Φ_{b0} are, respectively, the zero bias mean and the apparent barrier height. The standard deviation of the Gaussian distribution σ_S in the normalized distribution function $P(\Phi_{b0})$ represents the level of inhomogeneities at the interface of AlGaN/GaN in the GaN nanowire WGTs. $\overline{\Phi_{b0}}$ and Φ_{b0} (measured from semi-log I_{ds}–V_{gs} data) are associated as in [27,28]:

$$\Phi_{b0} = \overline{\Phi_{bo}} - \frac{\sigma_S^2}{2kT} \quad (6)$$

The above relation states that the effective Φ_{b0} is normally smaller than the mean $\overline{\Phi_{b0}}$ unless $\frac{\sigma_S^2}{kT} \approx 0$. This is because TE occurs through lower barriers. From Equation (6), a plot of Φ_{b0} versus 1/2 kT is a straight line with the slope (σ_S) and intercept ($\overline{\Phi_{b0}}$). Figure 4 shows the plots for Φ_{b0} versus 1/2 kT for different gate biases in the temperature range of 130–310 K where two straight lines with different slopes and intercepts are seen in the temperature range of 310–190 K (distribution 1) and 190–130 K (distribution 2). The values of $\overline{\Phi_{b0}}$ and σ_S are 0.65 eV and 119 meV for 2 V, 0.62 eV and 118 meV for 3 V, 0.61 eV and 117 meV for 4 V, and 0.59 eV and 116 meV for 5 V in the temperature range of 310–190 K. In the temperature range of 190–130 K, the values of $\overline{\Phi_{b0}}$ and σ_S come out to, respectively, be 0.45 eV and 84 meV for 2 V, 0.43 eV and 81 meV for 3 V, 0.41 eV and 80 meV for 4 V, and 0.39 eV and 79 meV for 5 V.

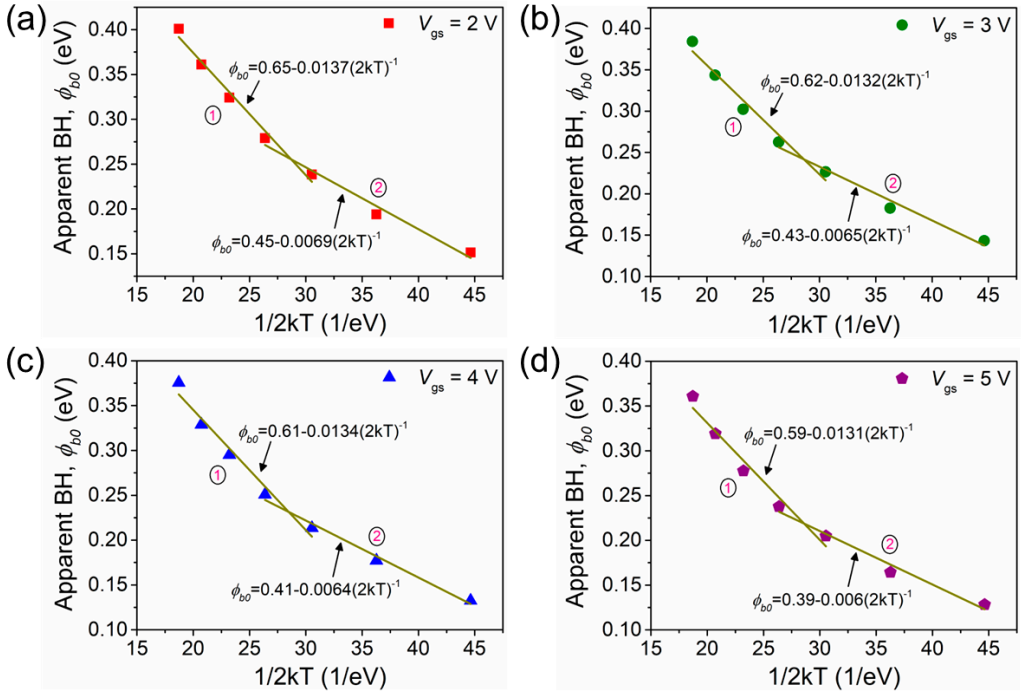

Figure 4. Apparent barrier height (Φ_{b0}) as a function of 1/2 kT in the temperature range of 310–130 K for different gate biases (**a**) 2 V, (**b**) 3 V, (**c**) 4 V, and (**d**) 5 V. Solid straight lines show the least squares fit. Lower values of σ_S in the temperature range of 190–130 K (distribution 2) as compared to 310–190 K (distribution 1) indicate that the interface is more homogenous in the lower temperature region.

Table 1 shows that the lower mean barrier heights, $\overline{\Phi_{b0}}$ in the low-temperature region (190–130 K, distribution 2) are due to the surface-related traps [14], and the higher values of the mean $\overline{\Phi_{b0}}$ in the high-temperature region (310–190 K, distribution 1) are due to temperature-assisted tunneling [14]. In addition, the lower value of σ_S in the 190–130 K temperature range suggests more GaN nanowire homogeneity in this range compared to the 310–190 K range. There are several reports on double Gaussian distributions in GaN-based devices that can be ascribed to the nature of the inhomogeneities in the two regions [29,30]. These two regions of inhomogeneity may be related to variation in the interface phase/composition, electrical charges, interface quality, or nonstoichiometry, etc. In addition, such inhomogeneities may happen on a nanoscale that inhibits their detection using typical measurements. The inhomogeneities affect the I_{ds}–V_{gs} measurements of a device mostly at low temperatures, so these measurements can explore the role of the barrier inhomogeneities present in the device. The occurrence of a double Gaussian distribution at a low temperature might happen due to some phase changes taking place below a certain temperature [26,31,32]. Further, the range of temperatures covered by each straight line suggests a region where the corresponding distribution is effective. The above results

reveal that the temperature-dependent characteristics of the GaN nanowire WGT measured at the AlGaN/GaN interface in the source/drain regions can be explained by the presence of a double Gaussian distribution of the barrier heights.

Table 1. Mean values of barrier heights and standard deviation at distribution 1 and 2 for different gate voltages.

V_{gs} (V)	Distribution 1		Distribution 2	
	$\overline{\Phi_{b0}}$ (eV)	σ_S (meV)	$\overline{\Phi_{b0}}$	σ_S (meV)
2	0.65	119	0.45	84
3	0.62	118	0.43	81
4	0.61	117	0.41	80
5	0.59	116	0.39	79

4. Conclusions

In summary, the barrier height, ideality factor and role of inhomogeneities in GaN nanowire WGTs were studied at different gate potentials as a function of temperature. In I temperature range of 130–310 K, the experimental zero bias depletion width is nearly equal to the nanowire height. Therefore, we suggest that electrical transport through the nanowire is also affected by a tunneling mechanism. Φ_{b0} seems to decrease and η seems to increase with a decrease in temperature for all gate voltages. We ascribe these behaviors to barrier inhomogeneities in the GaN nanowires. The temperature-dependent I_{ds}–V_{gs} characteristics of the GaN nanowire WGTs were shown to be a double Gaussian distribution with different standard deviations and mean barrier heights within the temperature regions of 310–190 K (distribution 1) and 190–130 K (distribution 2). These results are significant for the advancement of future applications and the enhancement of device performance.

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