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Superior High Transistor's Effective Mobility of 325 cm^2/V-s by 5 nm Quasi-Two-Dimensional SnON nFET

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Abstract: This work reports the first nanocrystalline SnON (7.6% nitrogen content) nanosheet n-type Field-Effect Transistor (nFET) with the transistor's effective mobility (μ_{eff}) as high as 357 and 325 cm^2/V-s at electron density (Q_e) of 5×10^{12} cm^{-2} and an ultra-thin body thickness (T_{body}) of 7 nm and 5 nm, respectively. At the same T_{body} and Q_e, these μ_{eff} values are significantly higher than those of single-crystalline Si, InGaAs, thin-body Si-on-Insulator (SOI), two-dimensional (2D) MoS_2 and WS_2. The new discovery of a slower μ_{eff} decay rate at high Q_e than that of the SiO_2/bulk-Si universal curve was found, owing to a one order of magnitude lower effective field (E_{eff}) by more than 10 times higher dielectric constant (κ) in the channel material, which keeps the electron wave-function away from the gate-oxide/semiconductor interface and lowers the gate-oxide surface scattering. In addition, the high μ_{eff} is also due to the overlapped large radius s-orbitals, low 0.29 m_o effective mass (m_e*) and low polar optical phonon scattering. SnON nFETs with record-breaking μ_{eff} and quasi-2D thickness enable a potential monolithic three-dimensional (3D) integrated circuit (IC) and embedded memory for 3D biological brain-mimicking structures.

Keywords: high mobility; thin-film transistors; SnON; SnO_2; density functional theory

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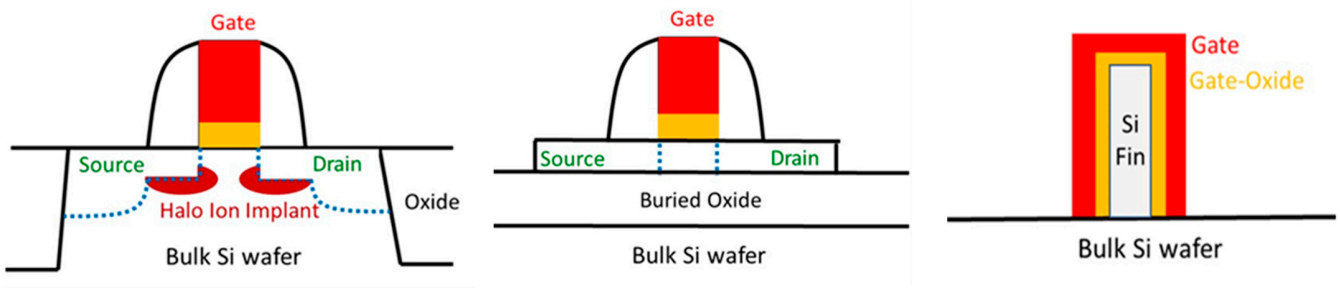
1. Introduction

Modern processors, with over 100 billion transistors, are among the most complex systems. To meet the ever-changing demand for small and high-performance devices, processor transistor density and performance must be increased. Therefore, Moore's law must be preserved, i.e., the Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) must continue shrinking in size. The conventional MOSFET is a surface channel device. In long-channel conventional MOSFETs technology, the characteristics of the transistor were at par with the essential speed as well as power requirements. In this era of electronics, power saving and low leakage are more crucial compared to an increase in speed. The drive current rises with the new generation of transistor. However, there is also a tremendous enhancement in the subthreshold leakage current, which results in an increase in the power consumption [1]. Moreover, in FETs with a small channel length, the depletion regions underneath the source and drain cause degraded FET's off-state leakage (I_{OFF}), poor sub-threshold slope (SS), and threshold voltage (V_T) reduction by drain-induced barrier lowering. To overcome those short-channel effects, a thin body thickness (T_{body}) Si-on-Insulator (SOI) was invented. The SOI can use a substrate bias to improve the gate electrostatic control on channel carriers. When transistor sizes grew smaller in conventional planar MOSFETs with a 1.2 nm SiO_2 gate oxide, the market required a significant innovation to retain performance while limiting short channel effects and power in advanced technologies, as the DC leakage in SiO_2 is intolerably high. It was necessary to create a gate dielectric that could be substituted with SiO_2, one that was thick enough to block direct electron tunneling through it but permeable enough to allow the electric field of the gate to enter the channel. Therefore, the solution was to use high dielectric–constant (high-κ) dielectric, which is a dielectric material that has a higher dielectric permittivity than SiO_2.

Although the use of high-κ dielectrics with metal gates increased the lifetime of planar MOSFET by decades, it became necessary to introduce new devices beyond the 28 nm technology node to address the problems with traditional MOSFET [2]. Tremendous efforts have been made to reduce oxide thickness (t_{ox}) and increase ε_{ox} to further decrease the gate length while retaining sufficient gate controllability. Yet, the Si T_{body} of SOI requires continuously thinning down to improve the short channel effects, which cause a technology challenge. One simple solution is to form the three-dimensional FinFET that has an even thinner Si Fin down to 6 nm T_{body} thickness. Both the sidewalls and top surface of Fin are covered by gate oxide and metal gate, which have better gate electrostatic control of the channel carriers than SOI. Therefore, the FinFET has been applied to 22 to 3 nm technology nodes rather than using SOI. Figure 1 shows the FET's technology flow. The figure shows the bulk MOSFET, SOI MOSFET, and three-dimensional FinFET.



(**a**) (**b**) (**c**)

Figure 1. The evolution of device structure from (**a**) planar MOSFET on bulk Si wafer, (**b**) planar MOSFET ultra-thin body SOI, and (**c**) 3D FinFET.

The continuous downscaling decreases the transistor's source and drain distance and causes lowered drain voltage (V_D) and power consumption of $V_DI_D/2$, where I_D is the drain current. The ultimate V_D downscaling is limited by the voltage drop in the sub-threshold region, which has an idea SS of 60 mV/dec. Although the SS can be improved by using the charges in ferroelectric gate dielectric [3], the relatively large thickness and crystallized high-κ gate dielectric are the major concerns to integrate into highly scaled FinFET and nanosheet FET. On the other hand, a high V_D is required to deliver enough output power for wireless communication [4]. The highly scaled FinFET and nanosheet FET cannot sustain the high V_D that will cause the device to break down. Fortunately, the Vacuum Nano-Triode device in the Nothing-On-Insulator (NOI) configuration may overcome this challenge by operating at a relatively high V_D [5,6]. This transistor showed excellent performance up to 4 THz, which is crucial for sixth-generation (6G) wireless communication. For logic application, further research and development to lower the V_D and V_G to less than 1 V is required for an NOI transistor.

Nanosheet transistors are the best solution to overcome these challenges of FinFET scaling, enabling higher drive currents [7,8]. The nanosheet FETs are suitable for high computing needs due to their compatibility with various single-crystal materials such as Si, SiGe, two-dimensional (2D) MoS_2 and WS_2, among others. The downscaling of Si nanosheet complementary FET is planned to 1 nm node, but further shrinking of the device is limited by the implementation of 2D materials and hyper-numerical-aperture (NA) extreme-ultraviolet (EUV) lithography. Unfortunately, there is no known solution to form a defect-free and uniform monolayer 2D material over the 12-inch wafer. The rapidly increasing cost and huge power consumption are the major bottlenecks to realizing a hyper-EUV lithography system. Those downscaling barriers may be overcome by the monolithic three-dimensional (3D) structure [9–11] that mimics the bio-brain. In addition, monolithic 3D integrated circuits (ICs) can provide better performance of higher operating frequencies and lower power consumption than their 2D counterparts [10]. Yet the poor μ_{eff} for a transistor made on the backend dielectric of an IC is the basic challenge. Previously,

we reported on the high field-effect mobility (μ_{FE}) of SnO_2 [9,12,13] and SnON FET [14], but the μ_{eff} is the required important data for transistors. The μ_{eff} can give crucial information on electron-scattering mechanisms over the wide range of inversion charge (Q_e). The Q_e or gate voltage (V_G)-dependent μ_{eff} is also essential for device modeling used for IC design. In this report, we measure the transistor output current over a wide range of V_G, equivalent to a Q_e close to 1×10^{13} cm^{-2}, to analyze the device-scaling mechanism. The major findings beyond our previous published paper [14] are the much lower μ_{eff} decay rate at high E_{eff} than SiO_2/Si, high-κ/InGaAs, high-κ/2D MoS_2 nFETs, etc. This is the new discovery that was never reported in any FET device. In order to deliver a high transistor output current for an FET and drive the IC speed quickly, preserving the high μ_{eff} at a high Q_e is critical. The physical limitation of a MOSFET is that the μ_{eff} degrades monotonically with increasing charge density. However, the MOSFET must be biased at high charge density to deliver a high output current. For the first time, this fundamental restriction is overcome by using a higher κ and high μ_{eff} channel. The nanocrystalline SnON n-type FET (nFET) has a μ_{eff} value as high as 325 cm^2/V-s at 5×10^{12} cm^{-2} electron density (Q_e) and 5 nm nanosheet body thickness (T_{body}). At the same T_{body}, this μ_{eff} is significantly higher than single-crystalline Si, InGaAs, 2D MoS_2, 2D WS_2 and 2D WSe_2. The high μ_{eff} is due to the >10× higher κ value of SnO_2 than other semiconductor materials of Si, GaAs, InP, GaN and SiC, which can lower the channel effective field (E_{eff}) by >10× even at high Q_e. In addition, the small 0.29 m_o effective mass (m_e*), large overlapped s-orbitals and low phonon scattering may also play important roles to increase the mobility, although the μ_{eff} depends on both extrinsic and intrinsic scattering mechanisms and will be discussed in the following sessions. The N^{3-} anions having a higher p orbital energy can move up the valance band (E_V) from first-principle QM calculation, and the oxygen vacancy levels (V_o) residing in the channel layer are reduced to improve the μ_{eff}. The 3D 400 °C process of SnON does not require a single crystal substrate; thus, the energy consumption is many orders of magnitude lower than today's single-crystal Si wafer. The record-high μ_{eff} and quasi-2D thickness SnON nFET suggest potential monolithic three-dimensional (3D) and embedded dynamic random access memory (DRAM) to mimic the 3D bio-brain structure.

2. Materials and Methods

The bottom-metal-gate/high-κ/[SnON or SnO_2] nFETs were made by depositing a 50 nm TaN as the bottom gate using reactive sputtering. Then, a 45 nm high-κ HfO_2 and 3 nm SiO_2 were deposited as a gate dielectric using an electron-beam evaporator and annealed at 400 °C in an oxygen environment for 30 min using a furnace. Furthermore, a SnON or SnO_2 channel layer were deposited by reactive sputtering using a Sn target (purity 99.99%) followed by post-annealing at 400 °C. The Sn sputter power, argon flow rate and process pressure are fixed at 30 W, 24 sccm and 7.6×10^{-3} torr, respectively. The O_2 flow rate is fixed at 20 sccm for the SnO_2 channel layer, while 7.6% nitrogen content (30 sccm of Nitrogen) was used for the deposition of the SnON channel layer. The source-drain electrodes of 80 nm thick Al were deposited and patterned using a thermal coater. The fabricated nFET has a channel length of 50 μm and width of 500 μm. The material properties of SnON and SnO_2 were studied using first-principle QM calculations [15]. The Broyden–Fletcher–Goldfarb–Shanno (BFGS) minimization technique has been used to optimize the crystal structure [16]. It was performed using the self-consistent field approach, which has a convergence precision of 1×10^{-8} eV/atom. This study made use of the generalized gradient approximation (GGA) with local density approximation plus the U (LDA + U) approach. The energy cutoff for enlarging the plane wave basis set was set at 430 eV, and the Brillouin zone was sampled using the Monkhorst–Pack k-point approach with the k-points (6 × 6 × 5) [17]. The electrical characterization of the nFET device was analyzed using the HP4155B semiconductor parameter analyzer with the help of a probe station.

3. Results

Figure 2 displays the cross-sectional transmission electron microscopy (TEM) image of the 5 nm SnON/SiO_2/HfO_2 stack on a Si substrate. A nanocrystalline uniform SnON layer of 5 nm ultra-thin thickness was observed. To enlarge the I_{ON}, a gate insulator with high-κ [18] HfO_2 was employed to reduce the operating voltage. Between the channel and gate dielectric, SiO_2 with 3 nm thickness was deposited to limit the remote phonon scattering occurring from the high-κ gate dielectric [19].

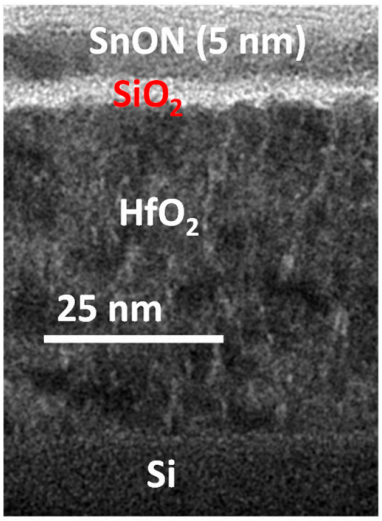


Figure 2. TEM image of the 5 nm-SnON/SiO_2/HfO_2 stack.

Using first-principle calculations based on density functional theory, the density of state (DOS) for SnO_2 and SnON were examined as shown in Figure 3a,b, respectively. For convenience of analysis, the valence band maximum (VBM) was adjusted to zero. The lower conduction states close to the conduction band minimum (CBM) in SnO_2 and SnON were primarily produced from Sn 5s orbitals [20], while the localized states immediately above the VBM in SnON had a predominance of N 2p character. The N states in the valence band, principally N 2p character, are the main cause of the bandgap reduction in SnON. SnO_2 and N_2-doped SnO_2 have effective electron masses (m_e*) of 0.41 m_o and 0.29 m_o, respectively, where m_o is the free electron mass which is reported in our previous work [14]. The m_e* for SnON is evidently smaller than SnO_2, which could result in a larger μ_{eff}.

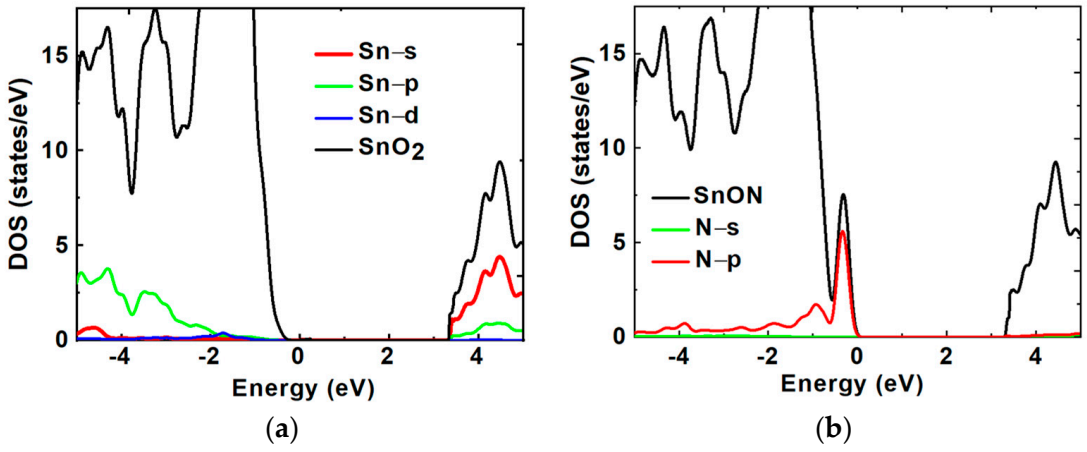


Figure 3. (**a**) DOS of Sn in SnO_2 and (**b**) DOS of N in SnON calculated using first-principle density functional theory.

Figure 4a–c depict the transistor's drain current versus drain voltage (I_D–V_D) characteristics at various V_G for SnO_2 and SnON nFETs with T_{body} of 5 nm and 7 nm. A clear pinch-off and good current saturation were measured. The SnON nFETs displayed higher I_D compared to the control SnO_2 device. Because the metal gate/high-κ was made at the same run with identical gate oxide capacitance, the only reason to cause a significantly higher I_D at the same V_G–V_T of SnON nFET is due to the higher μ_{eff}.

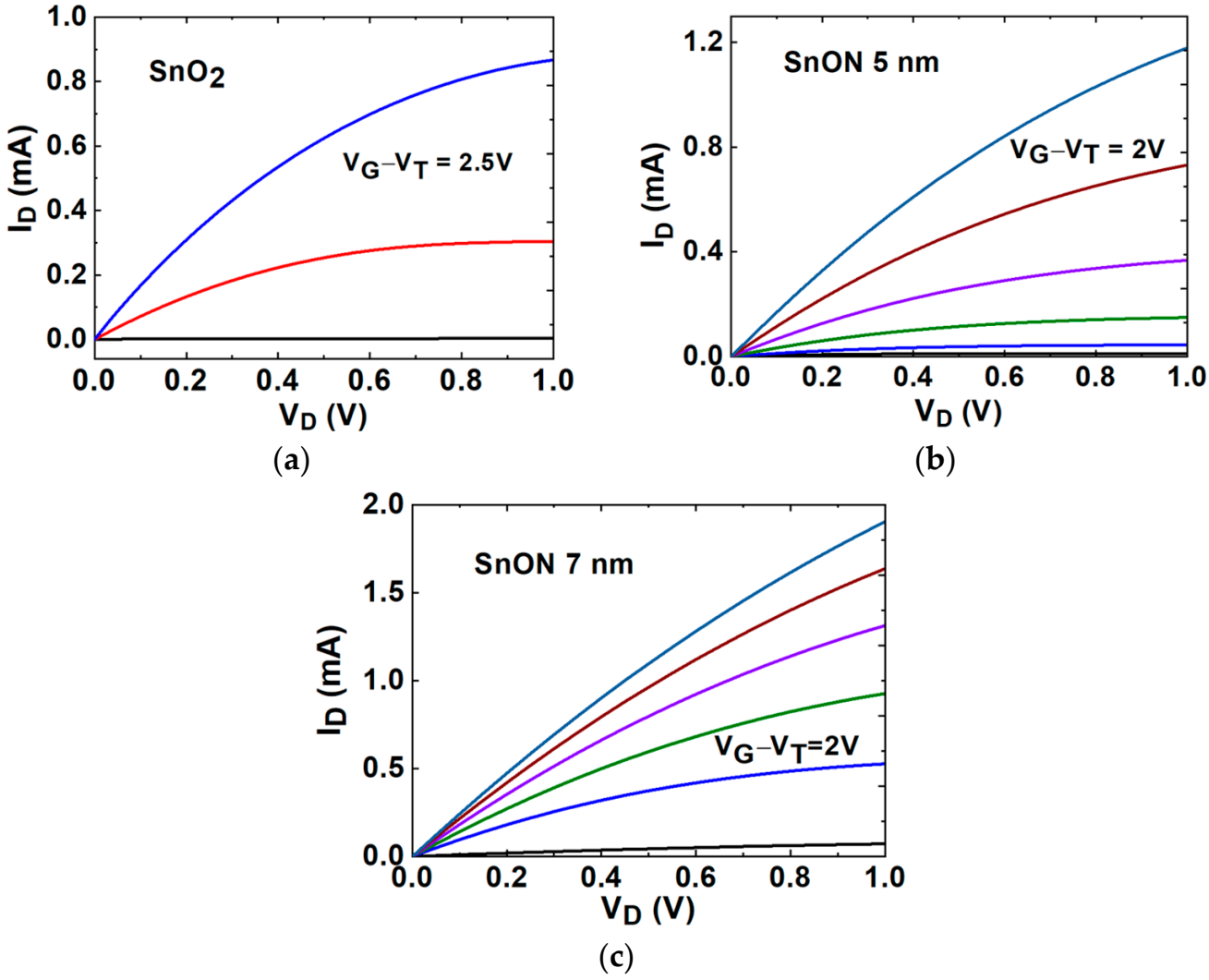


Figure 4. I_D-V_D output characteristics for (**a**) TaN/HfO_2/5 nm-SnO_2 nFET, (**b**) TaN/HfO_2/5 nm-SnON nFET, and (**c**) TaN/HfO_2/7 nm-SnON nFET.

Figure 5a,b display gate current versus gate voltage (I_G–V_G) and I_D–V_G transfer characteristics at a V_D = 0.1 V for SnON nFETs with T_{body} values of 5 and 7 nm, respectively. A large on-current/off-current (I_{ON}/I_{OFF}) is achieved in 5 nm T_{body} thickness, which is important for IC application. For accurate μ_{eff} extraction, a fat FET (long channel FET) [21] made in IC fabs must be used to lower the difference between physical and electrical gate length, where the source and drain depletion regions can decrease the electrical gate length. This is the reason why mA is used for the *Y*-axis rather than mA/μm.

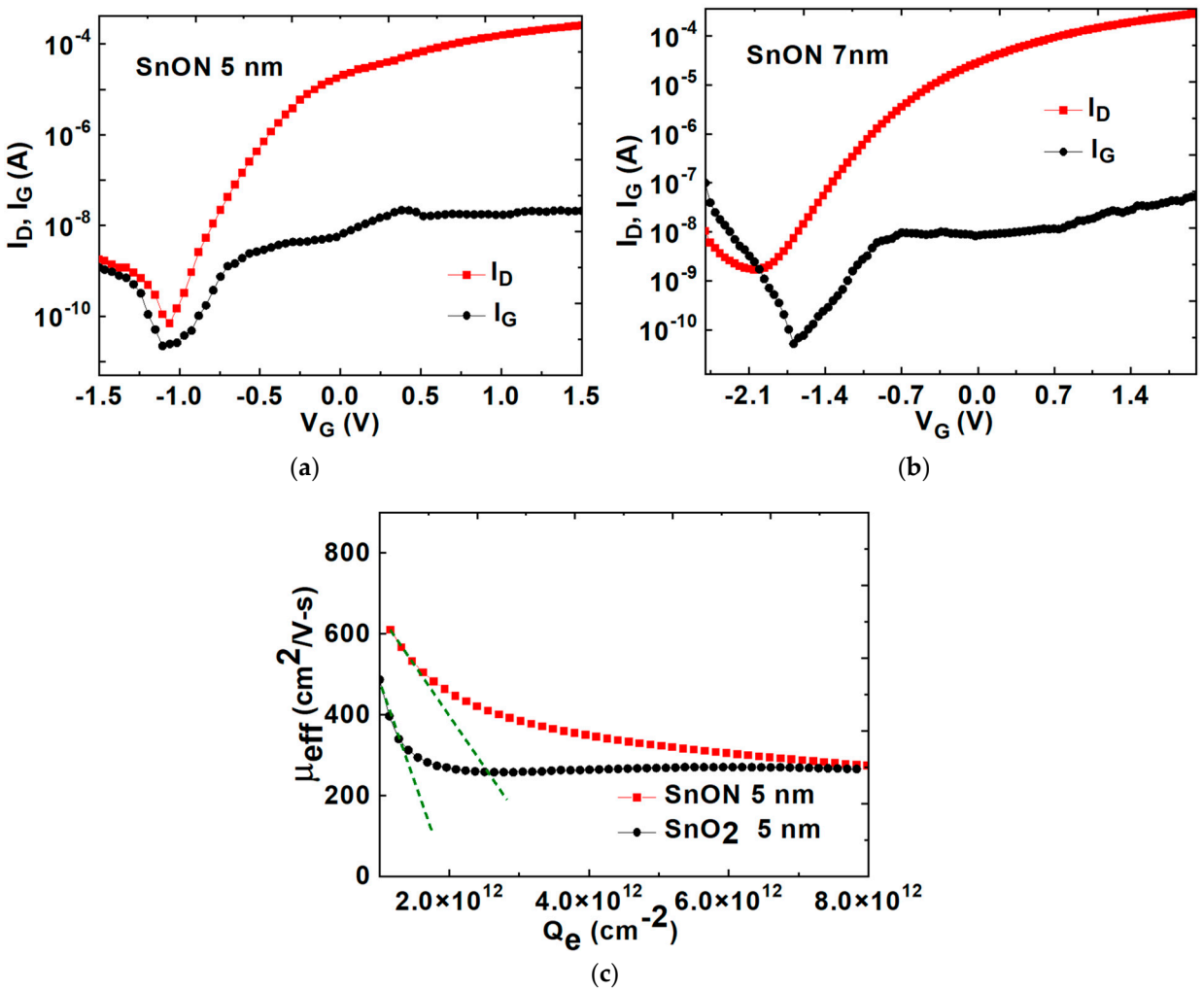


Figure 5. I_G–V_G and I_D–V_G transfer characteristics for (**a**) TaN/HfO_2/5 nm SnON nFET and (**b**) TaN/HfO_2/7 nm SnON nFET; and (**c**) μ_{eff} versus Q_e for 5 nm SnO_2 and SnON nFETs (The dashed lines are used to check the μ_{eff} dependence on Q_e).

The FET's scattering mechanism is further analyzed by the μ_{eff} as a function of Q_e. The μ_{eff} values of FET are calculated according to the conventional metal-oxide-semiconductor (MOS) FET model [22–24]:

$$\mu_{eff} = \frac{L_G}{W_G} \frac{dI_{DS}}{dV_{DS}} \frac{1}{C_{ox}(V_{GS} - V_T)}, \quad (1)$$

where L_G and W_G are the length and width of the conducting channel, respectively, and Cox is the gate-oxide capacitance. As shown in Figure 5c, at low to medium Q_e, the nFET's μ_{eff} of SnO_2 is significantly lower than that of the SnON one. The SnO_2 nFET shows much faster μ_{eff} degradation with increasing Q_e. Although the oxide charges in a high-κ dielectric are responsible for lower μ_{eff} than the conventional SiO_2 gate dielectric [25–28], such a μ_{eff} reduction is most significant at high Q_e rather than at low Q_e. It is reported that the μ_{eff} at low E_{eff} or Q_e is due to Coulomb scattering from charged impurities [24]. The potential reason for such a larger μ_{eff} of SnON nFET than that of SnO_2 may be related to the lower charged V_o. By injecting non-oxide nitrogen anions, SnON can lower the defect trap densities. This allows for the removal or passivation of Vo through substitutional alloying with N^{3-} to improve the μ_{eff}, as seen in Figure 6. Similar observations were also found with ZnON [29]. It is well known that the transition SiO_x between Si and SiO_2 gives a positive fixed oxide charge, which is primarily due to structural V_o defects in the oxide

layer. Such a positive V_o charge close to the valence band in SnON may be lowered by an extra N-band, as shown in the DOS of Figure 3b.

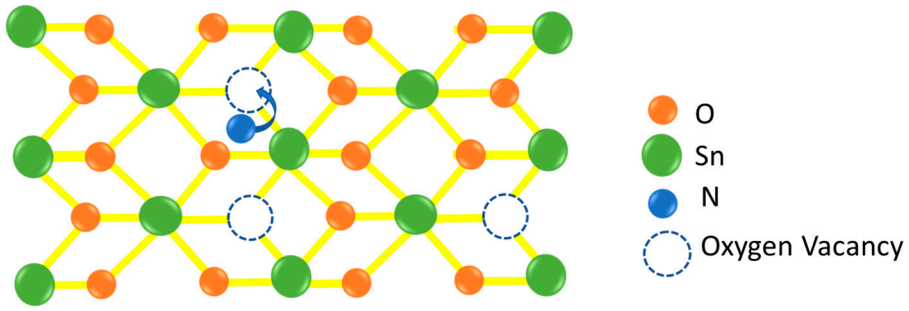


Figure 6. Diagrammatic sketch of substitutional alloying of oxygen vacancy with nitrogen atoms.

Figure 7a further plots $1/\mu_{eff}$ versus Q_e. The $1/\mu_{eff}$ has a linear relationship with Q_e.

$$1/\mu_{eff} = kQ_e, \quad (2)$$

where k is the proportional constant. The inversely linear relationship between μ_{eff} and Q_e is exactly the same as the μ_{eff} dependence on ionized impurity concentrations [24]. This confirms that the charged V_o in SnO_2 is the major reason to cause Coulomb scattering. The large slope in the low Q_e is related to charged V_o scattering in SnO_2 that is lowered by adding N^{3-} anions. We further compare the μ_{eff}–Q_e dependence using Equation (2) for universal SiO_2/bulk-Si, SiO_2/Si-on-Insulator (SOI), high-κ/SnO_2, and high-κ/SnON nFETs. As shown in Figure 7b, μ_{eff} values as high as 357 and 325 cm^2/V-s are achieved at Q_e of 5×10^{12} cm^{-2} and T_{body} of 7 and 5 nm, respectively. At 1×10^{13} cm^{-2} Q_e, an ultra-thin 5 and 7 nm thickness, the μ_{eff} of high-κ/SnON nFET is 85% and 95% of universal SiO_2/bulk-Si nFET. The μ_{eff} scattering mechanism of SiO_2/bulk-Si nFET at low, medium, and high E_{eff} is due to Coulomb, phonon, and surface scattering, respectively. The universal μ_{eff} of SiO_2/bulk-Si nFET depends on standard $Q_e^{-0.3}$ in medium Q_e, which becomes $Q_e^{-0.6}$ dependence at high Q_e to 1×10^{13} cm^{-2}. However, the μ_{eff} decay rate of high-κ/SnO_2 and high-κ/SnON nFETs at high Q_e is much slower than universal SiO_2/bulk-Si and thin-body SOI nFETs [30].

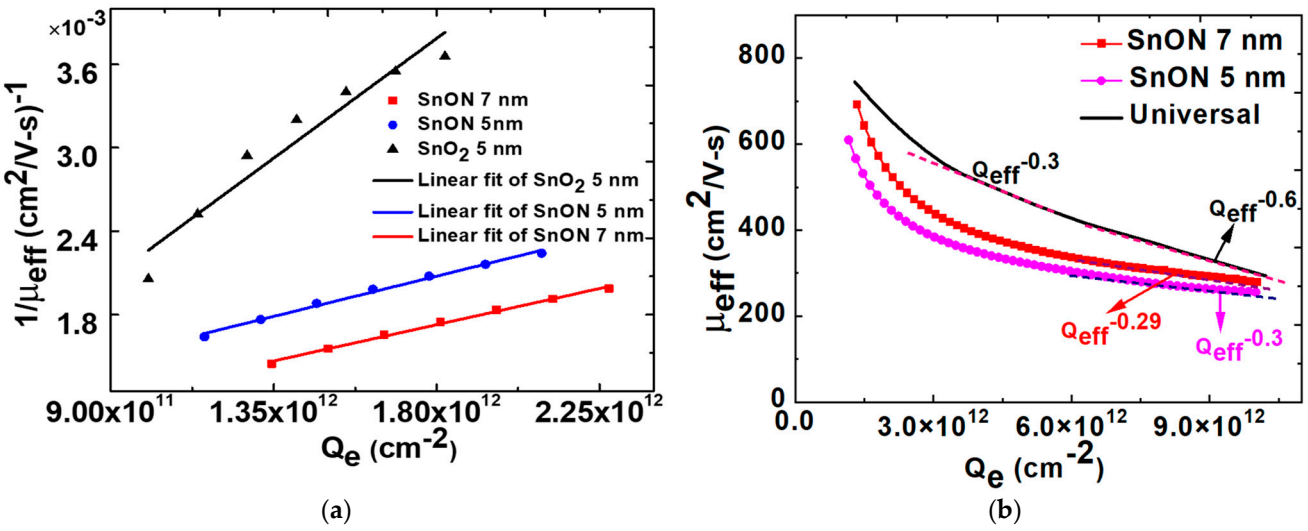


Figure 7. (**a**) $1/\mu_{eff}$ versus Q_e plot for 5 nm SnO_2, 5 nm SnON and 7 nm SnON nTFTs and (**b**) μ_{eff} versus Q_e with different channel thickness of SnON nFET and comparison with universal nFETs (The dashed lines are used to fit and check the μ_{eff} dependence on Q_e).

To understand such abnormal slow μ_{eff} dependence on Q_e, we further measured the dielectric constant, κ of 5 nm SnO_2. Figure 8 shows the measured capacitance under various voltages at 1 kHz. The SnO_2 has a κ of 123, which is >10× larger than major semiconductors of Si, GaAs, InP, GaN, SiC, etc. [31–35]. This high κ value is also close to the reported data in the literature [36]. The novel discovery μ_{eff} dependence on $Q_e^{-0.30}$ at a high Q_e range is due to the >10× higher κ value to keep a high-κ/SnON nFET at the medium E_{eff} range. Here, the E_{eff} is proportional to Q_e:

$$E_{eff} = \frac{|Q_{semi}|}{\varepsilon_{semi}} = \frac{1}{\varepsilon_{semi}}\left(\frac{|Q_e|}{n} + \left|N_{dep}\right|\right) \approx \frac{1}{\varepsilon_{semi}}\left(\frac{|Q_e|}{n}\right) @ \text{high } Q_e, \quad (3)$$

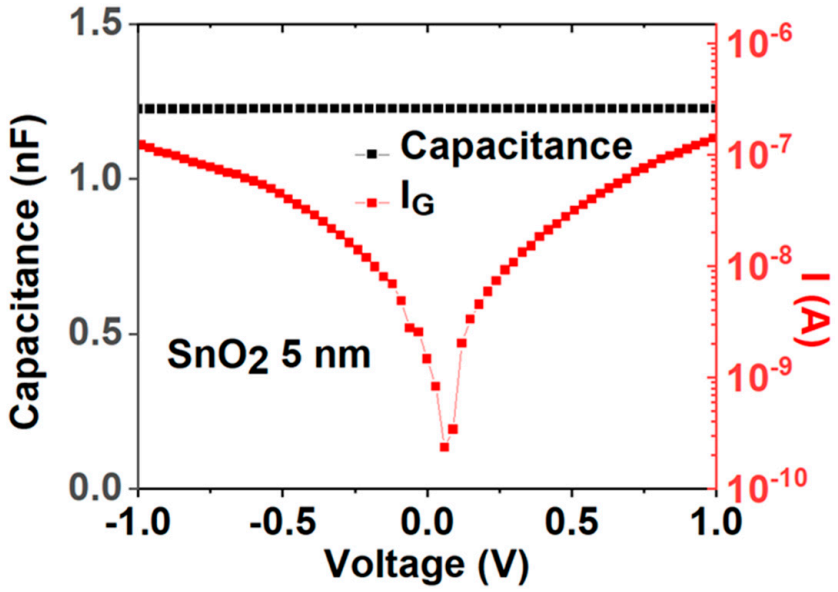


Figure 8. C-V and I-V plot for Ni/SnO_2/Ni capacitor.

The ε_{semi} equals $\varepsilon_0\kappa$, where ε_{semi} and ε_0 are the permittivity of the semiconductor and free space, respectively. N_{dep} is the depletion charge of charged impurities in doped Si or charged V_o in major oxide semiconductors. The *n* factor in SiO_2/bulk-Si is equal to 2 and 3 for nMOSFET and pMOSFET, respectively. This equation is basically Gauss's law. The Gauss law is one of Maxwell's equations [37], which cannot be changed in an ultra-thin T_{body} device. This is exactly the reason why this equation has been widely used for 2D material FETs [38]. The significantly much higher κ value than most of the commercial semiconductors of Si, GaAs, InP, GaN and SiC allows the channel electrons to keep a low E_{eff}. This in turn keeps the electron wave-functions in the conduction channel [39] away from the gate-oxide/semiconductor interface and decreases the gate-oxide surface scattering. The carrier transport in ultra-thin body or 2D materials is determined by both the intrinsic mobility of phonon scattering and Coulomb scattering from the charge impurities and defects, the extrinsic effects of remote phonon scattering from high-κ dielectrics, and the surface roughness scattering from the oxide/semiconductor interfaces. For InGaAs nFET at a relatively thick T_{body} larger than 20 nm [40], the μ_{eff} is dominated by intrinsic phonon scattering. Therefore, the μ_{eff} of InGaAs nFET is higher than that of Si due to the smaller m_e*. However, for a thin InGaAs T_{body} less than 20 nm, the extrinsic scattering of interface defects limits the μ_{eff} [40]. In this report, the μ_{eff} values of a thin T_{body} of 7 and 5 nm are still higher than those of a Si and InGaAs nFET. The reason can only be ascribed to the superb intrinsic property of >10× smaller E_{eff} to lower the interface scattering, smaller m_e*, and high phonon limited mobility. The device modeling of this record high μ_{eff} nFET may be developed by future researchers, as such figures are typical for the past InGaAs FET [41–43] and 2D materials FETs [44,45].

It is important to notice that the μ_{eff} values of SnON nFET are the highest values among all the oxide-based semiconductors. This is due to the smaller m_e^* and larger phonon energy (E_{op}) [46], which lead to a high μ_{eff}:

$$\mu_{op} \propto \frac{1}{\left(\frac{m_e^*}{m_0}\right)^{\frac{3}{2}}} \frac{\exp\left(\frac{E_{op}}{kT}\right) - 1}{\left(\frac{E_{op}}{kT}\right)^{\frac{1}{2}}} \quad (4)$$

The E_{op} is higher than ZnO, GaN, and SiC [47–50].

The total μ_{eff} can be expressed as:

$$\frac{1}{\mu_{total}} = \frac{1}{\mu_{intrinsic}} + \frac{1}{\mu_{extensic}} = \frac{1}{\mu_{Vo}} + \frac{1}{\mu_{op}} + \frac{1}{\mu_{high-k}} + \frac{1}{\mu_{sr}} \quad (5)$$

Here, the μ_{Vo} is the FET's mobility that is limited by the charged V_o. This μ_{Vo} is extremely important at low to medium Q_e, as shown in Figure 5c. In ultra-thin body 2D materials, the carrier transport is determined by phonon scattering from the dielectrics and Coulomb scattering from charged defects such as vacancies [51]. Ma and Jena et al. predicted that high-κ dielectrics provide an effective screening of the charge impurities, leading to high Coulomb-limited mobility [52]. Moreover, owing to the low formation energy of the chalcogen vacancy, a large amount of sulfur vacancies is commonly observed in synthesized 2D MoS_2, which can induce short-range scattering and degrade carrier mobility [53]. Thus, Equation (4) is also derived for 2D systems. In addition, the excellent matching of Equation (4) with measurements is also reported for SnO_2 nFET with a 5 nm channel thickness [46].

The radius of the s-orbital increases with the increasing principle quantum number n with n^2 dependence, so the overlapping s-orbitals are stronger for SnO_2 than for ZnO [20]. The theoretical background of high mobility in a metal-oxide semiconductor is due to the overlapped s-orbitals [54]. The larger s-orbitals and the stronger overlapping of electron clouds lead to high mobility. We have earlier reported that in SnON, the localized states just above the valence band maximum (VBM) have a predominant N 2p character and the lower conduction states near the conduction band minimum (CBM) were mostly derived from Sn 5s orbitals, which results in high electron mobility in SnON [14]. This explains why the mobility of SnON nFET is significantly larger than that of ZnO.

Table 1 compares the device performances. The wide energy bandgap (E_G) nanocrystalline SnON nFET has the highest μ_{eff} among single-crystal Si, InGaAs, 2D MoS_2, and 2D WS_2. It is noticed that the next 2 nm node commercial nanosheet nFET will use single-crystalline Si with a T_{body} of 7 nm, since the μ_{eff} decreases with decreasing T_{body} with a T_{body}^6 dependence [55]. The μ_{eff} of high-κ/SnON nFETs is 2.7 times higher than that of Si nFET at the same 5 nm T_{body}, which could be used for downscaling the nanosheet T_{body}. The wide-E_G SnON also leads to large I_{ON}/I_{OFF}, as shown in Figure 5a.

Table 1. Comparisons of 2D semiconductor performances with our present work at Q_e of 5×10^{12} cm^{-2}.

Semiconductor Material	E_G (eV)	m_{eff} (m_o)	Dielectric Const. κ	μ_{eff} (cm^2/V-s) @5 nm
SnON (this work)	~3.3	~0.29	123	325
Si [38]	1.12	1.08	11.7	120
MoS_2 [38]	1.8	~0.5	4~8 (2~5 layers)	184
WS_2 [38]	1.4	0.33	-	234
InGaAs [38]	0.75	0.042	12.9	200

The searching for high μ_{eff} material nFET leads to extensive research on high-mobility InGaAs nMOSFET [41]. The reason why the material failed to be implemented into manufacture is due to the relatively inferior oxide/semiconductor interface, which caused μ_{eff} degradation in thin T_{body} rather than the enhanced tunneling. For a T_{body} value less than 20 nm, the g_m and g_m/T_{body} of Si FinFET are still better than those of InGaAs FinFET [40]. In the InGaAs FET [40–42] and 2D material FET [56] evolution, a long gate length device was first made to investigate the intrinsic property, such as μ_{eff}, I_{on}/I_{off} and SS. The downscaling of InGaAs nFET took a decade-long study, until the μ_{eff} degraded fast with decreasing ultra-thin T_{body}. After the record-high μ_{eff} is reported, researchers and engineers in IC fabs will follow up to study the small gate length devices and the potential to be implanted in the gate all around (GAA) nanosheet FET.

Because the remarkably high μ_{eff} SnON nFET is the new data, there is no modeling on the experimental data reported so far. In the scientific field of semiconductor devices, the experiments are carried out before mobility modeling. The modeling work following experiments can be evident from past high-mobility InGaAs nFET development. The superb μ_{eff} in a 5 nm ultra-thin T_{body} will attract modeling experts in the future works. It is well known that the device modeling is developed after MOSFET fabrication in the IC industry, such as the widely used Berkeley Short-channel IGFET Model (BSIM). In this model, there are many fitting parameters to be measured experimentally in addition to physically based equations. As the devices become smaller in each technology node by Moore's law, new versions of device models are developed to accurately reflect the transistor's behavior. Therefore, the BSIM model has changed continuously for the past three decades. Such device modeling requires years of experience from both academic and IC fabs' team works, which is beyond our group's capability. Similar device modeling followed by this record-high μ_{eff} nFET may be developed later by theoreticians, as these results are typical for the past InGaAs FET [40–43] and 2D materials FETs [44,45].

4. Conclusions

In this work, we demonstrated record-high μ_{eff} 5 nm T_{body} nFETs, made on IC's backend for monolithic 3D usage. For the first time, the μ_{eff} of 325 $cm^2/V\text{-}s$ at 5×10^{12} cm^{-2} Q_e is 2.7 times higher than that of Si nFET at the same T_{body} of 5 nm. This was achieved using a wide-E_G 5 nm quasi-2D SnON channel processed at 400 °C. Such a high FET's μ_{eff} is due to the smaller 0.29 m_o, overlapped large-radius s-orbitals, and low polar optical phonon scattering. In addition, a smaller μ_{eff} decay rate than SiO_2/bulk-Si nFET at high Q_e was found, owing to the <10× E_{eff} by >10× higher κ value. The record-high μ_{eff} SnON nFETs formed on IC's backend signal empowering technology for monolithic 3D ICs.

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