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Mechanism of Random Telegraph Noise in 22-nm FDSOI-Based MOSFET at Cryogenic Temperatures

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Abstract: In the emerging process-based transistors, random telegraph noise (RTN) has become a critical reliability problem. However, the conventional method to analyze RTN properties may not be suitable for the advanced silicon-on-insulator (SOI)-based transistors, such as the fully depleted SOI (FDSOI)-based transistors. In this paper, the mechanism of RTN in a 22-nm FDSOI-based metal–oxide–semiconductor field-effect transistor (MOSFET) is discussed, and an improved approach to analyzing the relationship between the RTN time constants, the trap energy, and the trap depth of the device at cryogenic temperatures is proposed. The cryogenic measurements of RTN in a 22-nm FDSOI-based MOSFET were carried out and analyzed using the improved approach. In this approach, the quantum mechanical effects and diffuse scattering of electrons at the oxide–silicon interface are considered, and the slope of the trap potential determined by the gate voltage relation is assumed to decrease proportionally with temperature as a result of the electron distribution inside the top silicon, per the technology computer-aided design (TCAD) simulations. The fitted results of the improved approach have good consistency with the measured curves at cryogenic temperatures from 10 K to 100 K. The fitted trap depth was 0.13 nm, and the decrease in the fitted correction coefficient of the electron distribution proportionally with temperature is consistent with the aforementioned assumption.

Keywords: random telegraph noise (RTN); fully depleted silicon-on-insulator (FDSOI); cryogenic temperatures; trap depth; inversion layer thickness

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1. Introduction

With the scaling down and utilization of high-k metal gates (HKMGs) in metal-oxide-semiconductor field-effect transistors (MOSFETs), the occurrence of random telegraph noise (RTN), especially the generation of random telegraph signals (RTSs), is becoming a critical reliability problem in analog integrated circuits (ICs), digital ICs, and the memories due to the shift in threshold voltage from the capture and emission of carriers by traps inside the gate oxide [1–5]. Moreover, RTN is also a severe reliability problem in cryogenic quantum computing applications [6]. The integrated quantum processor, which contains quantum bits (q-bits) and peripheral circuits, operates at cryogenic temperatures. Because its peripheral circuits are based on MOSFETs, the RTN from the cryogenic MOSFETs may cause reliability problems in the integrated quantum processor. Besides, RTN can also cause reliability problems in other applications whose peripheral circuits are based on MOSFETs, such as the two-dimensional material-based applications [7–10]. Past research studying the mechanism of RTN on cryogenic bulk MOSFETs has already been presented, where primarily, the properties of RTN, such as time constants and trap depth, have been discussed [6,11,12]. However, the mechanism of RTN in the cryogenic fully depleted silicon-on-insulator (FDSOI) MOSFET, especially the relationship between the time constant, trap energy, and trap depth, is hardly mentioned in recent works. Considering that FDSOI MOSFETs are promising candidates for the peripheral circuits in integrated quantum

processors, it is necessary to investigate the mechanism of RTN at cryogenic temperatures in FDSOI MOSFETs.

In MOSFETs, both bulk and FDSOI MOSFETs, traps in the gate oxide may capture carriers from the channel or release (emit) carriers into the channel. This capture or emission of carriers can temporarily change the threshold voltage of the MOSFET, leading to a temporary shift in the drain current, as shown in Figure 1. The duration of capture and emission of carriers are denoted by t_c and t_e, respectively.

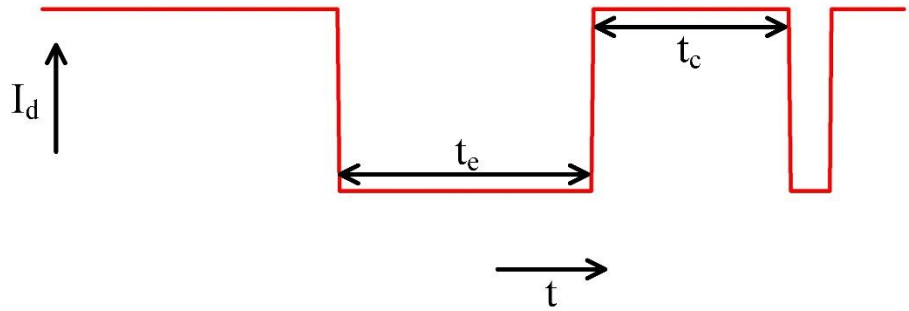


Figure 1. RTN in MOSFET, t_c is the capture time and t_e is the emission time.

The t_c and t_e appear randomly, obeying the Poisson distribution, and can be described as [13,14]:

$$P_\alpha(t_\alpha) = \frac{1}{\tau_\alpha}\exp\left(-\frac{t_\alpha}{\tau_\alpha}\right) \quad \alpha = c \text{ or } e \tag{1}$$

where, τ_α is the time constant of the capture or emission; $P_\alpha(t_\alpha)dt_\alpha$ is the probability that the capture or emission occurs between t_α and $t_\alpha + dt_\alpha$. To extract τ_α, the distribution of t_α is fitted to Equation (1), as shown in Figure 2. The measured data are the counts of different t_α; by fitting them to the Poisson distribution, τ_α can be extracted.

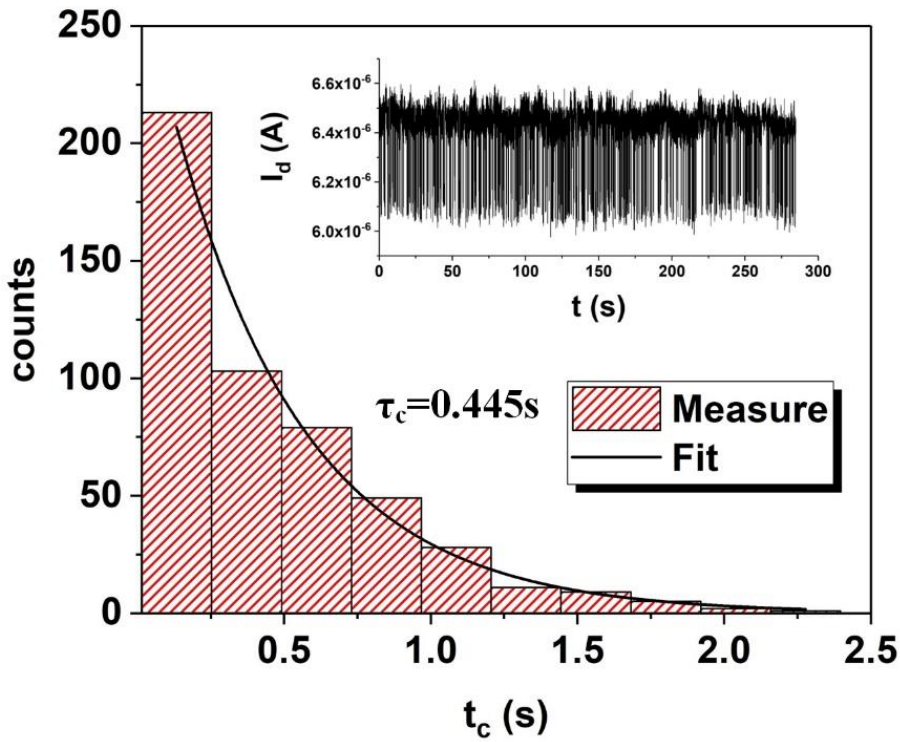


Figure 2. The fitting of τ_α to the Poisson distribution and the extraction of τ_α.

To understand the relationship between the time constants τ_α and the trap energy E_T, the grand partition function is adopted. According to the grand partition function, the relationship between τ_α and E_T can be described by [13,15]:

$$\tau_c = \tau_0 \cdot [1 + e^{(E_T - E_F)/kT}] \tag{2}$$

$$\tau_e = \tau_0 \cdot \left[1 + e^{-(E_T - E_F)/kT}\right] \tag{3}$$

where, τ_0 is the characteristic time constant, E_F is the Fermi level, k is the Boltzmann constant, and T is the absolute temperature. Then, it can be inferred that:

$$ln\frac{\tau_c}{\tau_e} = \frac{(E_T - E_F)}{kT} \tag{4}$$

In the bulk MOSFET, when the device is operating in the strong inversion region (assuming the potential of the inversion layer is pinned to the gate voltage), the trap depth can be extracted by Equation (4) [16–20]:

$$\frac{X_T}{t_{ox}} = -\frac{kT}{q}\frac{d\ ln\tau_c/\tau_e}{d\ V_g} \tag{5}$$

where, X_T is the trap depth from the oxide-silicon interface, t_{ox} is the thickness of the gate oxide, V_g is the gate voltage, and q is the charge of the electron.

Although the bulk MOSFET and the FDSOI MOSFET are both planar devices, it is still uncertain as to whether the relationship between the RTN time constants, the trap energy, and the trap depth in the bulk MOSFET (Equation (5)) is suitable for the FDSOI MOSFET or not. Thus, exploring an appropriate method to analyze the RTN properties in FDSOI MOSFETs, especially at cryogenic temperatures, is meaningful for reliability analysis in emerging SOI processes.

In this paper, the mechanism of RTN at cryogenic temperatures on a 22-nm FDSOI MOSFET is reported, and the relationship between the time constants, trap energy, and trap depth at cryogenic temperatures of the 22-nm FDSOI MOSFET is discussed. The paper is organized as follows: Section 2 introduces the experimental configuration of the cryogenic measurement of RTN in the 22-nm FDSOI MOSFET. Next, Section 3 presents the measurement results and the problems with the analysis of RTN. Then, Section 4 attempts to explain the problems mentioned in Section 3 and proposes an improved approach to analyzing the RTN in FDSOI MOSFETs at cryogenic temperatures. Finally, Section 5 makes a brief conclusion.

2. Experimental Configurations

To measure the RTN properties of the 22-nm FDSOI MOSFET at cryogenic temperatures, the device under test (DUT) of this experiment is based on the 22FDX technology from Global Foundries [21,22]. The 22FDX technology provides low threshold voltage (LVT) and super low threshold voltage (SLVT) N- and P-type MOSFETs with different gate lengths (L) and widths (W). For the experiment, a LVT N-type MOSFET with W/L = 160 nm/20 nm was chosen. The main dimensions of the chosen MOSFET are shown in Table 1. In Table 1, t_{Si}, t_{BOX}, t_{OX}, L_g, and W are the thickness of the top silicon, thickness of the buried oxide (BOX), thickness of the gate oxide, channel length, and channel width, respectively. The 22FDX technology uses the HKMG technology, where the traps inside the high-k gate oxide or at the oxide-silicon interface make the RTN problems worse.

The cryogenic experiments were conducted between 10 K and 100 K on a Lakeshore cryogenic probe station, and the RTN measurements were performed using the Keithley 4200A. To explore the changes in the properties related to RTN, in the measurements, the drain voltage was kept constant while V_g was varied and the time-domain characteristics of the drain current were sampled.

Table 1. The main dimensions of the 22-nm FDSOI MOSFET.

Name	Geometric Size
t_{Si}	7 nm
t_{BOX}	25 nm
t_{OX}	2 nm
L_g	20 nm
W	160 nm

3. Measurement Results

In the cryogenic RTN measurements on the FDSOI, it was observed that the t_c (high) and t_e (low) vary with the change in the V_g and T, which reveals that the time constants also vary with the V_g and T, as shown in Figure 3. Thereafter, the time constants were extracted as introduced in Section 1.

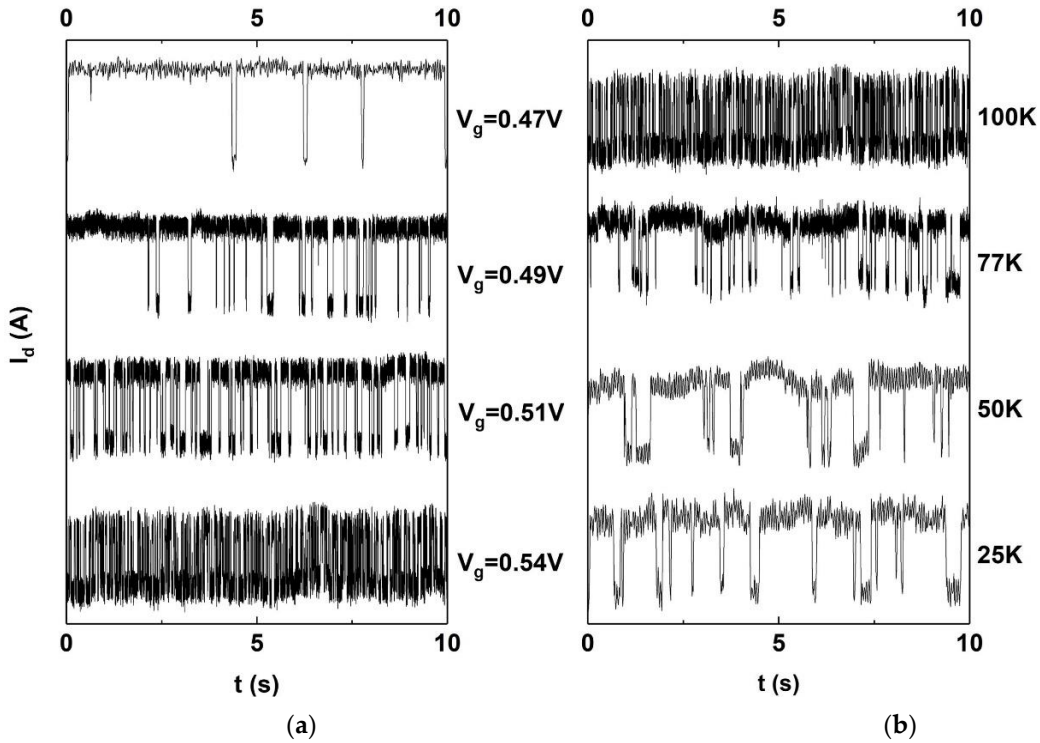


Figure 3. Time-domain graphs of RTN. (**a**) varying V_g at 100 K; (**b**) varying T at V_g = 0.54 V.

Figure 4 illustrates the relationship of τ_c and τ_e with V_g at different cryogenic temperatures from 10 K to 100 K. With the increase in temperature, both τ_c and τ_e decrease. However, when V_g decreases, τ_c increases exponentially, while τ_e only slightly increases. This is different from the phenomenon in [23] where τ_c increases exponentially and τ_e decreases exponentially with the decrease in V_g at room temperature.

At room temperature, the characteristic time constant, τ_0, in Equations (2) and (3) is considered as constant that will not change with V_g. Thus, the relationship of τ_c and τ_e with V_g according to Equations (2) and (3) would be different than what was observed in this study: if one time constant increases exponentially, the other should decrease exponentially [23]. However, according to the thermal activation theory [13], τ_0 may not be treated as a constant at cryogenic temperatures. Figure 5 shows the plots of τ_0 with V_g of the FDSOI at different cryogenic temperatures. It can be seen that τ_0 decreases exponentially as V_g increases, which may be due to the increasing carrier density in the inversion layer with the increase of V_g.

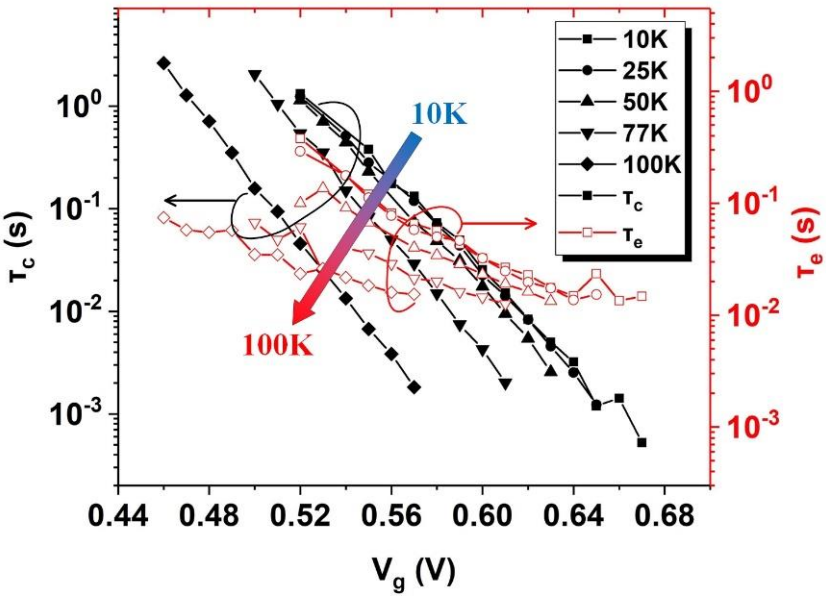


Figure 4. Plots of τ_c (solid) and τ_e (open) versus V_g at cryogenic temperatures ranging from 10 K to 100 K.

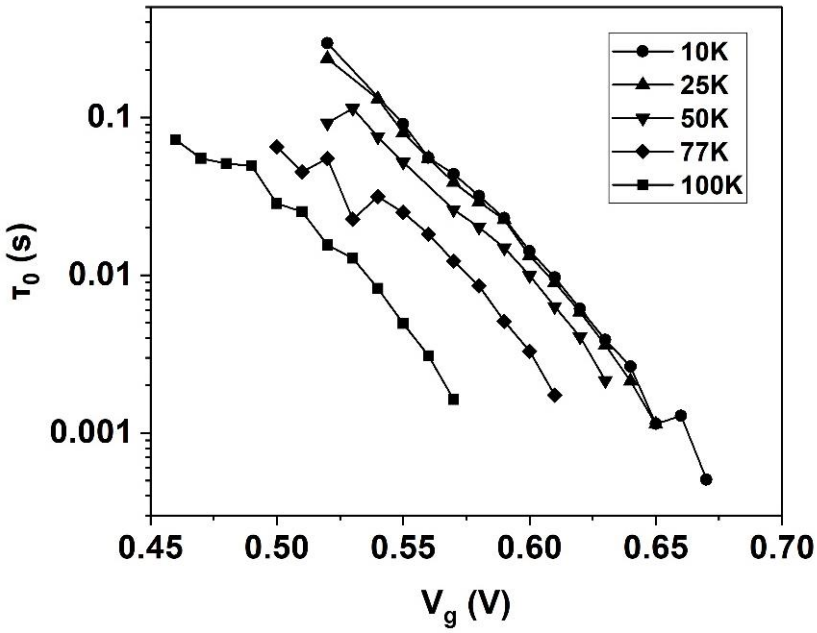
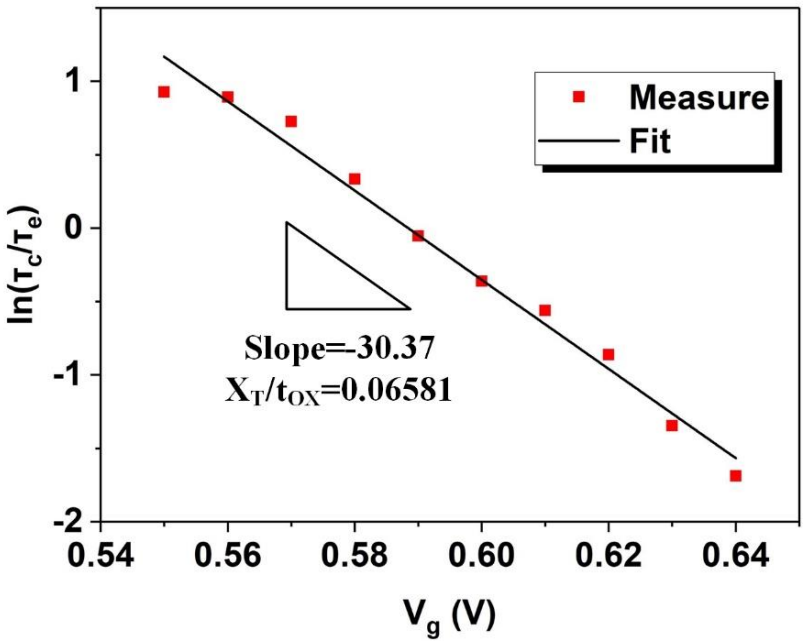
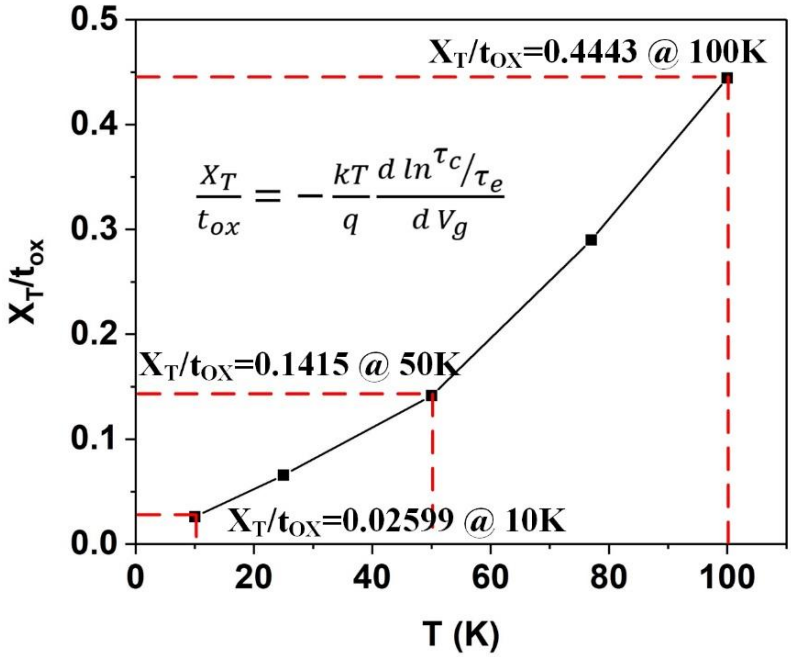


Figure 5. τ_0 versus V_g at different cryogenic temperatures.

To extract the trap depth using Equation (5), $ln\frac{\tau_c}{\tau_e}$ is calculated, plotted by V_g, and linearly fitted to extract the slope. Figure 6a shows the fitting procedure at T of 25 K. The slope of the fitted curve is −30.37, and according to Equation (5), $\frac{X_T}{t_{ox}}$ is 0.06581. Similarly, the trap depth was extracted for cryogenic temperatures of 10 K, 50 K, 77 K, and 100 K as well. The absolute errors between measured and linearly fitted $ln\frac{\tau_c}{\tau_e}$ curves are illustrated in Table 2. The total maximum error and total average error are 0.63789 and 0.13280, respectively. As shown in Figure 6b, $\frac{X_T}{t_{ox}}$ falls from 0.4443 at 100 K to 0.02599 at 10 K. This is an abnormal phenomenon because the location of the traps in the gate oxide is unlikely to change with the change in temperature in the FDSOI MOSFET. Moreover, this also implies that the conventional method of extracting the trap depth—i.e., Equation (5)—is probably not suitable for newer types of MOSFETs, such as the FDSOI MOSFET.



(**a**)



(**b**)

Figure 6. (**a**) Extracting the trap depth at 25 K; the extracted slope is −30.37, and the calculated $\frac{X_T}{t_{ox}}$ is 0.06581. (**b**) Plot showing the calculated trap depth versus temperature.

Table 2. The absolute errors between measured and linearly fitted $ln\frac{\tau_c}{\tau_e}$ curves.

Temperature	Max Error	Average Error
100 K	0.21419	0.06411
77 K	0.63789	0.17187
50 K	0.29193	0.10779
25 K	0.30458	0.14914
10 K	0.54369	0.17107
Total	0.63789	0.13280

4. Discussion

In the conventional trap depth extraction, the basic assumptions are that the potential of the inversion layer is constant and the peak of the carrier density is at the oxide-silicon interface, which are suitable for the bulk MOSFET. To extract the trap depth, from Equation (4), the first derivative of $ln\frac{\tau_c}{\tau_e}$ with respect to V_g is taken [24]:

$$\frac{d\ ln^{\tau_c}/_{\tau_e}}{d\ V_g} = -\frac{q}{kT}\frac{d\ V_{Trap}}{d\ V_g} \tag{6}$$

where, V_{Trap} stands for the trap potential.

Figure 7 illustrates the geometric relationship between the V_g, V_{Trap}, and X_T. It can be inferred easily that:

$$V_{trap} = V_{inv} + E_{OX}\ X_T = \frac{V_g - V_{inv}}{t_{OX}}\ X_T + V_{inv} = V_g\frac{X_T}{t_{OX}} + V_{inv}\left(1 - \frac{X_T}{t_{OX}}\right) \tag{7}$$

where, V_{inv} is the inversion layer potential and E_{OX} is the electrical field intensity inside the gate oxide. Assuming that V_{inv} is constant in the strong inversion region, the first derivative of V_{trap} with respect to V_g is:

$$\frac{d\ V_{Trap}}{d\ V_g} = \frac{X_T}{t_{OX}} \tag{8}$$

Thus, combining Equations (6) and (8), Equation (5) can be derived.

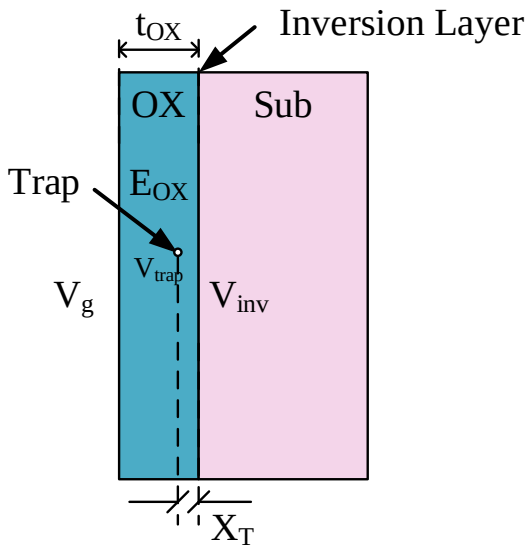


Figure 7. The geometric relationship between V_g, V_{Trap}, and X_T.

Nevertheless, these assumptions, while suitable for bulk MOSFETs, may not be precise for FDSOI MOSFETs. In the FDSOI MOSFET, carriers are generated inside the entire top silicon, and most of the time the peak of the carrier density is not located at the oxide-silicon interface due to quantum processes [25–31] and diffuse scattering [32,33]. Thus, the geometric relationship shown in Figure 7 is not precise for FDSOI MOSFETs, and Equation (8) cannot be derived by the differentiation of V_{trap}. Although Equations (5), (7) and (8) are no longer suitable for the FDSOI MOSFET, the slope of V_{trap} to V_g is still an important trap-related characteristic.

To explore the influence of the carrier distribution in the top silicon on the slope of V_{trap} with respect to V_g, TCAD simulations were performed. The TCAD simulations were implemented by Silvaco TCAD tools, and the quantum correction method is a self-consistent coupled Schrodinger-Poisson model. The device structure in the simulations is consistent with the real geometric size of a 22-nm FDSOI MOSFET as shown in Table 1.

Figure 8 illustrates the simulated results. The cutline of the electron density is in the middle of the channel, and the trap depth is set to 0.1 nm. Figure 8a, shows the results of the simulation that was performed at 10 K while the quantum correction was disabled. It can be observed that the peak of the electron density is at the oxide-silicon interface, resulting in a $V_{trap} - V_g$ slope of 0.05333. The slope from the simulation has good consistency with Equation (8), where $\frac{X_T}{t_{OX}}$ = 0.05. In Figure 8b, the temperature of the simulation was 100 K and the quantum correction was enabled. As a result of the quantum correction and the diffuse scattering, the peak of the electron density is at about 1.5 nm from the interface, and the electrons are distributed in a wide range inside the top silicon. Hence, the slope of $V_{trap} - V_g$ is greater than that in Figure 8a: 0.6138. The simulations demonstrate that the slope of V_{trap} with respect to V_g is strongly related to the distribution of electrons inside the top silicon and that the non-ideal electron distribution caused by quantum processes and diffuse scattering significantly increases the slope. Therefore, according to Equation (8), non-ideal electron distribution can also lead to a significant increase in the calculated trap depth.

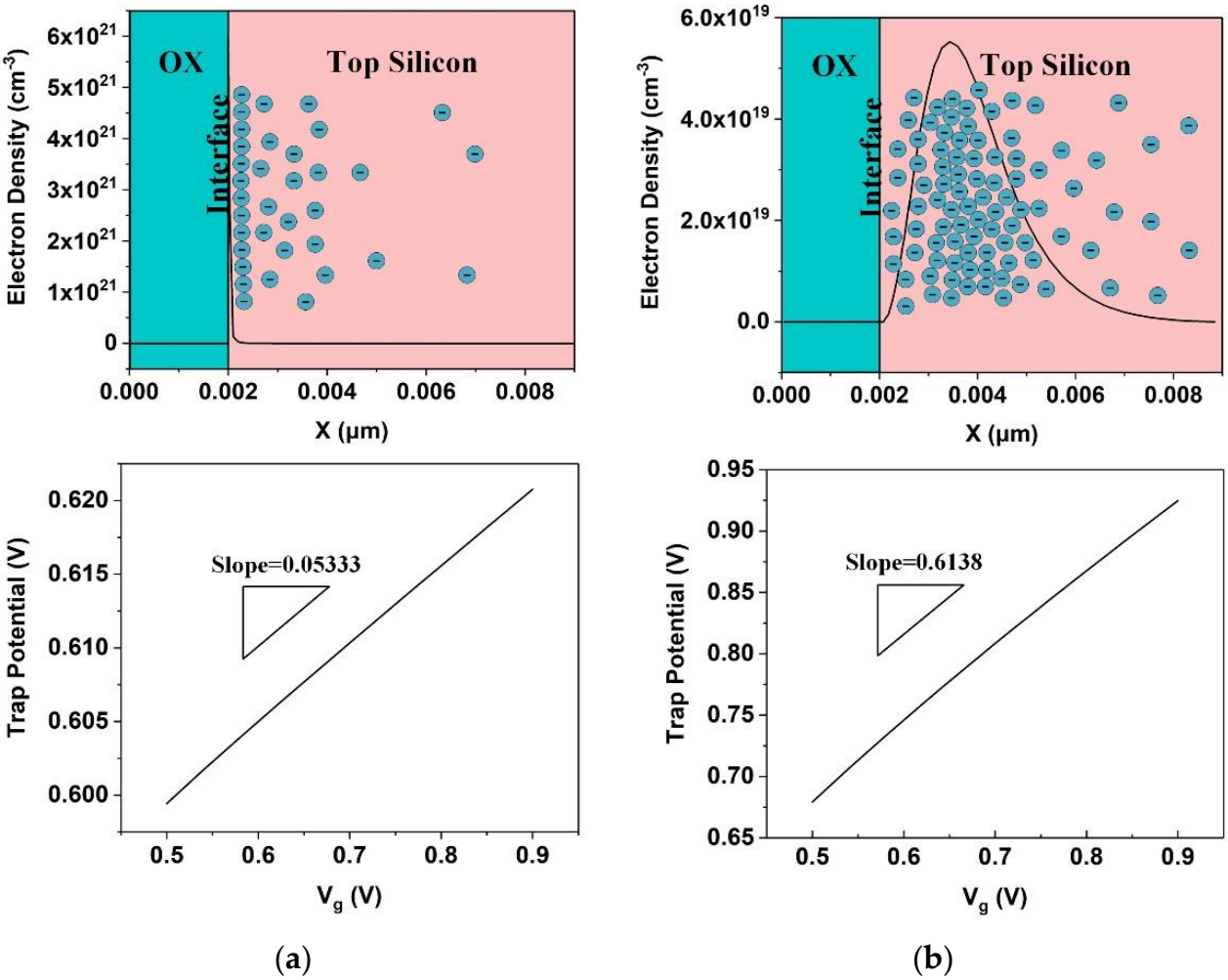


Figure 8. The results of the simulations: (**a**) at 10 K with quantum correction disabled and (**b**) at 100 K with quantum correction enabled.

As shown in Figure 6b, the calculated trap depth increases with temperature. Additionally, as discussed before, the non-ideal distribution of electrons increases the calculated trap depth as well. Thus, it can be deduced that temperature has a significant influence on the electron distribution inside the top silicon. To investigate this relationship, the quantum mechanical processes and diffuse scattering are first considered. Previous studies

have already proven that the inversion layer thickness—the average distance from the oxide-silicon interface to electrons—is primarily a result of quantum mechanics and diffuse scattering and decreases with the reduction in temperature [13,29,32,33], which means that the electrons in the inversion layer are closer to the oxide-silicon interface at lower temperatures. In other words, the electron distribution is closer to ideal as the temperatures decreases. This may explain the reduction in the calculated trap depth and in the $V_{trap} - V_g$ slope in Figure 6b.

To explain this issue quantitatively, an improved approach to analyzing the trap depth calculated from the RTN time constants is to be derived. To simplify the calculation, the potential at the inversion layer thickness is assumed to be pinned with respect to V_g. In addition, the electrical field intensity inside the inversion layer is also assumed to be uniform. These assumptions indicate that the electrons inside the inversion layer are gathered at the inversion layer thickness, i.e., the electron distribution has been ignored. Figure 9 illustrates an improved schematic showing the geometric relationship between V_{Trap} and X_T in the inversion region.

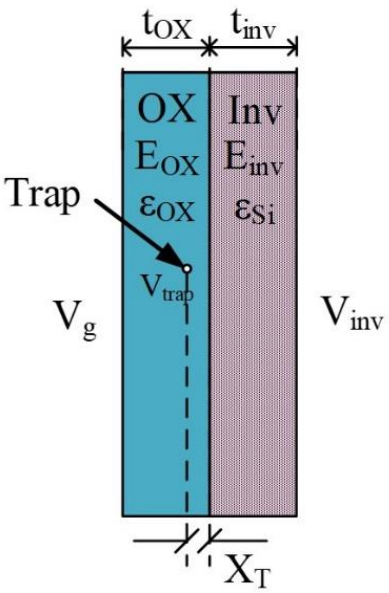


Figure 9. The geometric relationship between the V_g, V_{Trap}, and X_T considering the inversion layer thickness.

From Figure 9, it can be derived:

$$E_{OX} = \frac{\varepsilon_{Si}}{\varepsilon_{OX}} E_{inv} \tag{9}$$

$$V_{trap} = V_{inv} + E_{inv}\, t_{inv} + E_{OX}\, X_T \tag{10}$$

where, ε_{Si}, ε_{OX}, E_{inv}, and t_{inv} are the relative permittivity of silicon, the relative permittivity of the gate oxide, the effective electrical field intensity inside the inversion layer, and the inversion layer thickness, repectively. Combining Equations (9) and (10):

$$V_{trap} = V_{inv} + E_{inv}\left(t_{inv} + \frac{\varepsilon_{Si}}{\varepsilon_{OX}} X_T \right) \tag{11}$$

here, t_{inv} is a result of both quantum mechanics and diffuse scattering.

As discussed in [28], the inversion layer thickness due to quantum mechanics at room temperature can be given by:

$$t_{inv,QM} = \frac{\beta}{\alpha + {E_{inv}}^{0.7}} \tag{12}$$

where, α = 1 (MV/cm)$^{0.7}$ and β = 1.9 × 10^{-7} cm (MV/cm)$^{0.7}$ [13]. demonstrates that the inversion layer thickness decreases linearly with the reduction in temperature. Thus, in this deduction, it is also assumed that the inversion layer thickness from quantum mechanics decreases linearly with temperature:

$$t_{inv,QM} = \frac{\beta}{\alpha + {E_{inv}}^{0.7}} \frac{T}{T_0} \tag{13}$$

where, T_0 is the room temperature.

According to [32], the inversion layer thickness from the diffuse scattering is:

$$t_{inv,DS} = \frac{3kT}{2qE_{inv}} \tag{14}$$

So, the total inversion layer thickness becomes:

$$t_{inv} = t_{inv,QM} + t_{inv,DS} = \left(\frac{\beta}{\alpha + {E_{inv}}^{0.7}} + \frac{3kT_0}{2qE_{inv}} \right) \frac{T}{T_0} \tag{15}$$

E_{inv} is given by:

$$E_{inv} = \frac{V_{gtx} + \alpha(V_{th} - V_{FB} - \varphi_s)}{2t_{OX}} \tag{16}$$

$$V_{gtx} = \eta v_t \ln\left[1 + \exp\left(\frac{V_g - V_{th}}{\eta v_t} \right)\right] \tag{17}$$

where, V_{gtx} is the auxiliary function of V_g, α is a fitting parameter, V_{th} is the threshold voltage, V_{FB} is the flat band voltage, φ_s is the surface potential, η is the sub-threshold swing parameter, and v_t is the thermal voltage.

Based on the above discussion, with the increase in temperature, the electrons spread further into the top silicon, which was not considered in the former deduction. Thus, the correction of the electron distribution applied to Equation (11) is:

$$V_{trap} = V_{inv} + E_{inv}\left(t_{inv} + \frac{\varepsilon_{Si}}{\varepsilon_{OX}} X_T \right) + \chi V_g \tag{18}$$

where, χ is the correction coefficient of the electron distribution and represents the influence of the electron distribution on the $V_{trap} - V_g$ slope.

To fit the measured $ln\frac{\tau_c}{\tau_e}$, both sides of Equation (6) is integrated with respect to V_g as:

$$ln\frac{\tau_c}{\tau_e} = -\frac{q}{kT}\left(V_{Trap} - V_{inv}\right) + Con. \tag{19}$$

where, $Con.$ is the constant of integration. Combining Equations (15), (18) and (19) the fitting to the measured $ln\frac{\tau_c}{\tau_e}$ can be implemented.

Figure 10 shows the fitted plots of $ln\frac{\tau_c}{\tau_e}$ by V_g applying the fitting parameters in Table 3 and using the above deductions. They show good consistency with the measured plots for temperatures from 10 K to 100 K. The absolute errors between measured and fitted $ln\frac{\tau_c}{\tau_e}$ curves are shown in Table 4. The total maximum error is 0.62478 and the total average error is 0.10574, which are respectively lower by 2.1% and 20% than the conventional linear fitting. Among the fitting parameters, the fitted X_T is 0.13 nm and χ decreases from 0.34 to 0 with the reduction in temperature. The trend shown by χ indicates that the electrons are further spread into the top silicon with the rise in temperature, which is consistent with the former assumption.

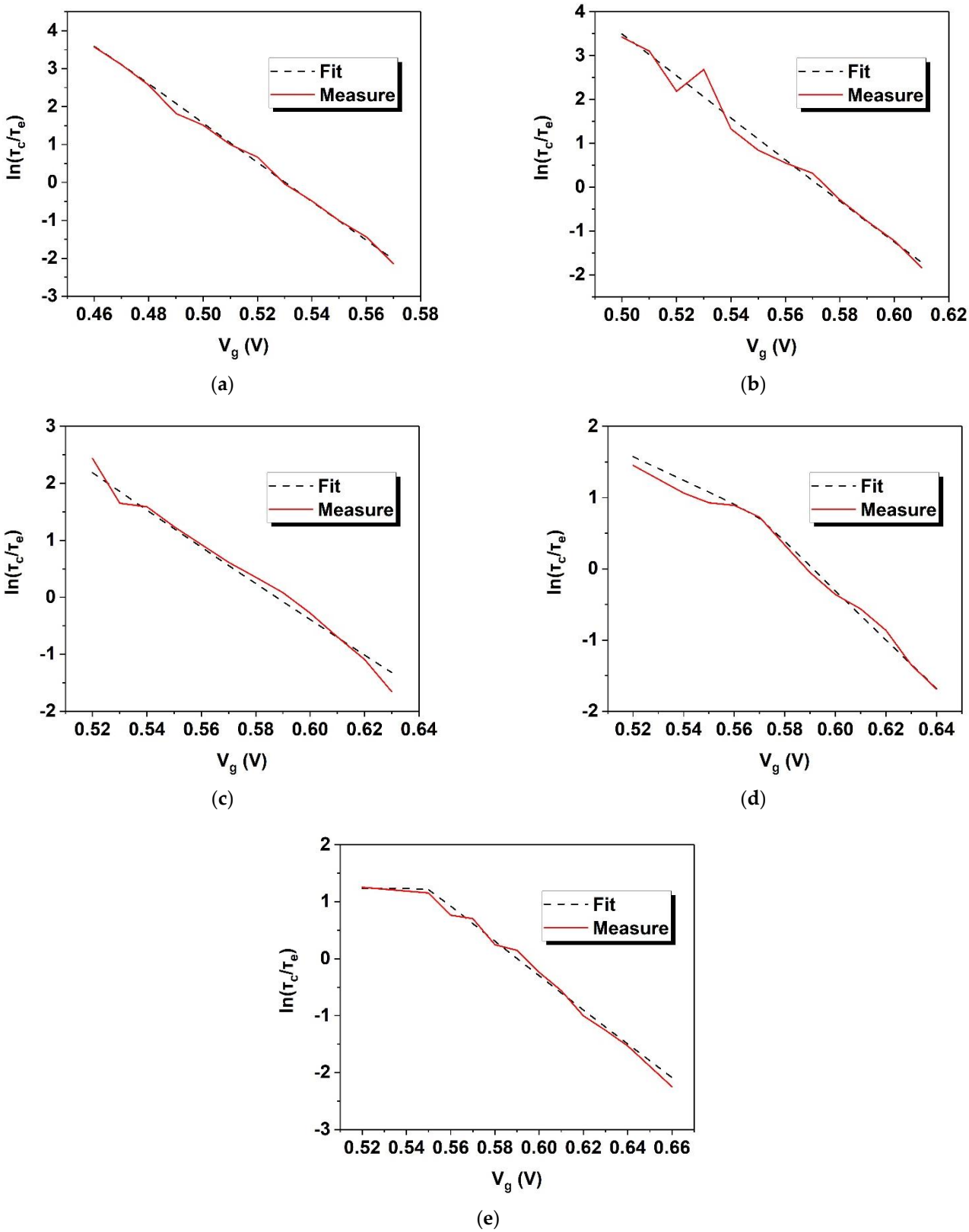


Figure 10. The measured (solid) and fitted (dashed) plots applying the parameters in Table 3 at temperatures of: (**a**) 100 K; (**b**) 77 K; (**c**) 50 K; (**d**) 25 K; and (**e**) 10 K.

Table 3. The parameters for fitting the $ln\frac{\tau_c}{\tau_e}$ plots.

Temperature	T_0	α	β	η	t_{OX}	X_T	V_{th}	$\alpha(V_{th}-V_{FB}-\varphi_s)$	χ	*Con.*
100 K	300 K	1 $(MV/cm)^{0.7}$	1.9×10^{-7} $cm(MV/cm)^{0.7}$	1.3	2 nm	0.13 nm	0.46 V	0.05 V	0.34	24.1
77 K							0.49 V	0.05 V	0.23	23.3
50 K							0.49 V	0.08 V	0.08	15.2
25 K							0.57 V	0.12 V	0.036	14.3
10 K							0.55 V	0.15 V	0	7.85

Table 4. The absolute errors between the measured and fitted $ln\frac{\tau_c}{\tau_e}$ curves.

Temperature	Max Error	Average Error
100 K	0.27068	0.06977
77 K	0.62478	0.17199
50 K	0.3329	0.12734
25 K	0.17920	0.07727
10 K	0.16343	0.08233
Total	0.62478	0.10574

5. Conclusions

This paper proposes an improved approach to analyze the RTN properties of 22-nm FDSOI-based MOSFETs at cryogenic temperatures. The cryogenic measurements of RTN on a 22-nm FDSOI-based DUT have been performed and analyzed using the improved approach, where the quantum mechanical effects and diffuse scattering of electrons inside the top silicon are considered. The basic assumption here is that the V_{trap} by V_g slope decreases proportionally with temperature due to the variation of the electron distribution, according to the TCAD simulation results. Applying the improved approach, the calculated and fitted plots of $ln\frac{\tau_c}{\tau_e}$ by V_g is found to be consistent with the measured results earlier. The fitted X_T was 0.13 nm, and the decrease of χ proportional with temperature indicates consistency with the aforementioned assumption. This work provides a new method for analyzing RTN in FDSOI MOSFETs at cryogenic temperatures, which plays a significant role in the reliability of cryogenic integration circuits such as the integrated quantum processor. It can also be used to analyze reliability problems caused by RTN in emerging SOI MOSFETs at the cryogenic temperatures.

Author Contributions: Data curation, B.Z. and L.S.; Methodology, Y.M.; Supervision, J.B. and M.L.; Validation, H.W. and L.F.; Writing—original draft, Y.M. All authors have read and agreed to the published version of the manuscript.

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Conflicts of Interest: The authors declare no conflict of interest.

References

1. Higashi, Y.; Momo, N.; Sasaki, H.; Momose, H.S.; Ohguro, T.; Mitani, Y.; Ishihara, T.; Matsuzawa, K. Unified transient and frequency domain noise simulation for random telegraph noise and flicker noise using a physics-based model. *IEEE Trans. Electron. Dev.* **2014**, *61*, 4197–4203. [CrossRef]
2. Simicic, M.; Weckx, P.; Parvais, B.; Roussel, P.; Kaczer, B.; Gielen, G. Understanding the impact of time-dependent random variability on analog ICs: From single transistor measurements to circuit simulations. *IEEE Trans. Very Large Scale Integr. Syst.* **2019**, *27*, 601–610. [CrossRef]
3. Simoen, E.; Claeys, C. The low-frequency noise behaviour of silicon-on-insulator technologies. *Solid-State Electron.* **1996**, *39*, 949–960. [CrossRef]
4. Fleetwood, D.M. Total-Ionizing-Dose Effects, Border Traps, and $1/f$ Noise in Emerging MOS Technologies. *IEEE Trans. Nucl. Sci.* **2020**, *67*, 1216–1240. [CrossRef]

5. Wirth, G. Time-Dependent Random Threshold Voltage Variation Due to Random Telegraph Noise. *IEEE Trans. Electron. Dev.* **2021**, *68*, 17–23. [CrossRef]
6. Michl, J.; Grill, A.; Stampfer, B.; Waldhoer, D.; Schleich, C.; Knobloch, T.; Ioannidis, E.; Enichlmair, H.; Minixhofer, R.; Kaczer, B.; et al. Evidence of Tunneling Driven Random Telegraph Noise in Cryo-CMOS. In Proceedings of the 2021 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 11 December 2021; pp. 31.3.1–31.3.4. [CrossRef]
7. Dastgeer, G.; Afzal, A.M.; Jaffery, S.H.A.; Imran, M.; Assiri, M.A.; Nisar, S. Gate modulation of the spin current in graphene/WSe2 van der Waals heterostructure at room temperature. *J. Alloys Compd.* **2022**, *919*, 165815. [CrossRef]
8. Dastgeer, G.; Shahzad, Z.M.; Chae, H.Y.; Kim, H.; Ko, B.M.; Eom, J. Bipolar Junction Transistor Exhibiting Excellent Output Characteristics with a Prompt Response against the Selective Protein. *Adv. Funct. Mater.* **2022**, *32*, 2204781. [CrossRef]
9. Dastgeer, G.; Nisar, S.; Shahzad, Z.M.; Rasheed, A.; Kim, D.; Jaffery, S.H.A.; Wang, L.; Usman, M.; Eom, J. Low-Power Negative-Differential-Resistance Device for Sensing the Selective Protein via Supporter Molecule Engineering. *Adv. Sci.* **2022**, 2204779. [CrossRef]
10. Lv, C.; Hu, C.; Luo, J.; Liu, S.; Qiao, Y.; Zhang, Z.; Song, J.; Shi, Y.; Cai, J.; Watanabe, A. Recent advances in graphene-based humidity sensors. *Nanomaterials* **2019**, *9*, 422. [CrossRef]
11. Whitcombe, A.; Taylor, S.; Denham, M.; Milovanovic, V.; Nikolic, B. On-chip I–V variability and random telegraph noise characterization in 28 nm CMOS. In Proceedings of the 2016 46th European Solid-State Device Research Conference (ESSDERC), Lausanne, Switzerland, 12–15 September 2016; pp. 248–251. [CrossRef]
12. Li, Z.; Sotto, M.; Liu, F.; Husain, M.K.; Zeimpekis, I.; Yoshimoto, H.; Tani, K.; Sasago, Y.; Hisamoto, D.; Fletcher, J.D.; et al. Random-telegraph-noise by resonant tunnelling at low temperatures. In Proceedings of the 2017 IEEE Electron Devices Technology and Manufacturing Conference (EDTM), Toyama, Japan, 28 February–2 March 2017; pp. 172–174. [CrossRef]
13. Kirton, M.J.; Uren, M.J. Noise in solid-state microstructures: A new perspective on individual defects, interface states and low-frequency ($1/f$) noise. *Adv. Phys.* **1989**, *38*, 367–468. [CrossRef]
14. Simoen, E.; Kaczer, B.; Toledano-Luque, M.; Claeys, C. Random Telegraph Noise: From a Device Physicist's Dream to a Designer's Nightmare. *ECS Trans.* **2011**, *39*, 3–15. [CrossRef]
15. Luo, M.; Wang, R.; Guo, S.; Wang, J.; Zou, J.; Huang, R. Impacts of random telegraph noise (RTN) on digital circuits. *IEEE Trans. Electron. Dev.* **2015**, *62*, 1725–1732. [CrossRef]
16. Lee, S.; Cho, H.J.; Son, Y.; Lee, D.S.; Shin, H. Characterization of oxide traps leading to RTN in high-K and metal gate MOSFETs. In Proceedings of the 2009 IEEE International Electron Devices Meeting (IEDM), Baltimore, MD, USA, 7–9 December 2009; pp. 763–766. [CrossRef]
17. Nagumo, T.; Takeuchi, K.; Hase, T.; Hayashi, Y. Statistical characterization of trap position, energy, amplitude and time constants by RTN measurement of multiple individual traps. In Proceedings of the 2010 International Electron Devices Meeting, San Francisco, CA, USA, 6–8 December 2010; pp. 628–631. [CrossRef]
18. Chiu, H.F.; Wu, S.L.; Chang, Y.S.; Chang, S.J.; Huang, P.C.; Chen, J.F.; Tsai, S.C.; Lai, C.M.; Hsu, C.W.; Cheng, O. Effect of annealing process on trap properties in high-k/metal gate n-channel metal-oxide-semiconductor field-effect transistors through low-frequency noise and random telegraph noise characterization. *Jpn. J. Appl. Phys.* **2013**, *52 Pt 2*, 04CC22. [CrossRef]
19. Chiu, H.F.; Wu, S.L.; Chang, Y.S.; Chang, S.J.; Chen, J.F.; Tsai, S.C.; Hsu, C.H.; Lai, C.M.; Hsu, C.W.; Cheng, O. Impact of oxygen annealing on high-k gate stack defects characterized by random telegraph noise. *Appl. Phys. Lett.* **2012**, *101*, 5–8. [CrossRef]
20. Wu, S.-L.; Chiu, H.-F.; Chang, Y.-S.; Cheng, O. Defect properties of high-k/metal-gate metal-oxide-semiconductor field-effect transistors determined by characterization of random telegraph noise. *Jpn. J. Appl. Phys.* **2014**, *53*, 038005. [CrossRef]
21. Carter, R.; Mazurier, J.; Pirro, L.; Sachse, J.-U.; Baars, P.; Faul, J.; Grass, C.; Grasshoff, G.; Javorka, P.; Kammler, T.; et al. 22 nm FDSOI technology for emerging mobile, Internet-of-Things, and RF applications. In Proceedings of the 2016 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 3–7 December 2016; pp. 2.2.1–2.2.4. [CrossRef]
22. Wang, H.; Bi, J.; Bu, J.; Liu, H.; Zhao, F.; Cao, H.; Ai, C. Characteristics of 22 nm UTBB-FDSOI technology with an ultra-wide temperature range. *Semicond. Sci. Technol.* **2022**, *37*, 105004. [CrossRef]
23. Miki, H.; Yamaoka, M.; Frank, D.J.; Cheng, K.; Park, D.-G.; Leobandung, E.; Torii, K. Voltage and temperature dependence of random telegraph noise in highly scaled HKMG ETSOI nFETs and its impact on logic delay uncertainty. In Proceedings of the 2012 Symposium on VLSI Technology (VLSIT), Honolulu, HI, USA, 12–14 June 2012; Volume 12, pp. 137–138. [CrossRef]
24. Çelik-Butler, Z.; Vasina, P.; Amarasinghe, N.V. A method for locating the position of oxide traps responsible for random telegraph signals in submicron MOSFET's. *IEEE Trans. Electron. Dev.* **2000**, *47*, 646–648. [CrossRef]
25. Ma, Y.; Liu, L.; Yu, Z.; Li, Z. On the degeneracy of quantized inversion layer in MOS structures. *Solid-State Electron.* **2000**, *44*, 1925–1929. [CrossRef]
26. Ma, Y.; Li, Z.; Liu, L.; Yu, Z. Comprehensive analytical physical model of quantized inversion layer in MOS structure. *Solid-State Electron.* **2001**, *45*, 267–273. [CrossRef]
27. Toriumi, A.; Yoshimi, M.; Iwase, M.; Taniguchi, K.; Hamaguchi, C. Experimental determination of finite inversion layer thickness in thin gate oxide MOSFETS. *Surf. Sci.* **1986**, *170*, 363–369. [CrossRef]
28. Liu, W.; Jin, X.; King, Y.; Hu, C. An efficient and accurate compact model for thin-oxide-mosfet intrinsic capacitance considering the finite charge layer thickness. *IEEE Trans. Electron. Dev.* **1999**, *46*, 1070–1072. [CrossRef]
29. Stern, F. Self-consistent results for n-type Si inversion layers. *Phys. Rev. B* **1972**, *5*, 4891–4899. [CrossRef]
30. Ando, T.; Fowler, A.B.; Stern, F. Electronic properties of two-dimensional systems. *Rev. Mod. Phys.* **1982**, *54*, 437–672. [CrossRef]

31. Ma, Y.; Liu, L.; Tian, L.; Li, Z. Statistical analysis of quantized inversion layer in MOS devices with ultra-thin gate oxide and high substrate doping levels. In Proceedings of the IEEE Hong Kong Electron Devices Meeting, Hong Kong, China, 24 June 2000; pp. 126–129. [CrossRef]
32. Schwarz, S.A.; Russek, S.E. Semi-Empirical Equations for Electron Velocity in Silicon: Part II—MOS Inversion Layer. *IEEE Trans. Electron. Dev.* **1983**, *30*, 1634–1639. [CrossRef]
33. Schrieffer, J.R. Effective Carrier Mobility in Surface-Space Charge Layers. *Phys. Rev.* **1955**, *97*, 641–646. [CrossRef]