nanomaterials

MDPI

Article

Sensitivity of Inner Spacer Thickness Variations for Sub-3-nm Node Silicon Nanosheet Field-Effect Transistors

Sanguk Lee, Jinsu Jeong, Jun-Sik Yoon, Seunghwan Lee, Junjong Lee, Jaewan Lim and Rock-Hyun Baek *

Department of Electrical Engineering, Pohang University of Science and Technology (POSTECH), Pohang 37673, Gyeongbuk, Korea
* Correspondence: rh.baek@postech.ac.kr; Tel.: +82-54-279-2220

Abstract: The inner spacer thickness (T_{IS}) variations in sub-3-nm, node 3-stacked, nanosheet field-effect transistors (NSFETs) were investigated using computer-aided design simulation technology. Inner spacer formation requires a high selectivity of SiGe to Si, which causes inevitable T_{IS} variation (ΔT_{IS}). The gate length (L_G) depends on the T_{IS}. Thus, the DC/AC performance is significantly affected by ΔT_{IS}. Because the effects of ΔT_{IS} on the performance depend on which inner spacer is varied, the sensitivities of the performance to the top, middle, and bottom (T, M, and B, respectively) ΔT_{IS} should be studied separately. In addition, the source/drain (S/D) recess process variation that forms the parasitic bottom transistor (tr_{pbt}) should be considered with ΔT_{IS} because the gate controllability over tr_{pbt} is significantly dependent on $\Delta T_{IS,B}$. If the S/D recess depth (T_{SD}) variation cannot be completely eliminated, reducing $\Delta T_{IS,B}$ is crucial for suppressing the effects of tr_{pbt}. It is noteworthy that reducing $\Delta T_{IS,B}$ is the most important factor when the T_{SD} variation occurs, whereas reducing $\Delta T_{IS,T}$ and $\Delta T_{IS,M}$ is crucial in the absence of T_{SD} variation to minimize the DC performance variation. As the T_{IS} increases, the gate capacitance (C_{gg}) decreases owing to the reduction in both parasitic and intrinsic capacitance, but the sensitivity of C_{gg} to each ΔT_{IS} is almost the same. Therefore, the difference in performance sensitivity related to AC response is also strongly affected by the DC characteristics. In particular, since T_{SD} of 5 nm increases the off-state current (I_{off}) sensitivity to $\Delta T_{IS,B}$ by a factor of 22.5 in NFETs, the $\Delta T_{IS,B}$ below 1 nm is essential for further scaling and yield enhancement.

Keywords: nanosheet FET; inner spacer; inner spacer thickness variation; performance sensitivity; source/drain recess depth; TCAD simulation

Citation: Lee, S.; Jeong, J.; Yoon, J.-S.; Lee, S.; Lee, J.; Lim, J.; Baek, R.-H. Sensitivity of Inner Spacer Thickness Variations for Sub-3-nm Node Silicon Nanosheet Field-Effect Transistors. *Nanomaterials* **2022**, *12*, 3349. https://doi.org/10.3390/nano12193349

Academic Editors: Yung-Hsien Wu and Albert Chin

Received: 31 August 2022
Accepted: 21 September 2022
Published: 26 September 2022

1. Introduction

Silicon fin-shaped field-effect transistors (FinFETs) have been continuously scaled down from 22-nm to 5-nm nodes using fins with high aspect ratios and design technology co-optimization [1–6]. However, increasing the fin aspect ratio is challenging owing to the process complexity, and FinFETs with narrow fins exhibit threshold-voltage variations and performance degradation induced by the quantum confinement effect [7–10]. By contrast, Silicon gate-all-around nanosheet field-effect transistors (NSFETs) have received considerable attention as promising devices that can replace FinFETs in sub-3-nm nodes, as they can overcome these limitations through stacked nanosheet (NS) channels [11]. Furthermore, NSFETs provide excellent electrostatics because the gate surrounds the NS channels and drives a larger current within the same footprint with a wider effective channel width than FinFETs [11,12].

The inner spacer is a distinctive structural feature of NSFETs that has not been employed in previous devices. Typically, selective etching of the SiGe sacrificial layers is performed to form the inner spacer. However, selective etching requires a high selectivity of SiGe to Si and lateral etching. Therefore, it can be vulnerable to process variations [13,14].

Furthermore, because the inner spacer determines the gate length (L_G), these variations result in NSFETs with unintended L_G changes and cause unoptimized leakage and DC/AC performance [11,15]. Therefore, precise control of the inner spacer thickness (T_{IS}) is crucial for performance optimization.

Previous studies related to the inner spacer have focused on the electrical properties of NSFETs, assuming the same shape and thickness from the top inner spacer to the bottom inner spacer [11,15]. However, in the actual process, the T_{IS} variation (ΔT_{IS}) may not occur uniformly [11,16]. In addition, for three-stacked NSFETs, the top and middle inner spacers adjoin two adjacent NS channels, while the bottom inner spacer adjoins only one NS channel and a punch-through stopper (PTS) region. Thus, the thickness variations of the top/middle/bottom (T/M/B) inner spacers have different effects on the device behavior; i.e., the T/M/B ΔT_{IS} ($\Delta T_{IS,T}/\Delta T_{IS,M}/\Delta T_{IS,B}$) have different effects on the performance. Therefore, the performance sensitivities must be studied separately. Additionally, the over-etched S/D recess is a crucial factor determining the effects of the parasitic bottom transistor (tr_{pbt}) on the DC performance [17]. The effects of tr_{pbt} on performance become more pronounced as L_G decreases, which is a potential threat for further scaling [17,18]. However, there have been no studies on the effects of the S/D recess depth (T_{SD}) along with T/M/B ΔT_{IS} on the device behavior. In this study, for the first time, we comprehensively analyzed the sensitivity of the DC/AC characteristics to each ΔT_{IS} considering the T_{SD}, and the off-state characteristics were analyzed in detail using fully calibrated computer-aided design (TCAD) simulation technology [19].

2. Device Structure and Simulation Methodology

The sub-3-nm node NSFETs investigated in this study were simulated using Sentaurus TCAD tools. The following physical models were considered in the TCAD simulation:

- The drift–diffusion model was considered using Poisson's equations and the continuity equations to determine the electrostatic potential and carrier transport.
- The density gradient model was considered for the quantum confinement effect in the drift-diffusion model [20,21].
- The Slotboom bandgap narrowing model was considered for doping-dependent bandgap narrowing in Si and SiGe [22,23].
- A low-field ballistic mobility model was considered for quasi-ballistic transport [24].
- Mobility degradation at the interfaces was considered for remote phonon scattering and remote Coulomb scattering [25].
- The inversion and accumulation layer mobility models were considered for Coulomb impurity, phonon scattering, and surface roughness scattering [26].
- A high-field saturation model was considered for carrier velocity saturation under a strong electric field [27].
- The deformation potential model was considered for the strain-induced density of states, effective mass of carriers, and energy-band shift [28].
- The Auger and Shockley–Read–Hall (SRH) recombination models were used.

Figure 1a shows schematics of the sub-3-nm node 3-stacked NSFETs. Among the T/M/B ΔT_{IS}, we varied only one of the T/M/B T_{IS}, with the others fixed at 5 nm, to investigate the effects of the T/M/B ΔT_{IS} on the DC/AC characteristics separately. Here, the thicknesses of the T/M/B inner spacers were defined as $T_{IS,T}$, $T_{IS,M}$, and $T_{IS,B}$, respectively. In addition, T_{SD} of 0 and 5 nm were used to consider the effects of T_{SD} on the performance along with those of ΔT_{IS} [14]. Therefore, a comprehensive analysis of ΔT_{IS} considering the T_{SD} effect was performed.

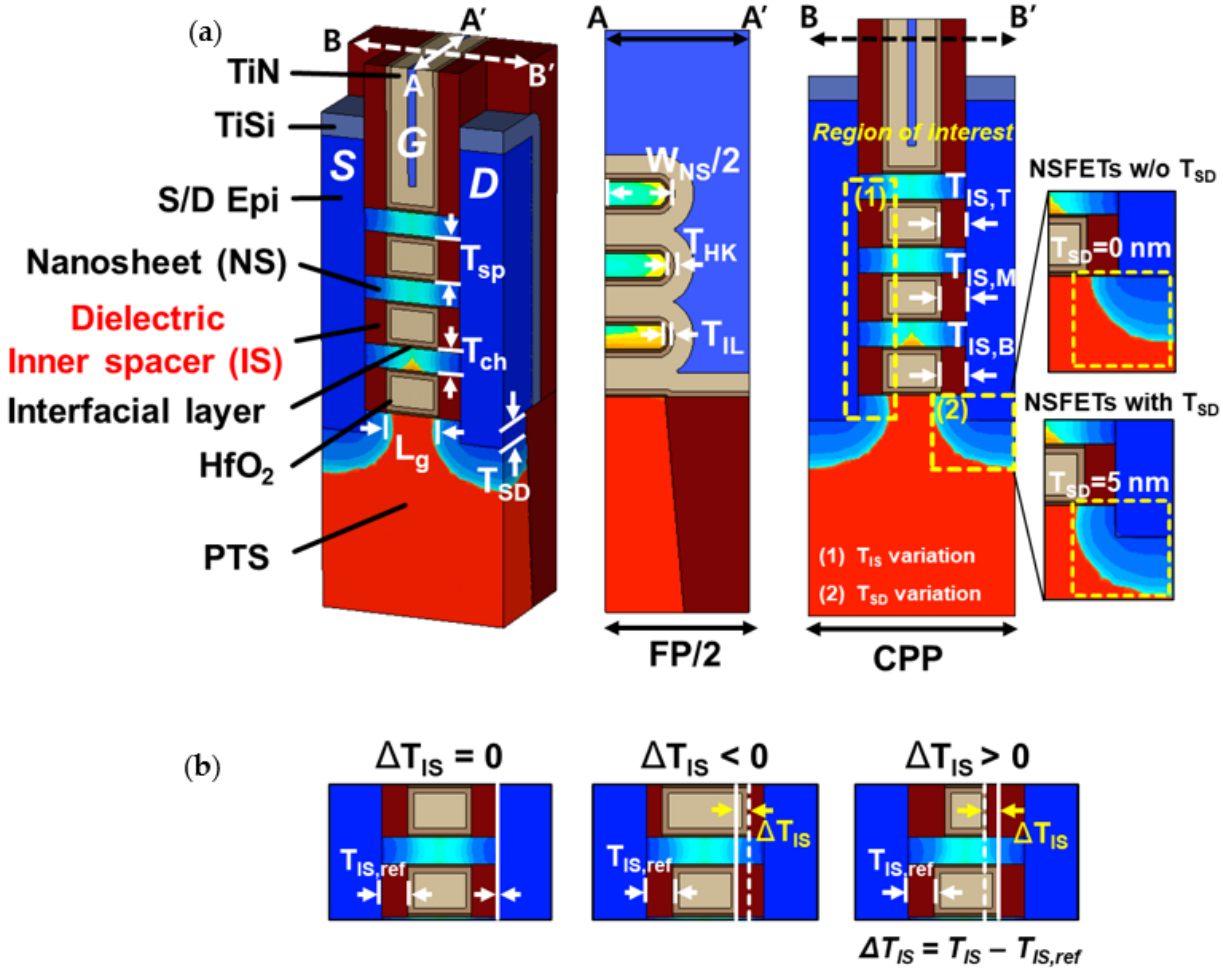

Figure 1. (**a**) Structure of NSFETs with the T_{SD} and cross-sectional views. (**b**) Schematics of ΔT_{IS} and its definition.

The T_{IS} without variation ($T_{IS,ref}$) was set as 5 nm, and only one of the three T_{IS} was varied from 3 to 7 nm (Figure 1b). In this study, ΔT_{IS} was defined as $T_{IS} - T_{IS,ref}$, and the L_G of each channel depended on ΔT_{IS} ($L_G = 22 - 2 \times (T_{IS,ref} + \Delta T_{IS})$). $Si_{0.98}C_{0.02}$ ($Si_{0.5}Ge_{0.5}$) S/D doped with phosphorus (boron) at 4×10^{20} cm^{-3} was used for the NFETs (PFETs). The contact resistance of the S/D was set as 1 $n\Omega \cdot cm^2$. The PTS layer was doped at 3×10^{18} cm^{-3}, and the drain voltage (V_{ds}) was fixed at $|0.7|$ V. The geometric parameters are presented in Table 1. The NSFETs were calibrated to TSMC's 5-nm node FinFETs [5], and the same physical parameters were used, as shown in our previous studies [29]. The drain current was fitted by adjusting the doping profile, ballistic coefficient, and saturation velocity. The doping profile was changed to fit the subthreshold swing and DIBL since the doping profile is deeply concerned with the device behaviors in the subthreshold region. The ballistic coefficient was tuned to fit the drain current in the linear region, and the saturation velocity was set to fit the drain current in the saturation region. We extracted the on-state current (I_{on}) and gate capacitance (C_{gg}) at $|V_{gs}| = 0.7$ V and $|V_{ds}| = 0.7$ V. Moreover, the off-state current (I_{off}) and parasitic capacitance (C_{para}) were extracted at $|V_{gs}| = 0$ V and $|V_{ds}| = 0.7$ V.

Table 1. Geometric parameters for sub-3-nm node NSFETs.

Fixed Parameters	Values
Contact poly pitch (CPP)	42 nm
Fin pitch (FP)	60 nm
Gate length (L_G)	12 nm
Spacing thickness (T_{SP})	10 nm
NS thickness (T_{CH})	5 nm
NS width (W_{NS})	25 nm
Interfacial layer thickness (T_{IL})	0.6 nm
HfO_2 thickness (T_{HK})	1.1 nm
T_{IS} without variation ($T_{IS,ref}$)	5 nm
S/D doping concentration (N_{SD})	4×10^{20} cm^{-3}
PTS doping concentration (N_{PTS})	3×10^{18} cm^{-3}
Variable parameters	**Values**
Excess S/D recess depth (T_{SD})	0 or 5 nm
Inner spacer thickness (T_{IS})	3–7 nm

3. Results and Discussion

Figure 2 shows the transfer curves of NSFETs with different $T_{IS,B}$ for T_{SD} = 0 and 5 nm. No significant dependence of the DC performance on $\Delta T_{IS,B}$ was observed at T_{SD} = 0 (Figure 2a). By contrast, at T_{SD} = 5 nm, the I_{off} increased significantly as $T_{IS,B}$ increased (Figure 2b). The T_{SD} typically impacts the I_{off} of tr_{pbt} [17], where $T_{IS,B}$ determines the L_G of tr_{pbt}. Because the L_G of tr_{pbt} affects the gate controllability over the PTS region, an increase in $\Delta T_{IS,B}$ significantly degrades the DC performance. As an increase in T_{SD} degrades the gate controllability of tr_{pbt}, $T_{IS,B}$ is a critical factor determining the parasitic punch-through current (I_{pt}) in the PTS region. Therefore, the subthreshold swing and DIBL are significantly degraded, as shown in the inset of Figure 2 and Table 2.

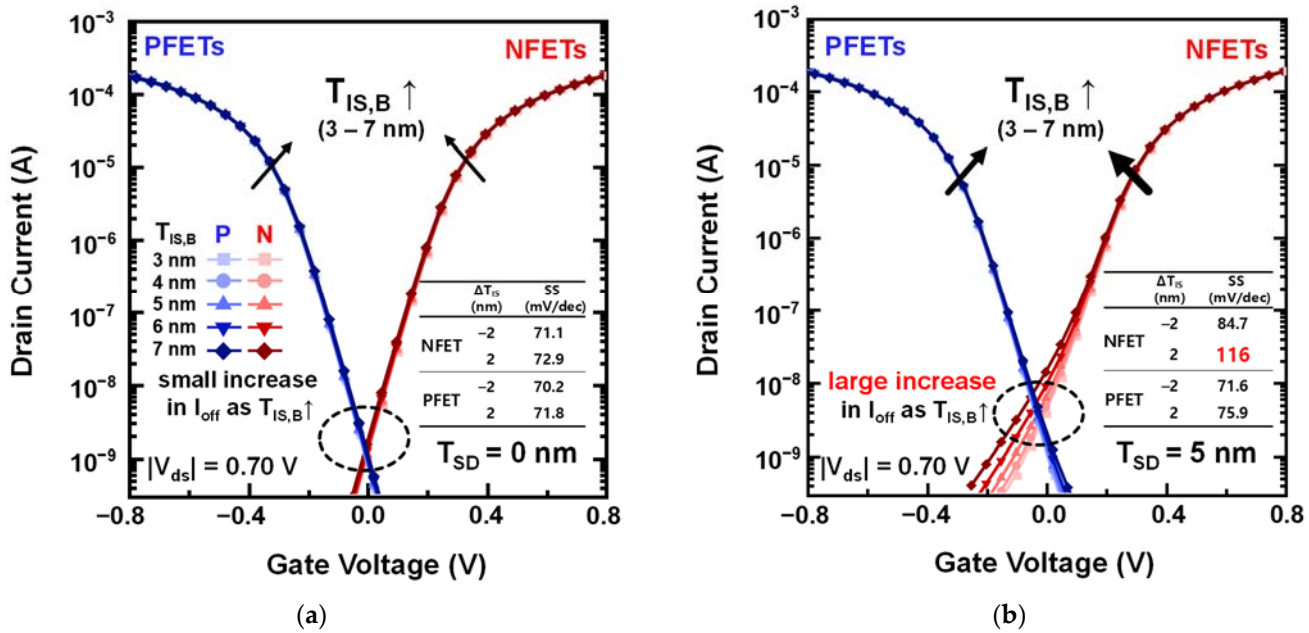

Figure 2. Transfer curves of the NSFETs having different $T_{IS,B}$ with (**a**) T_{SD} = 0 nm and (**b**) T_{SD} = 5 nm.

Table 2. DIBL of NSFETs according to the $T_{IS,B}$ and T_{SD}.

Type	$T_{IS,B}$ [nm]	DIBL [mV/V]	
		T_{SD} = 0 nm	T_{SD} = 5 nm
NFETs	3	60	67
	5	62	72
	7	67	81
PFETs	3	51	54
	5	53	57
	7	58	61

The I_{off} sensitivities to the T/M/B ΔT_{IS} ($S_{Ioff,T}/S_{Ioff,M}/S_{Ioff,B}$) are compared in Figure 3. We defined S_{Ioff} as the slope of $I_{off}-\Delta T_{IS}$, which indicates how sensitively I_{off} varies with respect to ΔT_{IS}. For the NFETs with T_{SD} = 0 nm, the $S_{Ioff,T}$ (0.208) and $S_{Ioff,M}$ (0.228) slightly exceeded the $S_{Ioff,B}$ (0.104 nA/nm), and similar S_{Ioff} tendencies were observed for the PFETs. The T_{SD} variation not only increased I_{off}, but also significantly increased $S_{Ioff,B}$ for both the NFETs and the PFETs. The $S_{Ioff,B}$ for the NFETs is greater than that for the PFETs, which is mainly attributed to the S/D dopant diffusion into the PTS region. Phosphorus has a higher diffusivity than boron; therefore, more S/D dopant diffuses into the PTS region in NFETs than in PFETs [30]. Consequently, the NFETs are more sensitive to the $\Delta T_{IS,B}$ in terms of I_{off}. For the NFETs with T_{SD} = 5 nm, $S_{Ioff,T}$, $S_{Ioff,M}$, and $S_{Ioff,B}$ were 0.195, 0.209, and 2.34 nA/nm, respectively. $S_{Ioff,T}$ and $S_{Ioff,M}$ were almost identical regardless of the T_{SD}, but $S_{Ioff,B}$ increased by a factor of 22.5 when the T_{SD} increased from 0 to 5 nm. This indicated that the S/D recess process variation slightly affects $S_{Ioff,T}$ and $S_{Ioff,M}$ but significantly affects $S_{Ioff,B}$. Thus, if the T_{SD} variation is not perfectly eliminated, $\Delta T_{IS,B}$ should be controlled below 1 nm, because devices with greater than 10 times in I_{off} are not suitable for the intended system-on-chip applications.

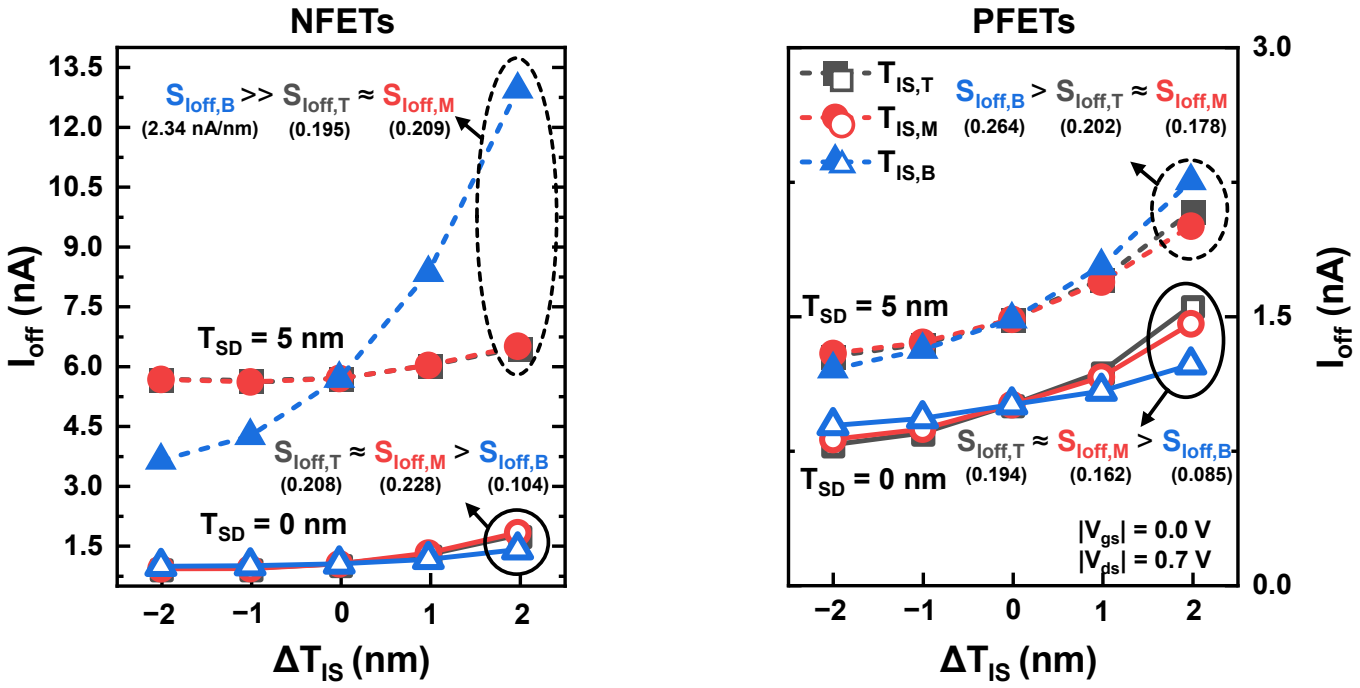

Figure 3. I_{off} of NSFETs according to ΔT_{IS} with T_{SD} = 0 and 5 nm.

The differences in the S_{Ioff} shown in Figure 3 can be explained using the I_{off}-density profiles (Figure 4). In NSFETs with T_{SD} = 0 nm, most carriers existed in the NS channels, and a few were in the PTS region owing to the heavily doped PTS. Furthermore, ΔT_{IS}-induced I_{off} density variations mainly arose in the NS channels next to the inner spacer

with variations in the thickness. Thus, the top and middle inner spacers adjacent to the NS channels with high carrier concentrations exhibited larger changes in the I_{off} density than the bottom inner spacer. Therefore, $S_{Ioff,T}$ and $S_{Ioff,M}$ are higher than $S_{Ioff,B}$ for the NSFETs with T_{SD} = 0 nm. By contrast, $S_{Ioff,B}$ was the highest when the T_{SD} was 5 nm. Figure 4b shows the I_{off} density profiles for NFETs with different $T_{IS,B}$ in the case of T_{SD} = 5 nm. As $T_{IS,B}$ increased, the off-state I_{pt} ($I_{pt,off}$) was not suppressed, resulting in a significant increase in I_{off}, as shown in Figure 2. The I_{off} density varied according to $\Delta T_{IS,B}$ in the bottom NS and PTS regions but varied to a significantly larger extent in the PTS region. Specifically, the T_{SD} variation significantly enhanced the effects of tr_{pbt} on I_{off}, and the change in $I_{pt,off}$ was a dominant factor in the $S_{Ioff,B}$ increment. This is because the PTS region was only controlled by the bottom gate. Therefore, the bottom gate could not effectively control the PTS region far from the bottom gate. As a result, worse short-channel effects (SCEs) were observed in the PTS region than in the NS channel.

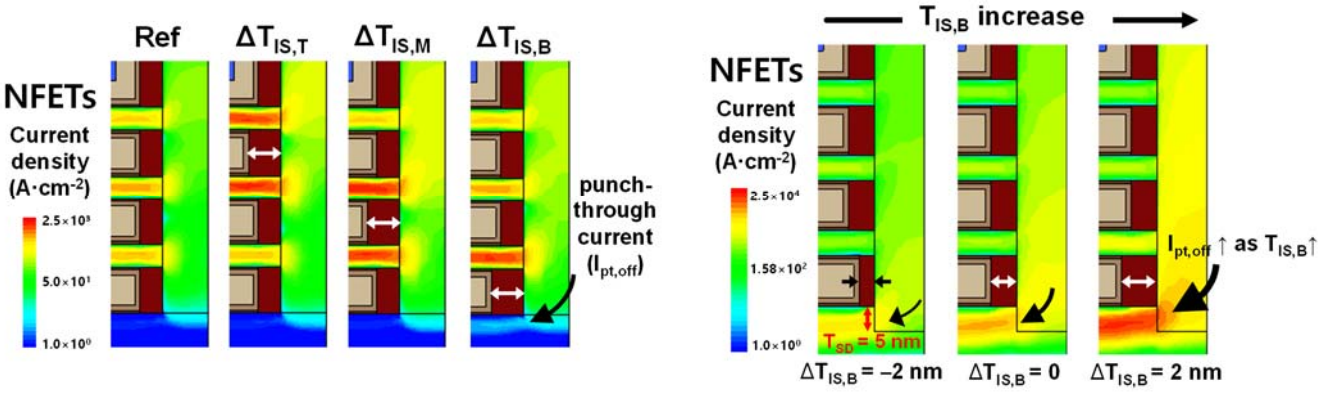

Figure 4. (**a**) I_{off} density profiles of the NFETs with T_{SD} = 0 and each ΔT_{IS} equal to 2 nm. (**b**) I_{off} density profiles of the NFETs with T_{SD} = 5 nm for different values of $\Delta T_{IS,B}$.

Figure 5a shows the conduction band energy (E_c) diagrams of the source–PTS–drain in the NFETs, which were extracted under the off-state bias condition. As the T_{SD} increased from 0 to 5 nm, the significant reduction in the energy barrier height (Φ_b) from 478 to 402 mV was caused by the larger amount of S/D dopant diffusion into the PTS region at a T_{SD} of 5 nm. In NFETs with T_{SD} = 0 nm, the Φ_b of the PTS region was sufficiently high to control $I_{pt,off}$ regardless of $\Delta T_{IS,B}$ (Figure 5b). Therefore, I_{off} can be effectively controlled even with $\Delta T_{IS,B}$. However, if Φ_b is not sufficiently high, the additional Φ_b reduction due to $\Delta T_{IS,B}$ can be a critical factor in inducing $I_{pt,off}$. An additional Φ_b reduction was observed when $T_{IS,B}$ increased, and the change in Φ_b by $\Delta T_{IS,B}$ significantly contributed to the $I_{pt,off}$ variation (Figures 3 and 5c). Therefore, the bottom L_G of tr_{pbt}, which is related to $T_{IS,B}$, is important for suppressing SCEs in the PTS region. According to these results, $S_{Ioff,B}$ is significantly affected by T_{SD}. Thus, minimizing $\Delta T_{IS,B}$ is more crucial when an over-etched S/D recess occurs.

Figure 6 shows the relationship between the on-state current (I_{on}) and ΔT_{IS}, and the slope indicates the I_{on} sensitivity (S_{Ion}). For the NFETs, the $S_{Ion,T}$ and $S_{Ion,M}$ are slightly higher than the $S_{Ion,B}$ regardless of the T_{SD}. By contrast, for the PFETs, the $S_{Ion,B}$ varied significantly with respect to the T_{SD}, leading to an increase in $S_{Ion,B}$ by a factor of 1.9. Thus, an increase in $\Delta T_{IS,B}$ can cause severe I_{on} variations when the T_{SD} is not precisely controlled. The reason for the differences in the S_{Ion} is explained in Figure 7.

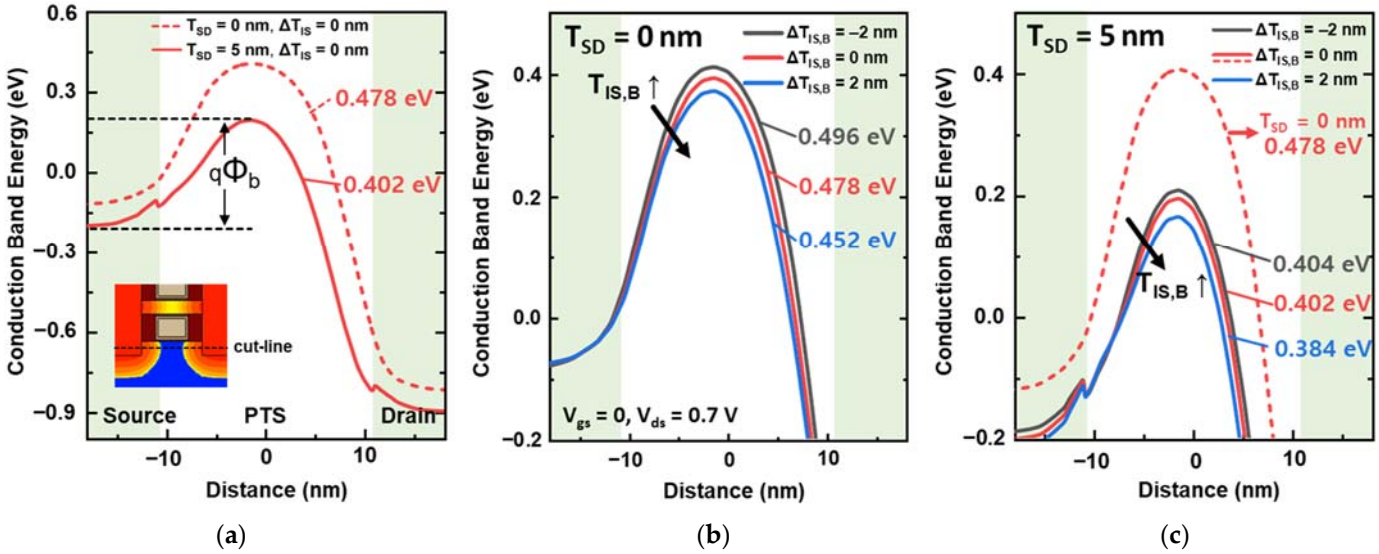

Figure 5. (**a**) Energy band diagram of the source–PTS–drain in NFETs with T_{SD} = 5 nm (solid line) and T_{SD} = 0 nm (dashed line). The E_c of the PTS region with different $T_{IS,B}$ at (**b**) T_{SD} = 0 and (**c**) T_{SD} = 5 nm.

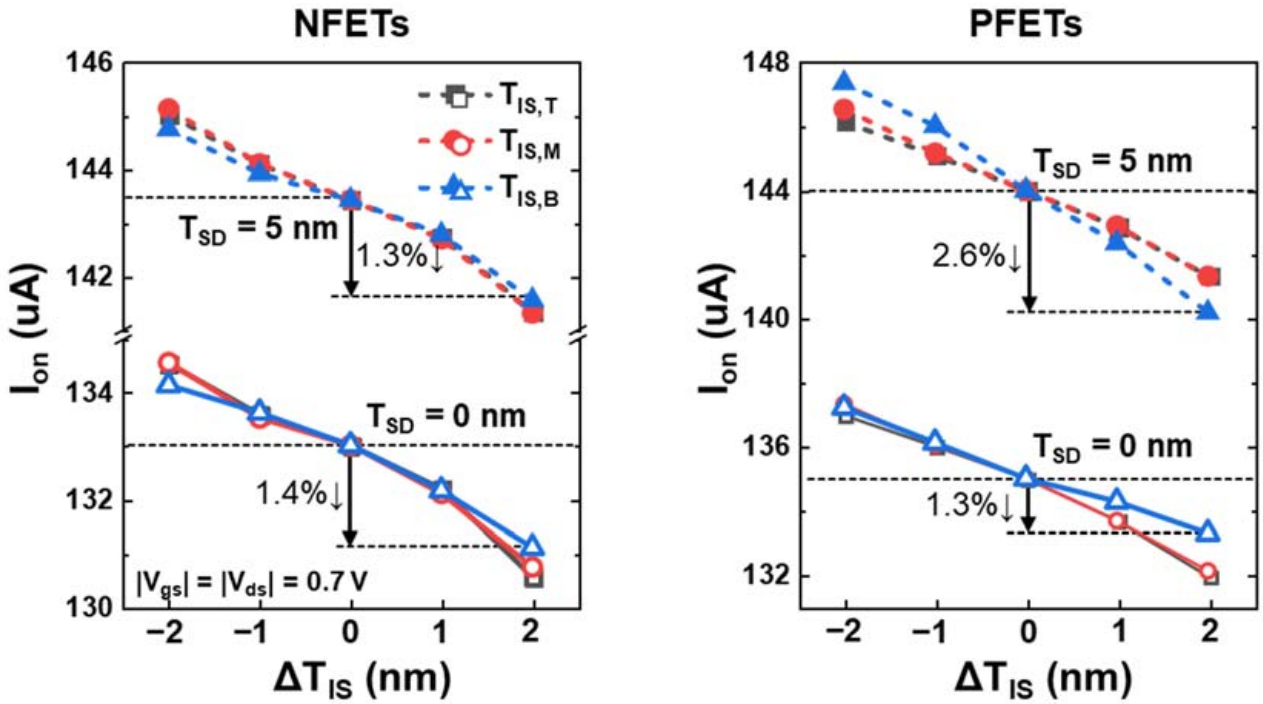

Figure 6. I_{on} of NSFETs having different ΔT_{IS} with T_{SD} = 5 nm (solid symbols) and T_{SD} = 0 nm (open symbols).

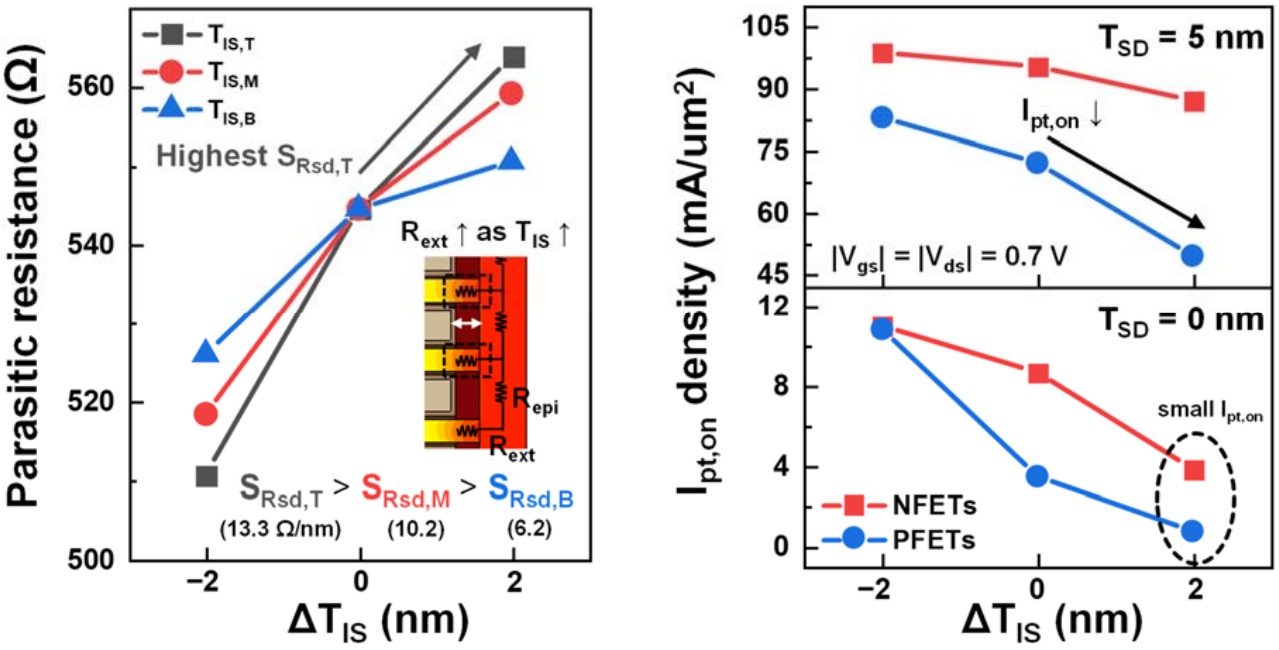

Figure 7. (**a**) Parasitic resistance (R_{sd}) of NFETs with respect to the ΔT_{IS}. (**b**) $I_{pt,on}$ density of NSFETs with respect to the $\Delta T_{IS,B}$.

The R_{sd} sensitivity (S_{Rsd}) and on-state I_{pt} ($I_{pt,on}$)-density variations to the ΔT_{IS} account for the differences in T/M/B S_{Ion} (Figure 7). R_{sd} was extracted using Y-function techniques, as described in [31]. Two main factors determine S_{Ion}: R_{sd} and inversion charges in the PTS region. Additionally, the major factors affecting S_{Ion} depend on the T_{SD}. For both the NFETs and PFETs with T_{SD} = 0 nm, S_{Ion} was mainly affected by the change in R_{sd}, which consisted of the series S/D epi resistance (R_{epi}) and extension resistance (R_{ext}). R_{epi} did not change with respect to ΔT_{IS}, but R_{ext} did. Because S_{Rsd} varied proportionally to the number of NS channels adjacent to the inner spacer where ΔT_{IS} occurred (Figure 7a), $S_{Ion,T}$ and $S_{Ion,M}$ were greater than $S_{Ion,B}$. However, the inversion charges in the PTS region significantly affected S_{Ion} when T_{SD} was 5 nm. As the deep T_{SD} caused a substantial current to flow through tr_{pbt}, the I_{on} contribution of the PTS region was no longer small. The inversion charges in the PTS region should also be considered (Figure 7b). For the NFETs, the $I_{pt,on}$ density in tr_{pbt} decreased slightly as $T_{IS,B}$ increased, whereas the large decrease in $I_{pt,on}$ was observed for the PFETs. This is because higher SCEs and V_{th} reductions were observed in the NFETs, as the large amounts of diffused S/D dopants reduced Φ_b (Figures 2b and 5a). Therefore, in the NFETs, the V_{th} reduction of tr_{pbt} lowered the effects of the increase in R_{sd}, which was the dominant factor determining $S_{Ion,B}$. By contrast, in the PFETs, the V_{th} reduction of tr_{pbt} was small; thus, $I_{pt,on}$ decreased significantly owing to the increase in the R_{sd} of tr_{pbt}. Consequently, $S_{Ion,B}$ was the smallest for the NFETs, but for the PFETs, the T_{SD} variation caused I_{on} to be most sensitive to $\Delta T_{IS,B}$.

Based on these results, we can provide two guidelines for controlling the DC performance variation, which depends on T_{SD}. In the case of T_{SD} = 0, precisely controlling $T_{IS,T}$ and $T_{IS,M}$ rather than $T_{IS,B}$ is effective for minimizing the variations in I_{off} and I_{on}, as shown in Figures 3 and 6. However, considering the T_{SD} variation, it is necessary to focus on the bottom inner spacer, because a precisely controlled $T_{IS,B}$, can considerably reduce the performance variation. Otherwise, the effects of tr_{pbt} on the DC performance become large as $T_{IS,B}$ increases, resulting in the worst case with the highest I_{off} and lowest I_{on} in PFETs, which significantly diminishes the performance advantages of NSFETs.

The gate capacitance (C_{gg}) with respect to ΔT_{IS} for NSFETs (T_{SD} = 0) is shown in Figure 8, and C_{gg} is decomposed into the intrinsic capacitance (C_{int}) and parasitic capac-

itance (C_{para}). C_{para} was extracted under the off-state bias, and C_{int} was calculated by subtracting C_{para} from C_{gg} under the on-state bias. As shown in Figure 8a, the differences in the C_{gg} sensitivity to T/M/B ΔT_{IS} (S_{Cgg}) were small. However, the changes in C_{int} and C_{para} for each ΔT_{IS} did not have the same sensitivity. C_{para}, which was determined by the fringing field between the gate and S/D, was affected by the T_{IS}. Therefore, the sensitivity of C_{para} to ΔT_{IS} was almost identical among the T/M/B ΔT_{IS} (Figure 8b). However, the sensitivity of C_{int} to $\Delta T_{IS,B}$ was lower than those of $\Delta T_{IS,T}$ and $\Delta T_{IS,M}$ (Figure 8c). Although the inversion charge variations caused by $\Delta T_{IS,B}$ mainly occurred in the bottom NS and PTS regions, the charge variations in the PTS region were smaller than those in the NS channels, leading to different AC sensitivities to the T/M/B ΔT_{IS}. However, because the differences in the C_{int} sensitivity to the T/M/B ΔT_{IS} were not large, it can be concluded that the overall performance sensitivity difference induced by each ΔT_{IS} has greater effects on DC (I_{off}, I_{on}) rather than the AC performance.

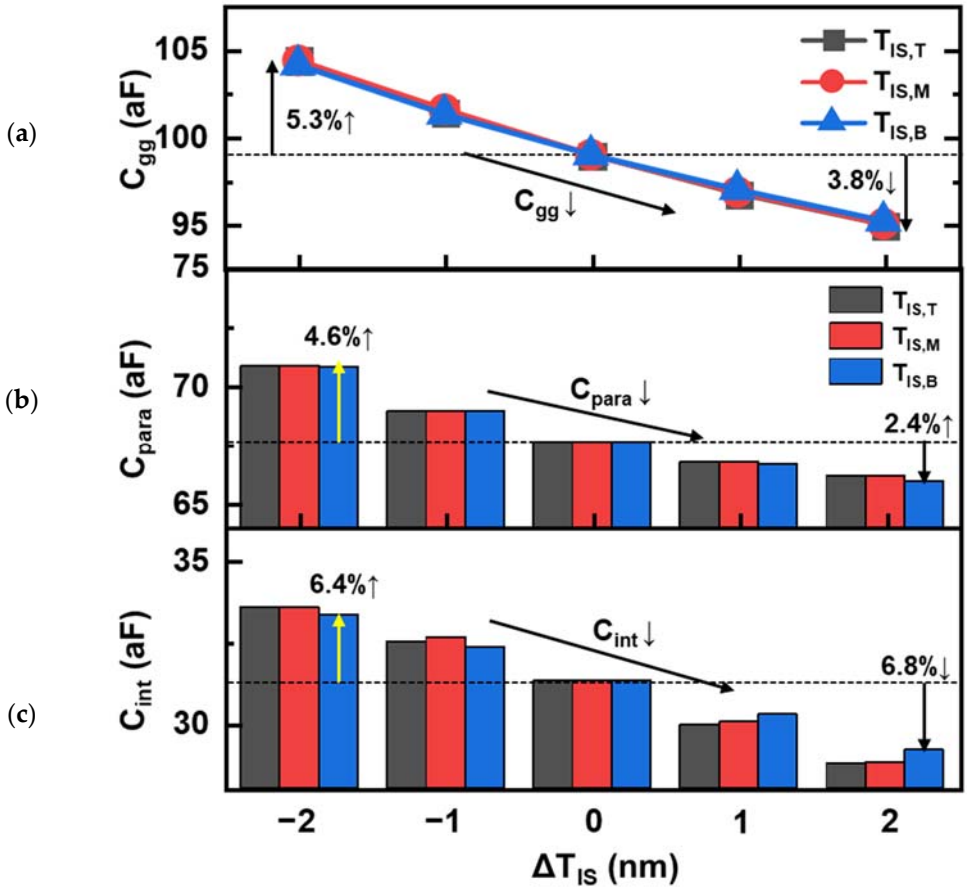

Figure 8. (**a**) C_{gg}, (**b**) C_{para}, and (**c**) C_{int} for NFETs with respect to ΔT_{IS} (T_{SD} = 0). The capacitances were extracted at a frequency of 1 MHz.

4. Conclusions

The sensitivities of the DC/AC performance to the T/M/B ΔT_{IS} in sub-3-nm node NSFETs were quantitatively investigated using a fully calibrated TCAD simulation. The DC performance sensitivities (I_{off}, I_{on}) to the T/M/B ΔT_{IS} differed. However, there were no significant differences in the AC sensitivities. One of the notable results was that ΔT_{IS}, which varied the performance the most, was different according to the T_{SD} variations. In NSFETs with T_{SD} = 0 nm, $S_{Ioff,B}$ was lower than $S_{Ioff,T}$ and $S_{Ioff,M}$ because the effects of $\Delta T_{IS,B}$ were primarily observed in the bottom NS channel. However, tr_{pbt} was no longer negligible when the T_{SD} was 5 nm. Thus, if the T_{SD} variation is not controlled, NFETs (PFETs) have higher $S_{Ioff,B}$ ($S_{Ion,B}$) because of the effects of tr_{pbt}. It can be concluded that

the bottom inner spacer is the element with the most significant effect on the DC/AC performance. Hence, reducing $\Delta T_{IS,B}$ is important for yield enhancement.

Author Contributions: Conceptualization, S.L. (Sanguk Lee); methodology, S.L. (Sanguk Lee), J.-S.Y. and J.J.; formal analysis, S.L. (Sanguk Lee); investigation, S.L. (Sanguk Lee), J.J., S.L. (Seunghwan Lee) and J.L. (Junjoung Lee); writing—original draft preparation, S.L. (Sanguk Lee); writing—review and editing, J.-S.Y., J.J., S.L. (Seunghwan Lee), J.L. (Junjoung Lee) and J.L. (Jaewan Lim); supervision, J.J. and R.-H.B.; project administration, R.-H.B.; funding acquisition, R.-H.B. All authors have read and agreed to the published version of the manuscript.

Funding: This work was supported in part by POSTECH-Samsung Electronics Industry-Academia Cooperative Research Center; National Research Foundation of Korea (NRF) grant funded by the Korea Government (MSIT) (No. NRF-2022R1C1C1004925, NRF-2020M3F3A2A02082436, NRF-2020R1A4A4079777); MOTIE (Ministry of Trade, Industry & Energy) (No. 20019450, 20020265) and KSRC (Korea Semiconductor Research Consortium) support program for the development of the future semiconductor device and BK21 FOUR Program.

Data Availability Statement: Not applicable.

Acknowledgments: The EDA tool was supported by the IC Design Education Center, Korea.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Auth, C.; Allen, C.; Blattner, A.; Bergstrom, D.; Brazier, M.; Bost, M.; Buehler, M.; Chikarmane, V.; Ghani, T.; Glassman, T.; et al. A 22nm High Performance and Low-Power CMOS Technology Featuring Fully-Depleted Tri-Gate Transistors, Self-Aligned Contacts and High Density MIM Capacitors. In *Digest of Technical Papers, Proceedings of the Symposium on VLSI Technology (Symposium on VLSI Technology), Honolulu, HI, USA, 12–14 June 2012*; IEEE: Piscataway, NJ, USA, 2012; Volume 980, pp. 131–132. [CrossRef]
2. Natarajan, S.; Agostinelli, M.; Akbar, S.; Bost, M.; Bowonder, A.; Chikarmane, V.; Chouksey, S.; Dasgupta, A.; Fischer, K.; Fu, Q.; et al. A 14nm Logic Technology Featuring 2nd-Generation FinFET, Air-Gapped Interconnects, Self-Aligned Double Patterning and a 0.0588 Mm2 SRAM Cell Size. In Proceedings of the 2014 IEEE International Electron Devices Meeting, San Francisco, CA, USA, 15–17 December 2014; pp. 3.7.1–3.7.3. [CrossRef]
3. Auth, C.; Aliyarukunju, A.; Asoro, M.; Bergstrom, D.; Bhagwat, V.; Birdsall, J.; Bisnik, N.; Buehler, M.; Chikarmane, V.; Ding, G.; et al. A 10nm High Performance and Low-Power CMOS Technology Featuring 3rd Generation FinFET Transistors, Self-Aligned Quad Patterning, Contact over Active Gate and Cobalt Local Interconnects. In Proceedings of the International Electron Devices Meeting, IEDM, San Francisco, CA, USA, 2–6 December 2017; pp. 29.1.1–29.1.4.
4. Xie, R.; Montanini, P.; Akarvardar, K.; Tripathi, N.; Haran, B.; Johnson, S.; Hook, T.; Hamieh, B.; Corliss, D.; Wang, J.; et al. A 7nm FinFET Technology Featuring EUV Patterning and Dual Strained High Mobility Channels. In Proceedings of the 2016 IEEE international electron devices meeting (IEDM), San Francisco, CA, USA, 3–7 December 2016; Volume 12, pp. 2.7.1–2.7.4. [CrossRef]
5. Yeap, G.; Chen, X.; Yang, B.R.; Lin, C.P.; Yang, F.C.; Leung, Y.K.; Lin, D.W.; Chen, C.P.; Yu, K.F.; Chen, D.H.; et al. 5nm CMOS Production Technology Platform Featuring Full-Fledged EUV, and High Mobility Channel FinFETs with Densest 0.021μm2 SRAM Cells for Mobile SoC and High Performance Computing Applications. In Proceedings of the 2019 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 7–11 December 2019; pp. 879–882. [CrossRef]
6. Kye, J.; Kim, H.; Lim, J.; Lee, S.; Jung, J.; Song, T. Smart Scaling Technology for Advanced FinFET Node. In Proceedings of the 2018 IEEE Symposium on VLSI Technology, Honolulu, HI, USA, 18–22 June 2018; pp. 149–150. [CrossRef]
7. Bae, G.; Bae, D.I.; Kang, M.; Hwang, S.M.; Kim, S.S.; Seo, B.; Kwon, T.Y.; Lee, T.J.; Moon, C.; Choi, Y.M.; et al. 3nm GAA Technology Featuring Multi-Bridge-Channel FET for Low Power and High Performance Applications. In Proceedings of the 2018 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 1–5 December 2018; pp. 28.7.1–28.7.4. [CrossRef]
8. Chang, J.B.; Guillorn, M.; Solomon, P.M.; Lin, C.H.; Engelmann, S.U.; Pyzyna, A.; Ott, J.A.; Haensch, W.E. Scaling of SOI FinFETs down to Fin Width of 4 nm for the 10nm Technology Node. In Proceedings of the 2011 Symposium on VLSI Technology, Kyoto, Japan, 14–16 June 2011; pp. 12–13.
9. He, X.; Fronheiser, J.; Zhao, P.; Hu, Z.; Uppal, S.; Wu, X.; Hu, Y.; Sporer, R.; Qin, L.; Krishnan, R.; et al. Impact of Aggressive Fin Width Scaling on FinFET Device Characteristics. In Proceedings of the 2017 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 2–6 December 2017; pp. 20.2.1–20.2.4. [CrossRef]
10. Razavieh, A.; Zeitzoff, P.; Nowak, E.J. Challenges and Limitations of CMOS Scaling for FinFET and beyond Architectures. *IEEE Trans. Nanotechnol.* **2019**, *18*, 999–1004. [CrossRef]
11. Loubet, N.; Hook, T.; Montanini, P.; Yeung, C.W.; Kanakasabapathy, S.; Guillom, M.; Yamashita, T.; Zhang, J.; Miao, X.; Wang, J.; et al. Stacked Nanosheet Gate-All-around Transistor to Enable Scaling beyond FinFET. In Proceedings of the 2017 Symposium on VLSI Technology, Kyoto, Japan, 5–8 June 2017; pp. T230–T231. [CrossRef]

12. Barraud, S.; Lapras, V.; Previtali, B.; Samson, M.P.; Lacord, J.; Martinie, S.; Jaud, M.; Athanasiou, S.; Triozon, F. Performance and Design Considerations for gate-all-around stacked-NanoWires FETs. In Proceedings of the 2017 IEEE international electron devices meeting (IEDM), San Francisco, CA, USA, 2–6 December 2017; pp. 1–4.
13. Barraud, S.; Lapras, V.; Samson, M.P.; Gaben, L.; Grenouillet, L.; Maffini-Alvaro, V.; Morand, Y.; Daranlot, J.; Rambal, N.; Previtalli, B.; et al. Vertically Stacked-NanoWires MOSFETs in a Replacement Metal Gate Process with Inner Spacer and SiGe Source/Drain. In Proceedings of the 2016 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 3–7 December 2016; pp. 17.6.1–17.6.4. [CrossRef]
14. Loubet, N.; Devarajan, T.; Zhang, J.; Miao, X.; Sankar, M.; Breton, M.; Chao, R.; Greene, A.; Yu, L.; Frougier, J.; et al. A Novel Dry Selective Etch of SiGe for the Enablement of High Performance Logic Stacked Gate-All-Around NanoSheet Devices. In Proceedings of the 2019 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 7–11 December 2019. [CrossRef]
15. Yoon, J.S.; Jeong, J.; Lee, S.; Baek, R.H. Punch-Through-Stopper Free Nanosheet FETs with Crescent Inner-Spacer and Isolated Source/Drain. *IEEE Access* **2019**, *7*, 38593–38596. [CrossRef]
16. Schmidt, D.; Cepler, A.; Durfee, C.; Pancharatnam, S.; Frougier, J.; Breton, M.; Greene, A.; Klare, M.; Koret, R.; Turovets, I. Development of SiGe Indentation Process Control for Gate-All-Around FET Technology Enablement. *IEEE Trans. Semicond. Manuf.* **2022**, *6507*, 412–417. [CrossRef]
17. Jeong, J.; Yoon, J.S.; Lee, S.; Baek, R.H. Comprehensive Analysis of Source and Drain Recess Depth Variations on Silicon Nanosheet FETs for Sub 5-Nm Node SoC Application. *IEEE Access* **2020**, *8*, 35873–35881. [CrossRef]
18. Zhang, J.; Pancharatnam, S.; Adams, C.; Wu, H.; Zhou, H.; Shen, T.; Xie, R.; Sankarapandian, M.; Wang, J.; Watanabe, K.; et al. Full Bottom Dielectric Isolation to Enable Stacked Nanosheet Transistor for Low Power and High Performance Applications. In Proceedings of the 2019 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 7–11 December. [CrossRef]
19. Synopsys Inc. *Version O-2019.12-SP1*; Synopsys Inc.: Mountain View, CA, USA, 2019.
20. Ancona, M.G.; Tiersten, H.F. Macroscopic Physics of the Silicon Inversion Layer. *Phys. Rev. B* **1987**, *35*, 7959–7965. [CrossRef] [PubMed]
21. Ancona, M.G.; Iafrate, G.J. Quantum Correction to the Equation of State of an Electron Gas in a Semiconductor. *Phys. Rev. B* **1989**, *39*, 9536–9540. [CrossRef]
22. Slotboom, J.W.; de Graaff, H.C. Measurements of Bandgap Narrowing in Si Bipolar Transistors. *Solid State Electron.* **1976**, *19*, 857–862. [CrossRef]
23. Klaassen, D.B.M.; Slotboom, J.W.; de Graaff, H.C. Unified Apparent Bandgap Narrowing in N- and p-Type Silicon. *Solid. State. Electron.* **1992**, *35*, 125–129. [CrossRef]
24. Shur, M.S. Low Ballistic Mobility in Submicron HEMTs. *IEEE Electron Device Lett.* **2002**, *23*, 511–513. [CrossRef]
25. Ando, T. Ultimate Scaling of High-κ Gate Dielectrics: Higher-κ or Interfacial Layer Scavenging? *Materials* **2012**, *5*, 478–500. [CrossRef]
26. Mujtaba, S.A. Advanced Mobility Models for Design and Simulation of Deep Submicron MOSFETs. Ph.D. Dissertation, Department of Electrical Engineering Stanford University, Stanford, CA, USA, 1996.
27. Canali, C.; Majni, G.; Minder, R.; Ottaviani, G. Electron and Hole Drift Velocity Measurements in Silicon and Their Empirical Relation to Electric Field and Temperatures. *IEEE Trans. Electron Devices* **1976**, *23*, 1113. [CrossRef]
28. Bardeen, J.; Shockley, W. Deformation Potentials and Mobilities in Non-Polar Crystals. *Phys. Rev.* **1950**, *80*, 72–80. [CrossRef]
29. Yoon, J.S.; Jeong, J.; Lee, S.; Lee, J.; Lee, S.; Baek, R.H.; Lim, S.K. Performance, Power, and Area of Standard Cells in Sub 3 nm Node Using Buried Power Rail. *IEEE Trans. Electron Devices* **2022**, *69*, 894–899. [CrossRef]
30. Zangenberg, N.R.; Fage-Pedersen, J.; Hansen, J.L.; Larsen, A.N. Boron and Phosphorus Diffusion in Strained and Relaxed Si and SiGe. *J. Appl. Phys.* **2003**, *94*, 3883–3890. [CrossRef]
31. Baek, R.H.; Baek, C.K.; Jung, S.W.; Yeoh, Y.Y.; Kim, D.W.; Lee, J.S.; Kim, D.M.; Jeong, Y.H. Characteristics of the Series Resistance Extracted from Si Nanowire FETs Using the Y-Function Technique. *IEEE Trans. Nanotechnol.* **2010**, *9*, 212–217. [CrossRef]