



Article High-Performance On-Chip Silicon Beamsplitter Based on Subwavelength Metamaterials for Enhanced Fabrication Tolerance

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Abstract: Efficient power splitting is a fundamental functionality in silicon photonic integrated circuits, but state-of-the-art power-division architectures are hampered by limited operational bandwidth, high sensitivity to fabrication errors or large footprints. In particular, traditional Y-junction power splitters suffer from fundamental mode losses due to limited fabrication resolution near the junction tip. In order to circumvent this limitation, we propose a new type of high-performance Y-junction power splitter that incorporates subwavelength metamaterials. Full three-dimensional simulations show a fundamental mode excess loss below 0.1 dB in an ultra-broad bandwidth of 300 nm (1400–1700 nm) when optimized for a fabrication resolution of 50 nm, and under 0.3 dB in a 350 nm extended bandwidth (1350–1700 nm) for a 100 nm resolution. Moreover, analysis of fabrication tolerances shows robust operation for the fundamental mode to etching errors up to ± 20 nm. A proof-of-concept device provides an initial validation of its operation principle, showing experimental excess losses lower than 0.2 dB in a 195 nm bandwidth for the best-case resolution scenario (i.e., 50 nm).

Keywords: photonic integrated circuits; silicon photonics; power division; beamsplitter; Y-junction; subwavelength metamaterial; ultra-broadband; fabrication-tolerant

1. Introduction

The silicon-on-insulator (SOI) integrated photonic platform has been successfully exploited in a wide variety of fields, from telecom and datacom systems [1,2] to biochemical sensors [3], LIDAR systems [4], microspectrometers [5–7] and supercontinuum generation [8], among many others. The expansion into these diverse application fields has been made possible by the inherent benefits of the SOI platform, including large capacity of integration due to high refractive-index contrast [9] and low-cost mass production provided by the compatibility with complementary metal oxide semiconductor (CMOS) fabrication processes [10]. Conversely, the strong modal confinement results in SOI devices with high sensitivity to geometrical deviations from nominal design. This constraint is also present in power splitting components, a fundamental functionality in most silicon photonic integrated circuits [11] and, specifically, in an extensive range of applications including wavelength- and mode-division multiplexing [12], optical phased arrays [13] and on-chip spectrometers [6].

State-of-the-art power division structures such as directional couplers, multimode interference (MMI) devices or power splitters based on slot and adiabatic waveguides entail shortcomings in terms of reduced operational bandwidth, high sensitivity to fabrication deviations or large footprints [14–21]. Directional couplers [14], despite a significant improvement in their manufacturing tolerances through geometrical optimization [15] and phase control sections [16], still present comparatively limited operational bandwidth.



Citation: Fernández de Cabo, R.; González-Andrade, D.; Cheben, P.; Velasco, A.V. High-Performance On-Chip Silicon Beamsplitter Based on Subwavelength Metamaterials for Enhanced Fabrication Tolerance. *Nanomaterials* **2021**, *11*, 1304. https:// doi.org/10.3390/nano11051304

Academic Editor: Werner Blau

Received: 19 April 2021 Accepted: 13 May 2021 Published: 14 May 2021

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Copyright: © 2021 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (https:// creativecommons.org/licenses/by/ 4.0/). While bent directional couplers [17] have achieved a broadband response, they are affected by a strong sensitivity to manufacturing deviations. Slot waveguides [18] and adiabatic couplers [19] have demonstrated good performance over a wide bandwidth; however, these devices have considerably larger footprints. Similarly, MMI couplers offer numerous advantages, such as relatively small size and relaxed manufacturing tolerances [20], but their bandwidth is limited by the strong modal dispersion in multimode SOI waveguides. Different structures have also been proposed for power splitting, including inverse tapers [21], adiabatic tapers [22] and photonic crystals [23], which are limited by their narrow bandwidth.

Symmetric Y-junctions, consisting of a stem waveguide which branches into two diverging arms, are one of the most widely used power splitters and belong to the very roots of integrated optics. Y-junction studies were first conducted in the 1970s [24,25], with the first cascaded 1×8 power splitters being presented on ion-exchanged glass in the 1980s [26]. Nowadays, Y-junctions are routinely incorporated, for example, in ultra-high speed, high-quality lithium niobate electro-optic modulators [27]. Due to the simplicity of its design and operation principle [28,29], we consider these devices to be of special interest for SOI platforms, particularly for applications involving cascaded power splitting (e.g., integrated microspectrometers [30]. Moreover, Y-junctions with a bimodal stem waveguide offer a strong potential in datacom applications of growing interest, such as mode division multiplexing [12,31,32]. The transition between the stem and arms is nearly lossless and wavelength independent for small enough branching angles and a perfectly sharp junction tip between said branches [28]. However, the latter condition is hindered in real scenarios by the finite resolution of fabrication processes, hence requiring the application of more complex structures and optimization algorithms, such as slotted Y-junctions [18] or particle swarm optimization (PSO) [33]. This is particularly stringent in deep-ultraviolet (UV) lithography [34], with a substantially larger minimum feature size (MFS) compared to electron-beam (e-beam) technology. Moreover, since the junction tip is located at the midpoint of the stem waveguide, coinciding with the fundamental mode power maximum, deviations from the tip nominal design particularly penalize losses for the fundamental mode. Conversely, first-order modes present a zero-power profile at their central point, enabling power lobe separation without significant losses.

Subwavelength grating (SWG) metamaterials, since their first demonstration in silicon waveguides [35–40], have been advantageously used as a powerful tool for overcoming performance limitations of conventional silicon-based integrated photonic devices [41,42]. SWGs are periodic arrangements of different dielectric materials with a grating period (Λ) substantially smaller than the wavelength (λ) of the propagating light [43]. Under this condition, the medium acts on a macroscopic level as a homogeneous metamaterial which combines the optical properties of its dielectric constituents (e.g., effective index, dispersion, anisotropy), hence enabling the customization of the medium optical response through geometrical design. This innovative solution has been successfully applied to fiber-chip couplers, on-chip polarization management, mode-division multiplexing and integrated interferometer arrays, to name a few examples [6,12,44]. Specifically, subwavelength metamaterials have been applied to different power splitting architectures such as directional couplers [45–47] or MMIs [48,49], providing compact devices with enhanced performance over a broad bandwidth [50].

In this work, we incorporate an SWG metamaterial in a symmetric Y-junction to effectively reduce mode confinement around the junction tip and, hence, mitigate fundamental mode loss penalty caused by MFS limitations. Two different resolution scenarios have been taken into account for the optimization of the SWG Y-junction: (i) with an MFS of 100 nm, corresponding to current deep-UV fabrication process (dry lithography) and (ii) with an MFS of 50 nm for emerging high-resolution processes in photonic foundries (immersion lithography). Full three-dimensional finite-difference time-domain (3D FDTD) simulations show negligible fundamental mode excess losses (EL) within an ultra-broad bandwidth in excess of 300 nm for both MFS scenarios. In addition, our device presents robust fabrications tolerances to over- and under-etching deviations of up to ± 20 nm. A proof-of-concept device was fabricated, showing experimental excess losses lower than 0.2 dB in a 195 nm bandwidth for the best-case resolution scenario.

2. Principle of Operation and Device Design

As a reference framework for our proposed device, let us first consider a conventional symmetric Y-junction as depicted in Figure 1a, operating for fundamental and first-order transverse electric (TE) modes. The device comprises an input multimode waveguide (stem) of width W_0 and length L_s , and two single-mode S-shaped output arms of width $W = W_0/2$, length L_B and final separation H_a , followed by output straight waveguides of length L_0 . S-shaped waveguides are typically used to implement lateral displacements connecting two parallel straight waveguides due to their reduced losses [51]. An adiabatic taper of length L_T is also included to adapt the stem waveguide to the width of both arms at the fork ($W_T = 2W + H_{off}$). When the divergence angle at the junction between the two arms is small enough to consider an adiabatic transition [28], the input fundamental TE mode (TE₀) injected at the stem is divided into two in-phase TE₀ modes at the output arms due to the symmetry of the device. Similarly, when the first-order TE mode (TE₁) is injected, the power is again equally divided into two TE_0 modes of equal amplitude at the output arms, but with a π phase difference (φ) between them. In order to account for the MFS constraint of the fabrication process, we consider a gap of width H_{off} between the two arms at the junction tip.



Figure 1. Schematic of (**a**) a conventional symmetric Y-junction and (**b**) SWG Y-junction. These two devices operate for both TE_0 and TE_1 modes.

Our proposed device, displayed in Figure 1b, operates analogously to a conventional symmetric Y-junction, but incorporates SWG metamaterials in both input and output waveguides, while preserving the same arm offset (H_{off}). Arm width (W) and final separation (H_a) are maintained identical as in the conventional Y-splitter for the sake of comparison. The input strip waveguide of length L_I and width W_S evolves into an SWG

period Λ .

waveguide of length L_C through an adiabatic taper (length L_{TI}). This SWG region is key to reduce the modal confinement of the TE₀ mode and subsequently to minimize the radiation loss at the fork and improve its excess losses. Furthermore, the use of subwavelength structures allows to define geometrical parameters (period, duty cycle and H_{off}) with larger values than the considered MFS (i.e., 50 nm and 100 nm). In order to minimize mode mismatch at the interface between the input stem and the output arms, we utilized different duty cycles on both sides, $DC_S = a_S / \Lambda$ and $DC_A = a_A / \Lambda$, where a_S and a_A are the length of the silicon segments in the stem and in the arms, respectively, considering a constant

The device was optimized for an SOI platform with a core waveguide thickness of 220 nm and both top and buried silicon dioxide layers. At a wavelength of 1550 nm, the material refractive indices were $n_{Si} \sim 3.48$ and $n_{SiO2} \sim 1.44$. The device was simulated using a 3D FDTD solver [52] for two different fabrication resolution limits: 50 nm and 100 nm. Therefore, the parameter H_{off} was modified accordingly to each MFS scenario. The width of the Y-junction arms was W = 500 nm, ensuring compatibility with conventional interconnection waveguides. An SWG period of $\Lambda = 220$ nm was selected to avoid radiation and Bragg regimes. The list of the remaining geometrical design parameters is provided in Table 1.

Design	Parameter	Symbol	Value (µm)
SWG and conventional Y-junctions	Arm width	W	0.5
	Arm final separation	H_a	1.5
	Arm length	L_B	12.3
Conventional Y-junction	Stem waveguide length	L_S	13
	Taper length	L_T	4
	Output section length	L_O	9
SWG Y-junction	Input strip width	W_S	1.2
	Input strip length	L_I	2
	Input SWG taper	L_{TI}	10
	Output SWG taper	L_{TO}	6
	Central SWG section	L_{C}	13
	Output strip length	L_E	3

Table 1. Conventional and SWG Y-junction geometrical parameters.

The width of the SWG stem waveguide was optimized to avoid a weak confinement of the Bloch–Floquet TE₁ mode, which would lead to high TE₁ excess losses (EL_{TE1}) due to substrate leakage or mode radiation. TE₁ mode splitting can be enhanced by selecting a wider SWG waveguide width, at the expense of a stronger confinement for the Bloch–Floquet TE₀ mode and, therefore, higher TE₀ excess losses (EL_{TE0}). Figure 2 shows the effective index of the Bloch-Floquet TE₁ mode ($n_{eff,1}$) supported by the SWG stem waveguide as a function of the waveguide width. The effective index of the Bloch–Floquet TE₀ mode ($n_{eff,0}$) supported by the arms is also shown with a dashed red line. On this account, a width of the SWG stem waveguide of $W_S = 1200$ nm was chosen as a compromise between EL_{TE0} and EL_{TE1} .

To further optimize mode matching at the stem-arms interface, we judiciously adjusted the duty cycle on both parts of the device. For this purpose, we swept EL for different DC_A while keeping a constant DC_S of 50% (see Figure 3). We assumed two additional restrictions, i.e., that the chosen DC_A cannot violate the MFS and that the optimum DC_A values EL_{TE0} and EL_{TE1} may not necessarily be identical. For the MFS of 50 nm, the optimal loss balance for both TE₀ and TE₁ modes was achieved with a $DC_A = 60\%$ (see Figure 3a). For the MFS of 100 nm, we found minimum EL for TE₁ at $DC_A = 55\%$ (see Figure 3b).



Figure 2. Effective index of the Bloch–Floquet TE_1 mode for different widths of the SWG stem waveguide. The effective index of the Bloch–Floquet TE_0 mode in a 500 nm wide SWG waveguide is represented with a dashed red line.



Figure 3. Calculated excess loss of the SWG Y-junction for variable DC_A ($DC_S = 50\%$), for (a) MFS = 50 nm; (b) MFS = 100 nm.

3. Simulation Results and Tolerance Analysis

The performance comparison between the optimized SWG Y-junction (red) and its conventional counterpart (blue) is shown in Figure 4 (EL_{TE0} solid curve, EL_{TE1} dashed curve). For an MFS of 50 nm (Figure 4a), our device shows an excellent performance in a broad bandwidth of 300 nm, with EL_{TE0} below 0.1 dB for a wavelength range from 1400 nm to 1700 nm, and under 0.3 dB for the TE₁ mode in a 1300–1600 nm window. For comparison, EL_{TE0} is reduced by 0.35 dB compared to the conventional splitter in a 250 nm bandwidth (1350-1600 nm), while EL_{TE1} is only slightly increased. Considering the MFS of 100 nm (Figure 4b), the SWG Y-junction exhibits *EL*_{TE0} as low as 0.3 dB in a 350 nm bandwidth (1350-1700 nm) and EL_{TE1} under 0.45 dB in a 300 nm wavelength range (1300-1600 nm). A significant reduction for EL_{TE0} is achieved at the central design wavelength (1550 nm), from 0.99 dB for a conventional Y-junction down to 0.12 dB for the SWG Y-junction. Despite a minor increase in *EL*_{TE1}, the sum of both EL values is significantly reduced for the SWG device compared to the conventional Y-junction, providing a more even performance for both modes, for both 100 nm and 50 nm MFS designs. This outstanding performance is achieved in a broad bandwidth of 300 nm (1300–1600 nm), with the $EL_{TE0} + EL_{TE1}$ under 0.5 dB being the figure of merit. The SWG Y-junction shows improved performance for both 100 nm and 50 nm MFS designs, while the performance of the conventional Yjunction degrades rapidly with increasing MFS. Simulations also confirmed that the effect of temperature changes on device performance were negligible for variations of ± 10 K for both modes (TE₀ or TE₁), as well as for the two MFS designs.



Figure 4. Calculated TE₀ (solid curve) and TE₁ (dashed curve) excess loss of the SWG Y-junction (red) compared to the conventional Y-junction (blue): (**a**) MFS = 50 nm, optimized SWG Y-junction with $DC_A = 60\%$; (**b**) MFS = 100 nm, optimized SWG Y-junction with $DC_A = 55\%$.

We also evaluated the fabrication tolerance of the SWG Y-junction to etching errors of $\Delta \delta = \pm 10$ nm and $\Delta \delta = \pm 20$ nm from our nominal design, as illustrated in Figure 5. For this purpose, we resized the whole device by adding to the length and width of the silicon segments the corresponding deviation, since we consider fabrication errors as absolute variations of the waveguide dimensions. Then, $a_S' = a_S + \Delta \delta$ and $a_A' = a_A + \Delta \delta$ are the lengths of the silicon segments at the stem and the arms of the SWG Y-junction, and the width at the stem and of the arms are $W_S' = W_S + \Delta \delta$ and $W_A' = W + \Delta \delta$, respectively. For both MFS values, i.e., 50 nm (Figure 5a) and 100 nm (Figure 5b), the SWG Y-junction performance degradation is observed predominantly for the TE₁ mode when $\Delta \delta$ is negative, i.e., for over-etching errors. By contrast, the TE₀ mode exhibits robust tolerances, particularly for the MFS = 50 nm.



Figure 5. Tolerances to fabrication errors of $\Delta \delta = \pm 10, \pm 20$ nm for TE₀ (solid curves) and TE₁ (dashed curves) for the SWG Y-junction with (**a**) MFS = 50 nm and (**b**) MFS = 100 nm.

4. Fabrication and Experimental Characterization

A proof-of-concept device was fabricated using SOI wafers with the 220 nm thick Si layer and 2 μ m thick buried oxide (BOX). E-beam lithography was used to define the pattern, and the 220 nm thick Si layer was fully etched by inductively coupled plasma reactive ion etching. A SiO₂ upper cladding was deposited via chemical vapor deposition to protect the devices. Figure 6 shows the scanning electron microscope (SEM) images of the fabricated devices prior the cladding deposition. SEM image of the subwavelength Y-junction with an MFS of 100 nm is presented in Figure 6a, with a more detailed view of the tip in Figure 6b. Adhering to this previous arrangement, SEM images of the splitter with an MFS of 50 nm can be seen in Figure 6c,d. Detailed SEM image analysis shows a

slight over etching, with deviations below $\Delta \delta < -10$ nm in SWG segments of both arms and stem. A Mach-Zehnder interferometer (MZI) comprising two SWG Y-splitters was used to evaluate the coupler performance. High-efficiency and broadband SWG edge couplers [53,54] were used to couple the light in and out of the chip within the entire operational bandwidth of the device.



Figure 6. Scanning electron microscope images, for an MFS = 100 nm of (**a**) the complete SWG Y-junction and (**b**) the fork. For an MFS = 50 nm, SEM pictures of (**c**) the complete device and (**d**) the fork.

The fabricated device was characterized with two tunable lasers sweeping the wavelength range from 1.41 to 1.68 µm, fully covering the S, C, L and U telecom bands, and partially the E-band. Polarization at the chip input was controlled through a three-paddle fiber polarizer followed by a linear polarizer, a half-wave plate and a lensed polarization maintaining fiber. The polarization state was verified using a free-space polarimeter for the entire wavelength range (1.41–1.68 μ m). The polarization state at the chip output was monitored with a Glan-Thompson polarizer, and a $40 \times$ microscope objective was used to focus the light onto a germanium photodetector. The difference between the transmittance of the measured MZI transmittance maxima and a reference waveguide, with the same waveguide length and number of bends as the MZI structure, allowed us to estimate the excess loss due to the SWG Y-junction. In order to conduct a conservative evaluation on the performance of our device, we chose the reference waveguide with the lowest measured losses among those available. Two reference Y-junctions (with an MFS of 100 nm and 50 nm, respectively) were also characterized in the 1410–1680 nm range to compare the performance of the SWG Y-junction with that of the conventional counterpart. The measured loss EL_{TE0} is shown in Figure 7.

The fabricated SWG Y-junction shows EL_{TE0} under 0.72 dB over the full bandwidth of 270 nm (1410–1680 nm) for the MFS = 100 nm. This value is reduced below 0.5 dB in a 210 nm bandwidth (1470–1680 nm). For the MFS = 50 nm, the EL_{TE0} is further reduced under 0.4 dB for the entire measured wavelength range, and under 0.22 dB in a 195 nm bandwidth (1485–1680 nm). This experimental performance implies significant improvement compared to the reference conventional Y-junction for both MFS scenarios, and particularly for the higher MFS case. Conventional Y-junctions show higher EL in all analyzed ranges, and a greater deterioration for shorter wavelengths, demonstrating the potential of SWG for circumventing fabrication resolution limitations. Table 2 summarizes the main parameters of our SWG Y-junction, compared with the performance of the stateof-the-art power splitters.



Figure 7. Measured EL for the TE₀ mode for the SWG Y-junction (red) and the conventional Y-junction (blue) when (**a**) MFS = 50 nm and (**b**) MFS = 100 nm. Simulation results are also included for reference in all cases (dashed).

Table 2. Experimental performance comparison of state-of-the art power splitters. (* Values estimated from manuscript figures and data).

Ref	Structure	Bandwidth (nm)	EL _{TE0} (dB)	MFS (nm)	Length (µm)
[16]	Directional coupler	88	<1.0	200	31.4
[17]	Bent directional coupler	80	<1.0	110	50
[18]	Slotted Y-junction	390	<1.0	100	200
[20]	MMI coupler	60	<1.0	500	27
[21]	Inverse tapers	40	<4.0 *	100	16.1
[22]	Adiabatic tapers	100	<0.6	200	40
[29]	Tapered Y-junction	100	< 0.3	0	30
[33]	PSO Y-junction	80	<1.0	200	2
[47]	SWG directional coupler	65	<1.0	90	4.5
[45]	SWG directional coupler	200	<1.0	110 *	17.3
[49]	SWG MMI	325	<1.0	95 *	25.4
This work	SWG Y-junction	270	< 0.4	50	41.3
This work	SWG Y-junction	270	<0.7	100	41.3

5. Discussion and Conclusions

We have proposed a new type of high-performance power splitter based on a Yjunction that incorporates subwavelength metamaterials. This strategy substantially reduces fundamental mode losses arising from limited fabrication resolution, particularly near the junction tip. For a high-resolution scenario (MFS = 50 nm), simulated excess losses for the fundamental mode are below 0.1 dB in an ultra-broad bandwidth of 300 nm (1400–1700 nm), and under 0.3 dB for the first-order mode in a 1300–1600 nm window. Considering a 100 nm MFS, our design presents EL for both TE₀ and TE₁ modes below 0.5 dB in 300 nm bandwidth (1300–1600 nm). Compared with a conventional Y-junction, this yields a reduction in TE₀ loss at the central design wavelength (1550 nm) from 0.99 dB down to 0.12 dB, with only a small penalty on TE₁ loss, the latter indeed being irrelevant for single-mode operation.

Furthermore, our device demonstrates robust fabrication tolerances to etching errors up to ± 20 nm, particularly for the TE₀ mode. Our simulation results have been validated by a proof-of-concept experimental device, yielding and EL < 0.22 dB in a 195 nm bandwidth (1485–1680 nm) for an MFS = 50 nm and EL < 0.5 dB in a 210 nm bandwidth (1470–1680 nm) for an MFS = 100 nm. Additional experimental characterization of the device, including TE₁ measurements and cascaded stages for enhanced accuracy, is expected in future works.

We believe that the SWG metamaterial engineered Y-junction power splitter will be useful for a wide range of applications of silicon photonic integrated circuits, with promising prospects for mode-division multiplexing, sensing, spectroscopy and any other application in which beam splitters are a cornerstone for optical power distribution.

Author Contributions: Conceptualization, P.C., A.V.V.; methodology and supervision, D.G.-A.; software, design, experimental validation and original draft preparation, R.F.d.C.; supervision, project administration and funding acquisition, A.V.V.; writing—review and editing, all authors. All authors have read and agreed to the published version of the manuscript.

Funding: This work has been funded in part by the Spanish Ministry of Science and Innovation (MICINN) under grants RTI2018-097957-B-C33, RED2018-102768-T and TEC2015-71127-C2-1-R (FPI BES-2016-077798) and the Community of Madrid—FEDER funds (S2018/NMT-4326). This project has received funding from the Horizon 2020 research and innovation program under Marie Sklodowska-Curie grant No. 734331.

Data Availability Statement: The data presented in this study are available on request from the corresponding author.

Conflicts of Interest: The authors declare no conflict of interest.

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