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Effect of Step Gate Work Function on InGaAs p-TFET for Low Power Switching Applications

Sayed Md Tariful Azam^{1,2}, Abu Saleh Md Bakibillah^{3,*}, Md Tanvir Hasan² and Md Abdus Samad Kamal^{4,*}

- ¹ Department of Electrical and Computer Engineering, Technische Universität Kaiserslautern, 67653 Kaiserslautern, Germany; sazam@rhrk.uni-kl.de
- ² Department of Electrical and Electronic Engineering, Jashore University of Science and Technology, Jashore 7408, Bangladesh; tan_vir_bd@yahoo.com
- ³ School of Engineering, Monash University, Bandar Sunway, Subang Jaya 47500, Malaysia
- ⁴ Graduate School of Science and Technology, Gunma University, 1-5-1 Tenjincho, Kiryu 376-8515, Japan
 - Correspondence: asm.bakibillah@monash.edu (A.S.M.B.); maskamal@ieee.org (M.A.S.K.)

Abstract: In this study, we theoretically investigated the effect of step gate work function on the InGaAs p-TFET device, which is formed by dual material gate (DMG). We analyzed the performance parameters of the device for low power digital and analog applications based on the gate work function difference $(\Delta \varphi_{S-D})$ of the source (φ_S) and drain (φ_D) side gate electrodes. In particular, the work function of the drain (φ_D) side gate electrodes was varied with respect to the high work function of the source side gate electrode (Pt, $\varphi_S = 5.65 \text{ eV}$) to produce the step gate work function. It was found that the device performance varies with the variation of gate work function difference $(\Delta \varphi_{S-D})$ due to a change in the electric field distribution, which also changes the carrier (hole) distribution of the device. We achieved low subthreshold slope (SS) and off-state current (I_{off}) of 30.89 mV/dec and 0.39 pA/µm, respectively, as well as low power dissipation, when the gate work function difference ($\Delta \varphi_{S-D} = 1.02 \text{ eV}$) was high. Therefore, the device can be a potential candidate for the future low power digital applications. On the other hand, high transconductance (g_m), high cut-off frequency (f_T), and low output conductance (g_d) of the device at low gate work function difference ($\Delta \varphi_{S-D} = 0.61 \text{ eV}$) make it a viable candidate for the future low power analog applications.

Keywords: p-TFET; gate work function; dual material gate; InGaAs; low power switching

1. Introduction

The band-to-band tunneling transport mechanism of tunnel field effect transistors (TFETs) allows the device to operate on low supply voltage (V_{DD}) and to overcome the subthreshold slope limit (SS \geq 60 mV/dec) of traditional metal oxide semiconductor field effect transistors (MOSFETs), which makes TFET a potential candidate for the future low power devices [1-5]. TFETs have lower power consumption in digital circuits and have higher sensitivity and transconductance per unit of current in analog circuits compared to the conventional MOSFETs [1,3,6–8]. In particular, low and direct bandgap III–V materials have attracted a lot of attention for TFET devices, due to their inherent material properties (such as direct band gap, high electron mobility, and low exciton binding energy) as compared to Si [2]. They have also higher tunneling efficiency due to their shorter tunneling distance and lower phonon emission. Among these materials, ternary III-V materials have a higher degree of compositional dependency, allowing designers to fine-tune the material properties to meet their requirements [9,10]. Moreover, nowadays, InGaAs is a very suitable material for TFET devices leading to open new opportunities to make the compact integrated circuits for next generation electronic as well as optoelectronic/photonic applications [2].

Unlike n-TFETs, p-TFETs (usually n-i-p doping structure) with III–V materials have built-in issues [2]. Due to the low conduction band density of states of III–V materials,



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Copyright: © 2021 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (https:// creativecommons.org/licenses/by/ 4.0/). a heavily n-doped source of p-TFETs induces large conduction band degeneracy, which causes exponential tail from Fermi distribution and thus, SS is increased. The optimal source doping should be lower than n-TFETs while focused on steep SS. On the other hand, reduced source doping results in a lower electric field at the tunnel junction, which reduces drain current (I_D). To date, the counter effect of doping on I_D and SS has been subsidized by using heterostructure or a heavily counter doped pocket between the source and channel regions to achieve steep SS and high I_D with high I_{on}/I_{off}, similar to n-TFETs (for complementary switching) [10–13]. In line with this expectation, the dual material gate (DMG) design is a leading contender for achieving steep SS and high I_D, because it combines the advantages of dual-material-gate and double-gate structures.

The DMG design was first proposed by Wei Long to suppress the short channel effect of MOSFET devices [14], where it was shown that in DMG devices instead of a single metal gate, two metal gates are positioned laterally on the gate region and the gate contact on the source side has higher work function than the gate contact on the drain side. The DMG structure reduces the electric field on the drain region and hence, the electric field is distributed, which increases channel efficiency. The distributed electric field and higher peak on the source side of the channel accelerate the charge carriers more rapidly, which makes DMG devices a potential candidate for high-speed applications. The DMG design is investigated in various recent devices, e.g., a DMG design in CNT-FET is reported in [15], the applicability of DMG devices for digital applications using gate-all-around (GAA) and GaN are reported in [16,17] and the applicability of DMG devices for subthreshold analog/RF applications are reported in [18,19]. The DMG designs are also explored for TFETs [20–24].

However, to the best of our knowledge, no DMG design for the InGaAs p-TFET device has been reported. For this paper, we investigated the DMG design on an InGaAs p-TFET device in terms of the step gate work function produced by the work function difference between the source and drain side gate electrodes. The work function of the drain side gate electrodes was regulated with reference to the high work function of the source side gate electrodes to generate the step gate work function. Our approach of using dual material gate with different work functions was inspired by our previous work [17], where the performance of sub-10-nm GaN-based DG-MOSFETs with different gate work function combinations were investigated and it was found that the short-channel effects (SCEs) can be significantly reduced using gates made of dual materials. We inspected the device's suitability for low-power digital and analog applications by analyzing capacitance and performance parameters. The results show improvements in I_{on} , I_{off} , I_{on}/I_{off} , SS, and DIBL over the reported data in this domain [23]. The paper is organized as follows. Section 2 describes the device structure and Section 3 provides the computation methods. Section 4 presents the results of transfer characteristics, output characteristics, and physical properties of the device. Section 5 gives the capacitance characteristics of the device and device level performance parameters for low power digital and analog applications. Finally, Section 6 draws the conclusion.

2. Device Structure

In this paper, a double gate p-TFET device has been studied using dual material gate structure to improve the device performance. The structure of the proposed p-type InGaAs DMG-TFET device is illustrated in Figure 1, where the source, channel, and drain lengths are 5 nm, 20 nm, and 5 nm, respectively [5]. We considered gate width as 1 μ m. For the proposed device, a channel thickness of 10 nm and a physical gate oxide (HfO₂, $\varepsilon = 22 \varepsilon_0$) thickness of 3 nm were used. Our study mainly exploited a 2D simulation setup with cross-sectional view of the proposed p-TFET device structure, where *x*- and *y*-axes are defined along the channel length and channel thickness, respectively. The doping concentrations, i.e., acceptor (N_A) and donor (N_D) of source and drain regions were considered as 1×10^{19} cm⁻³ (N_D) and 5×10^{18} cm⁻³ (N_A), respectively. In the channel region light, doping concentration of 1×10^{16} cm⁻³ (N_D) was used.



Figure 1. Schematic structure of the proposed double gate p-InGaAs TFET device.

The formation of step gate work function requires two types of gate electrodes, e.g., high and low work function electrodes on the source side (ϕ_S) and the drain side (ϕ_D), respectively. In this work, we considered the same length for both electrodes, i.e., $L_{\phi S} = L_{\phi D} = 10$ nm. Since a high work function source side gate electrode improves carrier efficiency in channel under the ϕ_S region [20,24], we considered $\phi_S = 5.65$ eV (Pt). On the other hand, low work function gate electrodes such as Ni, Mo, and W were employed in the ϕ_D region. In the literature, the gate electrodes on the source are denoted as the tunneling (control) and auxiliary (screen) gates, respectively [22–24]. The device performance is analyzed in terms of step gate work function induced by the difference in work function ($\Delta \phi_{S-D}$) between the source side (ϕ_S) and the drain side (ϕ_D) gate electrodes. The differences in work function ($\Delta \phi_{S-D}$) considered in this study are given in Table 1.

Table 1. Work function combinations and differences considered in this study.

Source Side Electrode, ϕ_S (eV)	Drain Side Electrode, φ_D (eV)	Work Function Difference, $\Delta \varphi_{S-D}$ (eV)
Pt (5.65)	Ni (5.04)	0.61
	Mo (4.95)	0.70
	W (4.63)	1.02

3. Computational Methods

We conducted all simulations using Silvaco ATLAS TCAD [25] and the simulation setup was adopted from our previous work [5] and Kim et al. [9]. The carrier distribution was calculated using the Fermi model. To compute the carrier recombination, we used the Shockley–Read–Hall (SRH) and auger recombination models, as well as the bandgap narrowing model that describes the high doping effect on the bandgap. Low field mobility due to doping density was taken into account by the concentration dependent mobility model, while field velocity saturation was taken into account by the field dependent mobility model. We considered quantum effects using the density gradient quantum moments model [5,9]. To tunnel through the bandgap using trap states, we used the trap assisted tunneling model with phonon scattering effect. A nonlocal band-to-band tunneling model was used to explain nonlocal interband tunneling effect. The on-state (source-to-channel) and off-state (drain-to-channel) tunneling were considered as separate tunneling regions. The tunneling probability *T*(*E*) is calculated as

$$T(E) = \exp\left(-\frac{4\sqrt{2m^*}E_g^{\frac{3}{2}}}{3|e|\hbar\xi}\right)$$
(1)

where m^* is the effective mass, E_g is the bandgap energy, ξ is the electric field, and \hbar is the reduced Planck constant. The simulations were performed at room temperature (300 K). In this paper, I_{on} and I_{off} are considered as drain current (I_D) at $V_{DD} = V_{GS} = -0.5$ V and

 $V_{DD} = -0.5 \text{ V}$, $V_{GS} = 0 \text{ V}$, respectively. The DIBL and SS were calculated at constant I_D of $1 \times 10^{-9} \text{ A}/\mu\text{m}$. The simulations were also carried out at a frequency of 1 MHz.

4. Results and Discussion

The transfer characteristics of the device for differences in work functions are shown in Figure 2a. It is found that for the lowest work function difference ($\Delta \varphi_{S-D} = 0.61 \text{ eV}$), the device exhibits the highest I_{on} (83.2 µA/µm) and I_{off} (28.3 pA/µm). The inset figure of Figure 2a shows that I_{on} decreases linearly from 83.2 µA/µm to 38.9 µA/µm when the work function difference is increased from $\Delta \varphi_{S-D} = 0.61 \text{ eV}$ to $\Delta \varphi_{S-D} = 1.02 \text{ eV}$. Figure 2b shows the output characteristics of the device at V_{GS} = -0.5 V, where the I_D-V_{DD} curve shows that the increasing rate of drain current (I_D) with respect to drain voltage (V_{DD}) is higher for $\Delta \varphi_{S-D} = 0.61 \text{ eV}$ and $\Delta \varphi_{S-D} = 0.7 \text{ eV}$ compared to $\Delta \varphi_{S-D} = 1.02 \text{ eV}$, which means that saturation is not reached yet for $\Delta \varphi_{S-D} = 1.02 \text{ eV}$. Delayed saturation characteristics of $\Delta \varphi_{S-D} = 1.02 \text{ eV}$ can be improved by higher source doping that reduces the source depletion [26]. On the other hand, higher source doping increases SS of the device and introduces Fermi tail.



Figure 2. (a) Transfer characteristics (I_D - V_{GS}) at $V_{DD} = -0.5$ V; inset shows I_{on} as a function of work function difference ($\Delta \phi_{S-D}$) and (b) output characteristics (I_D - V_{DD}) at $V_{GS} = -0.5$ V.

The band profiles of the device for both off-state ($V_{DD} = -0.5 \text{ V}$, $V_{GS} = 0 \text{ V}$) and on-state ($V_{DD} = V_{GS} = -0.5$ V) are shown in Figure 3. In a p-TFET, the on-state negative gate bias shifts the bands up to align the conduction band of the source region with the valence band of the channel region, allowing holes to tunnel from the conduction band to the valence band. In other words, the electron tunnels from the valence band of the channel region to the conduction band of the source region. In this condition, the potential of the high work function gate electrode is higher than the potential of the low work function gate electrode for the same applied negative gate bias and the effect is reflected in the channel region. It is found that in the ϕ_S region, a high work function gate electrode Pt causes both the conduction band and the valence band to have a high potential in all $\Delta \phi_{S-D}$ conditions. On the contrary, both the conduction band and the valence band have lower potential in the ϕ_D region (under the low work function electrode) than in the ϕ_S region, and their potential varies according to the work function of the gate electrodes. As a result, the energy bands of device in the channel region show step-like (or undulated) features. Furthermore, a lower potential in the ϕ_D region indicates that carriers in that region have less energy. Hence, the drain to channel tunneling probability is low in the off-state.

The fluctuation of I_{off} , I_{on}/I_{off} , SS, and DIBL as a function of gate work function difference ($\Delta\phi_{S-D}$) is shown in Figure 4a,b. When the work function difference is increased from 0.61 eV to 1.02 eV, I_{off} reduces on logarithmic scale from 28.3 pA/m to 0.39 pA/m. As a result, at $\Delta\phi_{S-D} = 1.02$ eV, the highest I_{on}/I_{off} ratio of 9.94×10^7 is obtained. It is also observed that SS drops with an increase in $\Delta\phi_{S-D}$. The lowest SS of 30.89 mV/dec is achieved for $\Delta\phi_{S-D} = 1.02$ eV. The highest SS of 37.84 mV/dec is observed when $\Delta\phi_{S-D} = 0.61$ eV, which is still less than the traditional SS limit of 60 mV/dec. Unlike SS, the DIBL of the device increases with the increase of $\Delta\phi_{S-D}$. We found approximately the same DIBL for $\Delta\phi_{S-D} = 0.61$ eV and $\Delta\phi_{S-D} = 0.7$ eV, which are 49.25 mV/V and 49.81 mV/V, respectively. In the case of $\Delta\phi_{S-D} = 1.02$ eV, the highest DIBL of 59.41 mV/V is achieved.



Figure 3. Conduction band (CB) and valance band (VB) profiles along the channel—dot line: off-state ($V_{DD} = -0.5 \text{ V}$, $V_{GS} = 0 \text{ V}$), solid line: on-state ($V_{DD} = V_{GS} = -0.5 \text{ V}$).



Figure 4. (a) I_{off} and I_{on}/I_{off} and (b) SS and DIBL as a function of work function difference ($\Delta \phi_{S-D}$).

The surface potential of the device in the off-state ($V_{DD} = -0.5 \text{ V}$, $V_{GS} = 0 \text{ V}$) and on-state ($V_{DD} = V_{GS} = -0.5 \text{ V}$) is shown in Figure 5. The negative drain bias and gate bias reduce the surface potential in the drain and channel regions, respectively, while the surface potential in the grounded source region remains higher. However, in the channel region, the surface potential varies according to the work function difference ($\Delta \varphi_{S-D}$). Hence, the highest and lowest surface potentials in the channel region, respectively, are caused by high work function difference ($\Delta \varphi_{S-D} = 1.02 \text{ eV}$) and low work function difference ($\Delta \varphi_{S-D} = 0.61 \text{ eV}$). The surface potential of single material gate devices remains constant through the channel region according to their work function. However, the surface potential of dual material gate devices introduces a step-like feature in the channel region according to their respective work functions [16,23].



Figure 5. Surface Potential along the channel—dot line: off-state ($V_{DD} = -0.5 \text{ V}$, $V_{GS} = 0 \text{ V}$), solid line: on-state ($V_{DD} = V_{GS} = -0.5 \text{ V}$).

As shown in Figure 5, a high work function electrode has a strong impact in the ϕ_S region. As a result, the surface potential dips in the middle of the ϕ_S region, forming a trough. On the other hand, a low work function in the ϕ_D region increases surface potential in the middle of ϕ_D region, creating a crest that shades the ϕ_S region from the high drain bias (V_{DD}) effect. As a result, the surface potential difference between the ϕ_S and ϕ_D regions forms the step-like feature in the channel region. When $\Delta\phi_{S-D} = 0.61$ eV and 0.7 eV, the surface potential in the crest is lower than the trough surface potential; therefore, it is approximately constant (small gradient) around the metal junction. However, when $\Delta\phi_{S-D} = 1.02$ eV, the crest and trough surface potentials are approximately the same, and the surface potential becomes constant (flat) around the metal junction.

Figure 6a,b show the electric field and hole velocity of the device, respectively. The high electric field in the tunnel junction of the source and channel region is nearly the same in all circumstances due to the same ϕ_S electrode. The electric field fluctuates with ϕ_D in the drain region, with the largest peak occurring at the channel–drain junction for a high work function difference ($\Delta \phi_{S-D} = 1.02 \text{ eV}$). The work function difference between two electrodes raises negative peaks around the junction [23,24], as shown in the inset of the figure. It is found that a low work function difference ($\Delta \phi_{S-D} = 0.61 \text{ eV}$) has the lowest negative peak. On the contrary, a high work function difference ($\Delta \phi_{S-D} = 1.02 \text{ eV}$) has the two highest negative peaks. The opposite potential trend appears at the transition of the two gates is responsible for negative electric field peaks [24]. Since the carrier velocity (here, majority carriers are holes) are proportional to the electric field, in Figure 6b, the hole velocity imitates the peaks of the electric field curves. Like the electric field, hole velocity is high at the source–channel junction of two electrodes and has negative peaks. Then, the velocity increases again towards the drain.



Figure 6. (a) Electric Field; inset shows zoomed electric field at the circled region and (b) Hole velocity along the channel at on-state ($V_{DD} = V_{GS} = -0.5$ V).

The on-state hole concentration contour plots of the device for different cases are shown in Figure 7. In Figure 7a, the hole concentration in the ϕ_S region is higher than the ϕ_D region for $\Delta\phi_{S-D} = 0.61$ eV. In Figure 7b, the hole concentration becomes confined in the ϕ_S region for $\Delta\phi_{S-D} = 0.7$ eV. It is found that the hole concentration in the ϕ_D and drain regions are lower than the previous case. In these two cases, holes are distributed from the ϕ_S region near the metal junction, and poorly distributed in the ϕ_D and drain regions when $\Delta\phi_{S-D} = 1.02$ eV. Note that, in all cases, the hole concentration in the ϕ_S region is higher on semiconductor–dielectric material interface than the middle of the channel (along *y*-axis). When compared to the electric fields of the device in Figure 6a, it appears that the electric field decreases as hole confinement increases in the ϕ_S region. The next section.



Figure 7. Hole concentration contours at on-state ($V_{DD} = V_{GS} = -0.5$ V) for (**a**) $\Delta \phi_{S-D} = 0.61$ eV, (**b**) $\Delta \phi_{S-D} = 0.7$ eV, and (**c**) $\Delta \phi_{S-D} = 1.02$ eV.

5. Performance Parameter Analysis

5.1. Capacitance Analysis

We started by examining the device's C-V curves for different gate work functions (as shown in Figure 8), as capacitance characteristics are crucial in analyzing both digital and analog device performance. In Figure 8a, a high work function electrode (Pt) on the ϕ_S region results in a high gate-to-source (C_{GS}) capacitance. On the other hand, low work function materials on the ϕ_D region reduce gate-to-drain (C_{GD}) capacitances in all circumstances. Hence, we achieved a negligible miller effect, which has been a significant concern for TFET devices [27], and reduced output voltage overshoot and undershoot is expected in large-signal transient response in all circumstances. Moreover, Figure 8a shows that for $\Delta\phi_{S-D} = 1.02$ eV, both gate-to-source (C_{GS}) and gate-to-drain (C_{GD}) capacitances are higher than the other two cases. Figure 8b depicts the total (gate) capacitance (C_{GG}~C_{GS} + C_{GD}), which exhibits the similar characteristics, with the highest and lowest total (gate) capacitance (C_{GG}) being $\Delta\phi_{S-D} = 1.02$ eV and $\Delta\phi_{S-D} = 0.61$ eV, respectively. The total (gate) capacitance (C_{GG}) remains approximately the same when $\Delta\phi_{S-D} = 0.61$ eV and $\Delta\phi_{S-D} = 0.7$ eV.



Figure 8. (a) Dot line: Gate-to-Drain (C_{GD}) and solid line: Gate-to-Source (C_{GS}) capacitance (b) total capacitance (C_{GG}) as a function of Gate Voltage (V_{GS}) at $V_{DD} = -0.5$ V.

5.2. Digital Performance Parameters

To investigate the device's digital performance, different parameters were considered, e.g., intrinsic speed ($\tau = C_{GG}V_{DD}/I_{on}$), leakage power ($P_{leak} = nI_{off}V_{DD}$), dynamic power ($P_{dyn} = 0.5 \times nI_{on}V_{DD}\alpha$), total power ($P_{total} = P_{leak} + P_{dyn}$), dynamic energy ($E_{dyn} = 0.5 \times nC_{GG}V_{DD}^2\alpha$), leakage energy ($E_{leak} = n^2I_{off}V_{DD}\tau$), and total energy ($E_{total} = E_{leak} + E_{dyn}$). The logic depth n = 50 and activity factor $\alpha = 2\%$ were used [28]. The calculated values of these parameters are listed in Table 2.

	$\Delta \phi_{S-D}$ (eV)		
Parameters	0.61	0.7	1.02
τ (ps)	2.22	2.55	5.07
P _{leak} (μW/μm)	$7.09 imes10^{-4}$	$4.53 imes 10^{-5}$	9.77×10^{-6}
$P_{dyn} (\mu W/\mu m)$	20.8	18.2	9.71
P _{total} (μW/μm)	20.8	18.2	9.71
E _{leak} (aJ/μm)	$78.6 imes 10^{-3}$	5.77×10^{-3}	2.47×10^{-3}
E _{dyn} (aJ/μm)	46.2	46.4	49.2
E _{total} (aJ/μm)	46.2	46.4	49.2

 Table 2. Digital performance parameters.

It is found that the highest gate capacitance (C_{GG}) at $\Delta \varphi_{S-D} = 1.02$ eV results in ~2 times higher intrinsic speed (τ). The leakage power (P_{leak}) is proportional to I_{off} and therefore, P_{leak} dissipation at $\Delta \varphi_{S-D} = 1.02$ eV is ~13.78 × 10⁻³ times lower than at $\Delta \varphi_{S-D} = 0.61$ eV. In addition, the lowest I_{on} at $\Delta \varphi_{S-D} = 1.02$ eV results in the lowest dynamic power (P_{dyn}). Therefore, $\Delta \varphi_{S-D} = 1.02$ eV has the lowest total power (P_{total}) dissipation. A high gate capacitance (C_{GG}) of $\Delta \varphi_{S-D} = 1.02$ eV slightly increases the dynamic energy consumption (E_{dyn}) of the device than other cases of $\Delta \varphi_{S-D}$. In spite of the highest intrinsic speed (τ) at $\Delta \varphi_{S-D} = 1.02$ eV, the lowest I_{off} of the device gives the lowest leakage energy consumption (E_{leak}). The result shows that the dynamic component of power and energy of the device play the key role in total power (P_{total}) dissipation and energy (E_{total}) consumption of the device for different $\Delta \varphi_{S-D}$. Since the low power device is the primary concern for modern digital applications, with the lowest power dissipation at $\Delta \varphi_{S-D} = 1.02$ eV (about half of the other two cases and slightly higher energy consumption), the high work function difference model fits well for digital application requirements.

5.3. RF Performance Parameters

The device's RF performance was measured in terms of transconductance ($g_m = I_D/V_{GS}$), output conductance ($g_d = dI_D/dV_{DD}$), cut-off frequency ($f_T = g_m/2\pi C_{GG}$), and transconductance generation factor (TGF = g_m/I_D). Figure 9a,b shows the transconductance (g_m) and cut-off frequency (f_T) of the device for different $\Delta \phi_{S-D}$ as a function of gate voltage (V_{GS}). In Figure 9a, the inset figure shows the output conductance (g_d) as a function of $\Delta \phi_{S-D}$ at $V_{\text{CS}} = -0.5$ V. High transconductance (g_m) ensures high amplification and high cut-off frequency (f_T) is the key parameter for high-speed applications to analyze the device's gain [29]. The highest drain current (I_D) at $\Delta \phi_{S-D} = 0.61$ eV results in the highest transconductance g_m (426.29 μ S/ μ m), which is ~1.605 times higher than $\Delta \phi_{S-D} = 1.02$ eV. The lowest output conductance (g_d) and highest transconductance (g_m) of $\Delta \phi_{S-D} = 0.61$ eV result in the highest voltage gain ($A_v = g_m/g_d$), as seen in the inset of Figure 9a. The lowest gate capacitance (C_{GG}) and highest transconductance of the device at $\Delta \phi_{S-D} = 0.61$ eV also gives the highest cut-off frequency $f_T = 183.72$ GHz, which is 1.71 times higher than at $\Delta \phi_{S-D} = 1.02$ eV. Figure 9c depicts the device's transconductance generation factor (TGF) as a function of drain current (I_D) , which is a key parameter for low power analog subthreshold applications [30]. It is referred to as the transconductance-to-current ratio (g_m/I_d) as well as device efficiency in the literature [29]. It measures the efficiency of the device to convert current (power) into transconductance (speed) [31]. Due to steep SS of the device at $\Delta \phi_{S-D} = 1.02$ eV, the TGF is also found to be steep. Here, all cases match the traditional FET limit (38.5 μ S/ μ A) for the same drain current (I_D). In the subthreshold region, $\Delta \phi_{S-D} = 0.61$ eV has higher TGF than $\Delta \phi_{S-D}$ = 0.7 eV and lower TGF than $\Delta \phi_{S-D}$ = 1.02 eV. In capacitive load circuits, a lower TGF implies lower input drivability, which indicates higher power dissipation. On the other hand, higher TGF costs in terms of linearity of the device [30]. With the highest transconductance



Figure 9. (a) Transconductance (g_m), (b) cut-off frequency (f_T) as function of Gate Voltage (V_{GS}), and (c) transconductance to current ratio (gm/Id) as function of drain current (Id) at V_{DD} = -0.5 V; inset shows output conductance (g_d) at V_{DD} = V_{GS} = -0.5 V as a function of work function difference ($\Delta\phi_{S-D}$).

6. Conclusions

In this paper, we have investigated the effect of step gate work function on the InGaAs p-TFET device based on the gate work function difference ($\Delta \phi_{S-D}$) of the source (ϕ_S) and drain (ϕ_D) side gate electrodes. Firstly, we have analyzed the transfer and output characteristics, and physical properties of the device. The results show that the work function difference ($\Delta \phi_{S-D}$) changes the electric field on the channel by creating a potential difference in energy bands between the ϕ_S and ϕ_D regions. We achieved the lowest SS (30.86 mV/dec), I_{off} (0.39 × 10⁻¹² A/µm), and minimum I_{on}/I_{off} ratio (9.97 × 10⁷) for high work function difference $\Delta \phi_{S-D} = 1.02$ eV. Finally, we have explored the digital and analog performance parameters at the device level. It is found that the device with a high work function difference $\Delta \phi_{S-D} = 1.02$ eV dissipates the least amount of power and consumes the least amount of leakage energy, making it suitable for digital applications. On the other hand, a low work function difference $\Delta \phi_{S-D} = 0.61$ eV results in the lowest output conductance g_d (29.4 μ S/ μ m), maximum transconductance g_m (426 μ S/ μ m), and cut-off frequency f_T (184 GH_z). At $\Delta \phi_{S-D} = 0.61$ eV, the lowest g_d and highest g_m produce the largest voltage gain, which is an important parameter in analog applications. The findings reveal that the InGaAs p-TFET can be used for both low-power digital and analog applications by tuning the step gate work function of the device. From the above discussion, we can conclude that InGaAs TFETs will be suitable for future low-power integrated switching circuit applications.

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