Supporting Information

Highly Aligned Polymeric Nanowire Etch-Mask Lithography enabling the integration of Graphene Nanoribbon Transistors

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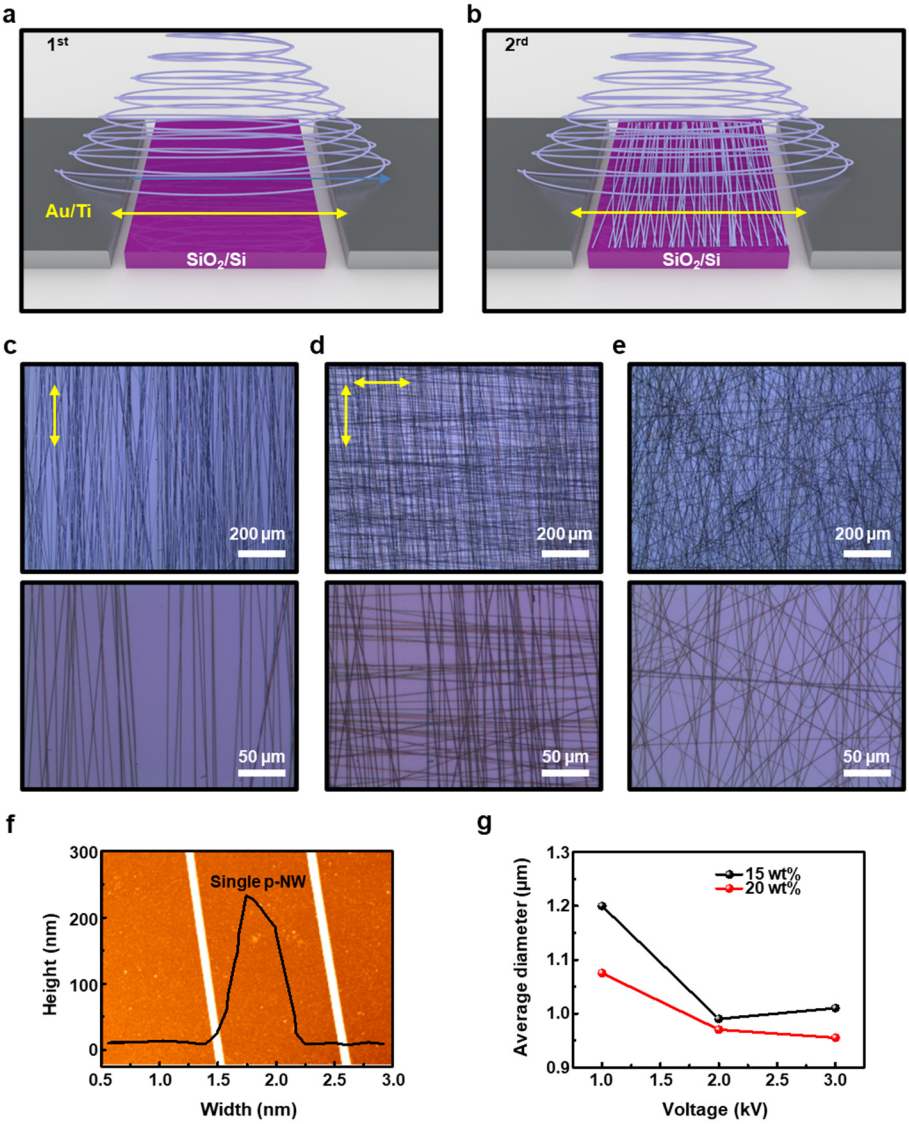

Figure S1. a-b) Schematic illustration of the first and second alignment of p-NWs on a SiO_2/Si substrate using a bridged collector. c-e) Optical micrographs on the control experiments single, crossed, and random networks of p-NWs on the substrates. f) Representative AFM image and corresponding height profile. g) Concentration effect on the applied voltages in the electrospinning process.

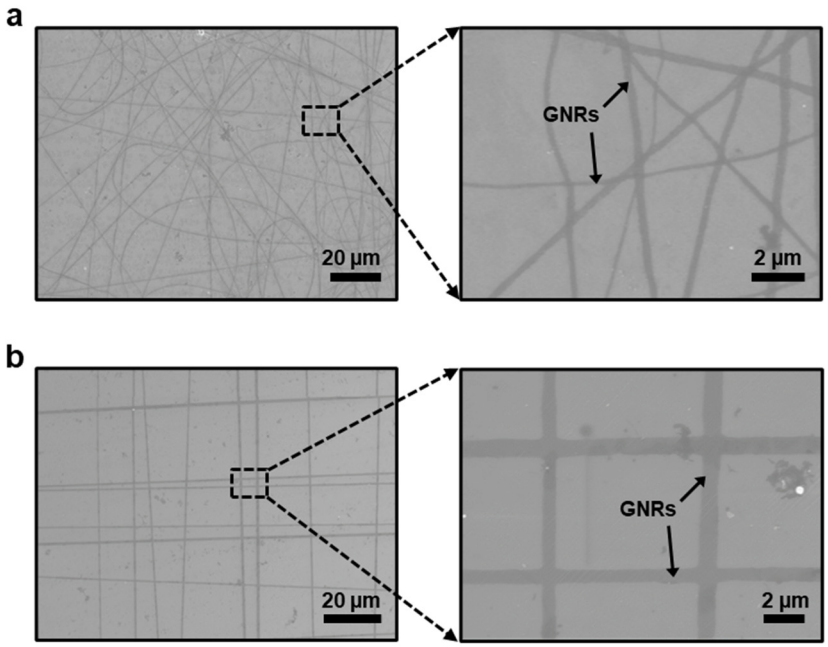

Figure S2. a-b) SEM images of the random networks and orthogonally crossed GNR arrays on a SiO_2/Si substrate after O_2 plasma and the removal of p-NWs; the enlarged SEM images (right) represent randomly oriented and aligned GNR structures in the form of the interconnected configurations.

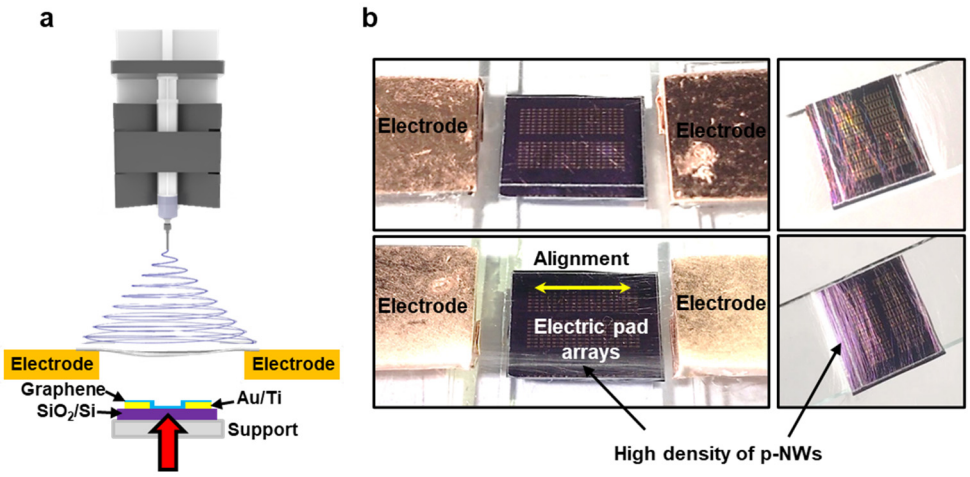

Figure S3. a) Schematic illustration of the electrospinning process on the processing substrate with electric pads (i.e., source/drain) to integrate GNR-array based FETs; a slide glass was used as a support in the transfer printing process of the highly aligned p-NWs. b) The real images in the process of density control as a function of electrospinning time; the processing substrate was placed between the Cu electrodes (i.e., bridged collector).

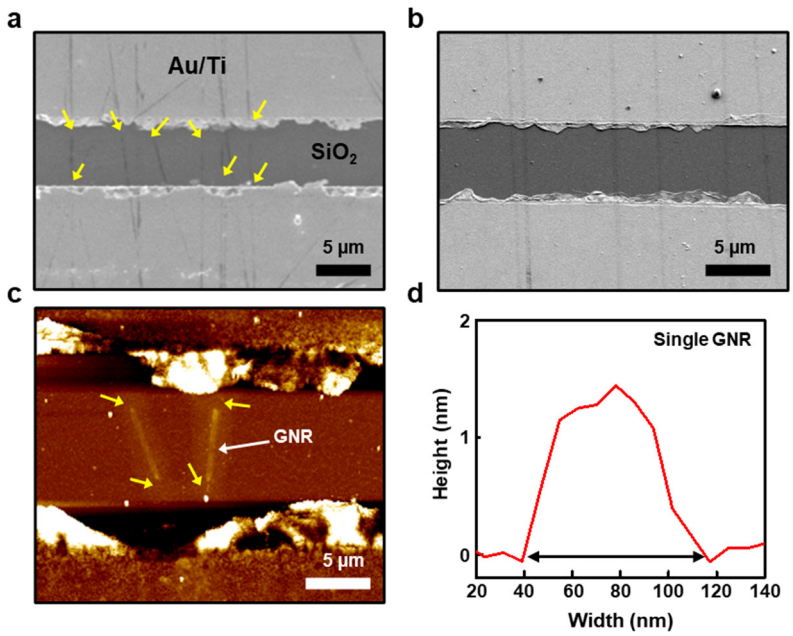

Figure S4. Annealing effect on the enhanced step coverage of GNRs in the active channel formation. a) SEM image of the disconnected GNRs (see yellow arrows) between the source-drain electrodes without annealing process. b) Conformally formed GNRs with electrically connected configuration between the source-drain electrodes with the annealing process. c) AFM image measured from the sample in a); GNRs were electrically isolated away from the electrodes. d) AFM height profile measured from the sample in b); the width of single GNR was ~82 nm in this case.

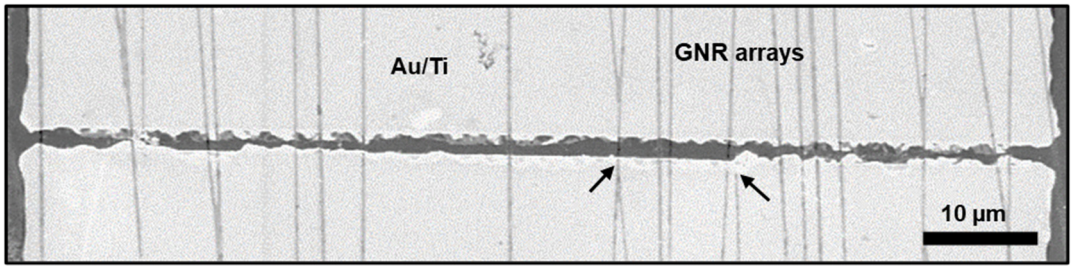

Figure S5. Highly aligned arrays of GNRs between the source-drain electrodes; most of the GNRs was uniformly connected in the conductive channel, except some misaligned and disconnected on the electric pads (see marked arrows).

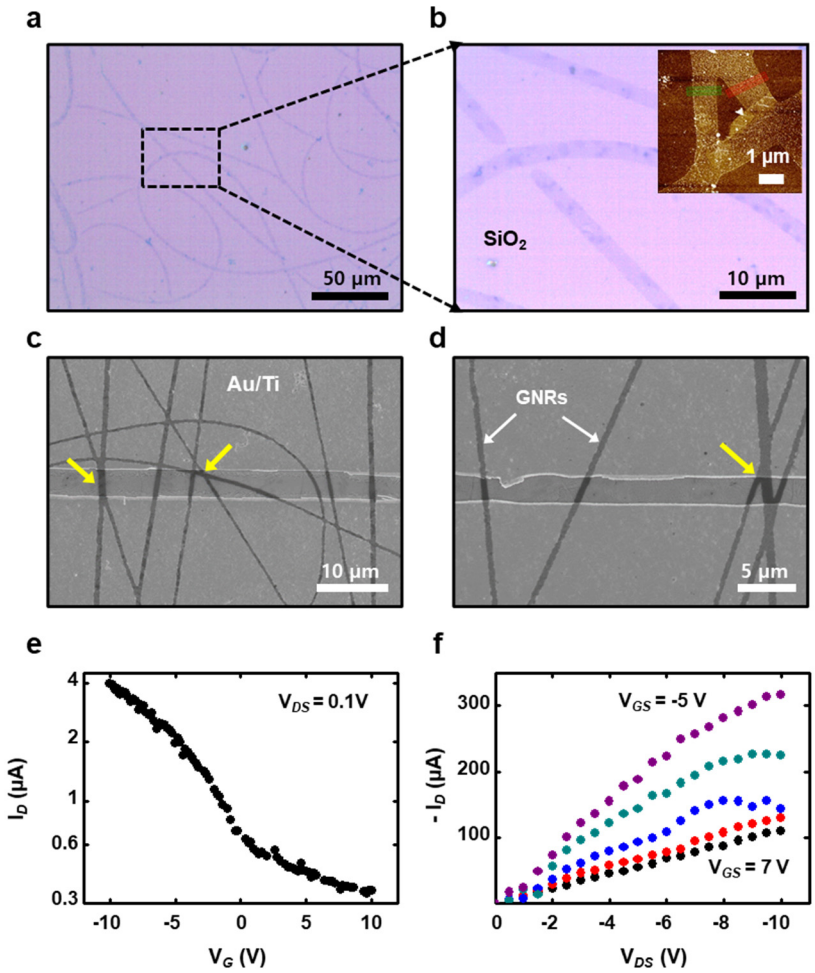

Figure S6. a-b) Optical micrographs of the random network arrays of GNRs formed on a SiO2/Si substrate; the inset shows a representative AFM image measured from the surface, in which micron ribbons were appeared with unaligned configuration. c-d) SEM images of partially aligned and unaligned arrays of GNRs between the source-drain electrodes; the yellow arrows indicate more widen GNRs, resulted from the overlapped etch-mask of the p-NWs. e-f) Typical I_D-V_G curve from the FET built with random networks of GNRs, and the corresponding output characteristics, respectively.

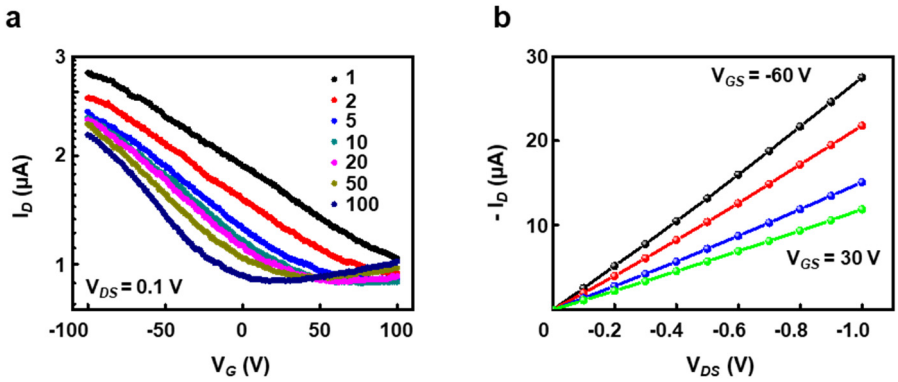

Figure S7. Electric filed annealing effect on the GNR-FET. a) I_D-V_G curve of GNR device after high-power electrical annealing sweeps (i.e., 100 times), which shows slightly asymmetric hole and electron conduction. b) I_D-V_{DS} curve of the same device with 30 V steps of V_{GS}.

Table S1. Previously reported GNR-based transistors.

Graphene width	I_{ON}/I_{OFF}	Method	Ref.
10 nm	$>10^5$	Chemical synthesis	1
10 nm	3000	E-beam lithography	2
15 nm	12	Nanowire lithography	3
~5 nm	270	Nanowire lithography	4
~40 nm	56	DNA nanowire array lithography	5
~10 nm	10	E-beam lithography	6

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