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High-Performance Top-Gate Thin-Film Transistor with an Ultra-Thin Channel Layer

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Abstract: Metal-oxide thin-film transistors (TFTs) have been implanted for a display panel, but further mobility improvement is required for future applications. In this study, excellent performance was observed for top-gate coplanar binary SnO_2 TFTs, with a high field-effect mobility (μ_{FE}) of 136 cm^2/Vs, a large on-current/off-current (I_{ON}/I_{OFF}) of 1.5×10^8, and steep subthreshold slopes of 108 mV/dec. Here, μ_{FE} represents the maximum among the top-gate TFTs made on an amorphous SiO_2 substrate, with a maximum process temperature of ≤ 400 °C. In contrast to a bottom-gate device, a top-gate device is the standard structure for monolithic integrated circuits (ICs). Such a superb device integrity was achieved by using an ultra-thin SnO_2 channel layer of 4.5 nm and an HfO_2 gate dielectric with a 3 nm SiO_2 interfacial layer between the SnO_2 and HfO_2. The inserted SiO_2 layer is crucial for decreasing the charged defect scattering in the HfO_2 and HfO_2/SnO_2 interfaces to increase the mobility. Such high μ_{FE}, large I_{ON}, and low I_{OFF} top-gate SnO_2 devices with a coplanar structure are important for display, dynamic random-access memory, and monolithic three-dimensional ICs.

Keywords: thin-film transistor; SnO_2; TFT; integrated circuit; monolithic; 3D IC; brain-mimic

1. Introduction

The development of high-performance transistors has been continuously pursued for more than seven decades, since the transistor was invented in 1947. The metal-oxide thin-film transistor (TFT) was invented in 1964 [1], and had the important merits of low-temperature fabrication, a simple process for mass production, and visible light transparency [1–26]. Moreover, metal-oxide TFTs have widely diverse applications, such as in active matrix organic light emitting diodes [2,3], flexible electronics [4–7], and gas sensors [8–10]. By applying a high-mobility channel material and high-dielectric-constant (high-κ) gate dielectric, metal-oxide TFT can also be used in high-speed low-power monolithic three-dimensional (3D) integrated circuits (ICs) [11–16]. Furthermore, the wide energy bandgap, excellent field-effect mobility (μ_{FE}) at high temperatures, and low leakage current of metal-oxide TFTs are especially important for high-temperature electronics [17] and dynamic random-access memory (DRAM) access transistors. In this paper, we report a top-gate SnO_2 TFT that uses a combined HfO_2 and SiO_2 stack as a gate dielectric layer and an SnO_2 channel layer. The top-gate TFT structure is more favorable than the bottom-gate device, owing to its high performance and easy integration in forming an IC. This top-gate device, with an SiO_2 interfacial layer between HfO_2 and SnO_2, exhibited an excellent device performance, with a remarkably high μ_{FE} of 136 cm^2/Vs, a large on-/off-current (I_{ON}/I_{OFF}) of 1.5×10^8, a sharp subthreshold slope (SS) of 108 mV/dec, and a much better resistance

to moisture than the bottom-gate SnO_2 TFT. Here, the SiO_2 interfacial layer with a thickness of 3 nm is the key factor in decreasing the charged defect scattering inside HfO_2 and increasing the μ_{FE}. Such high-performance TFTs are crucial for future-generation high-resolution displays, DRAM access transistors, high interconnect-density monolithic 3D ICs, and 3D brain-mimicking ICs [11–13], where the down-scaling of silicon ICs is expected to be ended at an equivalent node around 1 nm within ten years.

2. Materials and Methods

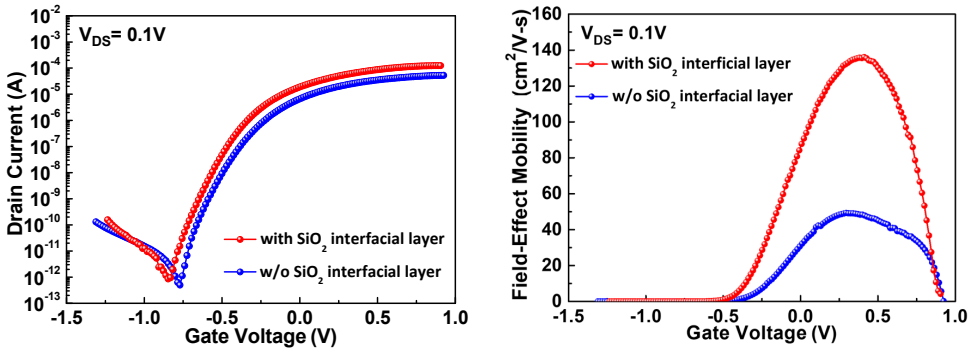
P-type silicon wafers with ~10 ohmic-cm resistivity were used as substrates. A standard IC cleaning process was applied to remove the particles and native oxide from the silicon substrate. Then, an SiO_2 layer with a thickness of 300 nm was formed on the substrate, and was used as an inter-metal-dielectric layer of the IC. Thereafter, a 4.5 nm SnO_2 layer was deposited through reactive sputtering with a Sn target under a pressure of 7.6×10^{-3} torr, a mixture of O_2/Ar gas flow at 20/24 sccm, and a DC power of 50 W. The deposited SnO_2 layer was subjected to post-annealing at 350 °C in ambient air for 30 min. Next, 30 nm low work function aluminum Schottky source and drain electrodes [27,28] were deposited and patterned. Subsequently, a 3 nm SiO_2 layer and a 50 nm high-κ HfO_2 gate dielectric were deposited on the SnO_2 layer through physical vapor deposition. Finally, a 30 nm Ni top-gate electrode was created using electron-beam evaporation and patterning. The gate length and width are 50 and 400 μm, respectively. Material analyses through X-ray photoelectron spectroscopy (XPS), secondary ion mass spectrometry (SIMS), and high-resolution transmission electron microscopy (TEM) were performed using Thermo Nexsa (Thermo Fisher Scientific Inc., Waltham, MA, USA), CAMECA IMS-6fE7 (CAMECA, Gennevilliers, France), and FEI Talos F200X (FEI company, Hillsboro, OR, USA), respectively. The electrical characterization of the device was measured using the HP4155B semiconductor parameter analyzer (HP, Englewood, CO, USA) and a probe station.

3. Results and Discussion

Figure 1a presents the drain-source current versus gate-source voltage (I_{DS}-V_{GS}) characteristics of the top-gate TFTs with and without the SiO_2 interfacial layer between the SnO_2 channel and the HfO_2 gate dielectric. The devices, with and without the ultra-thin SiO_2, exhibit good I_{ON}/I_{OFF}s of 1.5×10^8 and 1×10^8, respectively, and sharp turn-on SS values of 108 and 117 mV/dec, respectively. The interface trap density (D_{it}) can be calculated from SS [29,30]:

$$D_{it} = \frac{1}{q}\left(\frac{SS}{kT/q \times ln10} - 1\right)C_{ox} - \frac{C_{dep}}{q}, \quad (1)$$

where C_{dep} is the depletion capacitance. A D_{it} of 5.5×10^{12} $eV^{-1}cm^{-2}$ is obtained, which is higher than the high-κ/silicon transistor. Further interface improvement can increase the SS and μ_{FE}.



(**a**) (**b**)

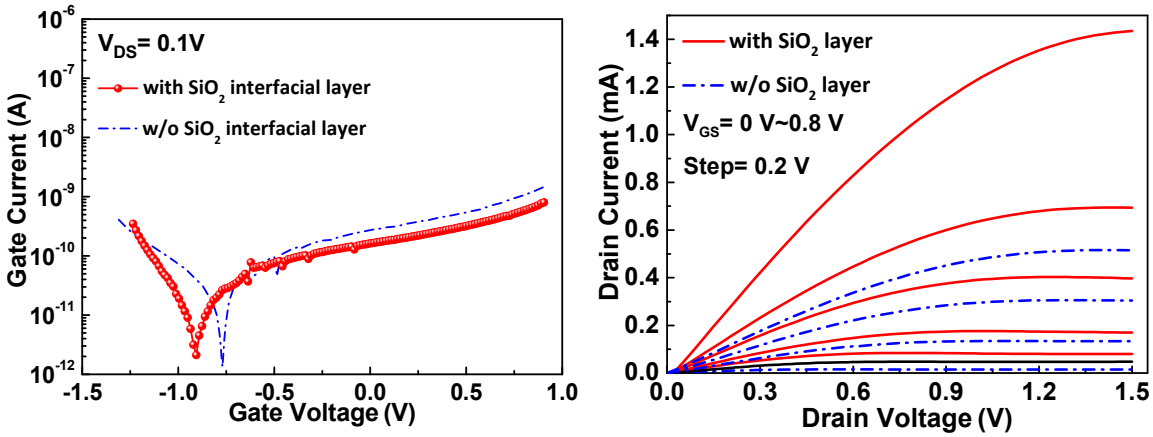
Figure 1. (**a**) I_{DS}-V_{GS} and (**b**) μ_{FE}-V_{GS} characteristics of the top-gate SnO_2 TFTs with and without an SiO_2 interfacial layer.

Figure 1b depicts the μ_{FE}-V_{GS} characteristics of these devices. The μ_{FE} was obtained by a standard method used in silicon IC from the trans-conductance (g_m) at a small V_{DS} of 0.1 V:

$$\mu_{FE} = \frac{g_m}{(W_G/L_G)C_{ox}V_{DS}}, \quad (2)$$

where W_G, L_G, and C_{ox} are the gate width, gate length, and oxide capacitance, respectively. The C_{ox} was obtained from the measured *C*-*V* characteristics divided by the area of the Ni/HfO_2/SiO_2/Al MIM device on the same chip. The SnO_2 TFT with an SiO_2 interfacial layer has a μ_{FE} as high as 136 cm^2/Vs, which is significantly higher than the 49.3 cm^2/Vs for the device without the SiO_2 layer. This is the highest μ_{FE} value for top-gate TFTs made on an amorphous SiO_2 substrate and processed at a temperature of ≤400 °C [21–25].

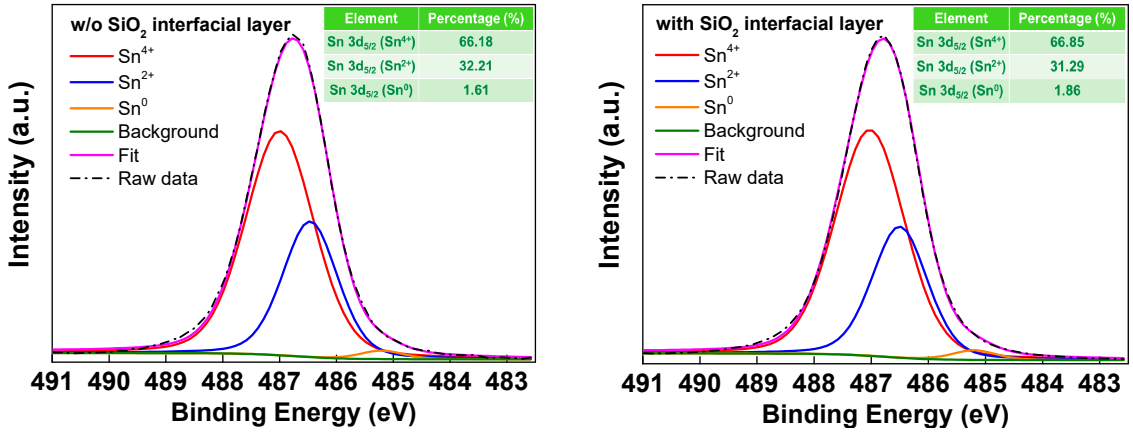
To understand the significantly better the I_{DS} and μ_{FE} data for TFTs with an ultra-thin SiO_2 layer, we further measured the gate-source current versus gate-source voltage (I_{GS}-V_{GS}) characteristics. As shown in Figure 2a, the gate leakage current does not demonstrate a significant difference between these two devices because the interfacial SiO_2 layer was only 3 nm thick, and much thinner than the high-κ HfO_2, which had a thickness of 50 nm. The I_{DS} versus the drain-source voltage (I_{DS}-V_{DS}) characteristics are presented in Figure 2b. The TFT device with the ultra-thin SiO_2 layer exhibits a higher I_{DS} than the TFT without it, which is consistent with the I_{DS}-V_{GS} and μ_{FE}-V_{GS} data presented in Figure 1a,b, because the higher I_{DS} leads to a higher μ_{FE} value.



(**a**) (**b**)

Figure 2. (**a**) I_{GS}-V_{GS} and (**b**) I_{DS}-V_{DS} characteristics of the top-gate SnO_2 with and without an SiO_2 interfacial layer.

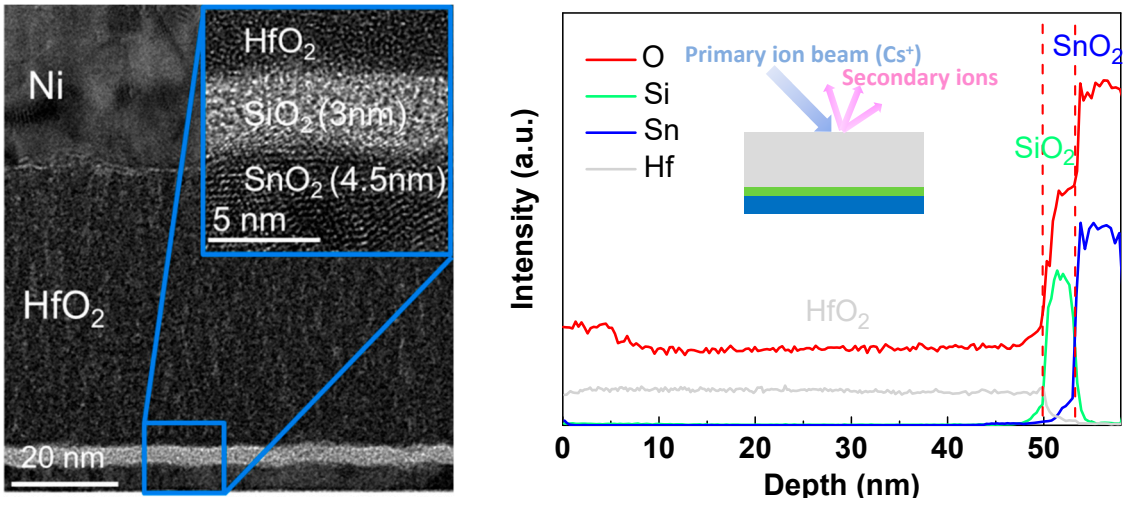
An XPS analysis was performed on both the HfO_2/SiO_2/SnO_2 and the HfO_2/SnO_2 stacks. Before the analysis, both samples were sputter-etched from HfO_2 to SnO_2 at a slow rate of 0.1 nm/s. As shown in Figure 3, the Sn $3d_{5/2}$ spectrum of the SnO_x layer is split into three peaks: Sn^{4+}, Sn^{2+}, and Sn^0. The binding energies of the Sn^{4+}, Sn^{2+}, and Sn^0 peaks were 487, 486.5, and 485.2 eV, respectively. The intensity of Sn^{2+} is related to the p-type SnO TFT [18]. By contrast, Sn^{4+} conducts electrons for n-type TFTs [11–16]. As the results obtained using XPS analysis do not indicate obvious differences between these two samples, the inserted SiO_2 interfacial layer has little effect on the chemical composition of the SnO_x channel layer.



(**a**) (**b**)

Figure 3. The XPS spectra of Sn $3d_{5/2}$ in the SnO_2 layer of the TFT devices (**a**) without and (**b**) with an SiO_2 interfacial layer.

We further investigated the $HfO_2/SiO_2/SnO_2$ stack through TEM and SIMS measurements. Figure 4a displays the cross-sectional TEM image of the SnO_2 TFT with an SiO_2 interfacial layer, where the thicknesses of HfO_2, SiO_2, and SnO_2 were 50, 3, and 4.5 nm, respectively. The distributions of the Sn, Si, Hf, and O atoms in the gate stack and channel layer are depicted from the SIMS depth profiles in Figure 4b. An SiO_2 interfacial layer was clearly observed in both the TEM and SIMS analyses.



(**a**) (**b**)

Figure 4. (**a**) The cross-sectional TEM image and (**b**) SIMS depth profiles of the SnO_2 TFT with an SiO_2 interfacial layer.

It is important to note that the extra SiO_2 interfacial layer will increase the thickness of the gate dielectric slightly and theoretically lead to a slightly higher transistor threshold voltage (V_{TH}) than the device without the SiO_2 layer. However, the I_{DS}-V_{GS} characteristics of the SnO_2 devices in Figure 1a display a contrary result. Thus, the increased V_{TH} for the device without the interfacial SiO_2 layer is due to the extra negative charges formed in HfO_2. These negative charges may also exist in the HfO_2/SnO_2 interface because the interface charges are strongly related to *SS* [22], which improves with the extra SiO_2 interfacial layer, as shown in Figure 1a. Further, such negative charges in the HfO_2 and HfO_2/SnO_2 interfaces can cause electron scattering and degrade the mobility [31,32], as shown in Figure 1b. It is known that the high-κ gate dielectric has defects, especially when formed at low

temperatures. The negative charges formed in the HfO_2 and HfO_2/SnO_2 interfaces cause channel electron scattering and mobility degradation, which can be observed in the schematic diagrams illustrated in Figure 5a,b. The device with the SiO_2 interfacial layer has less negative charge scattering in HfO_2 and the interface because of the separation of the SiO_2 layer, which results in a higher mobility and I_{DS}.

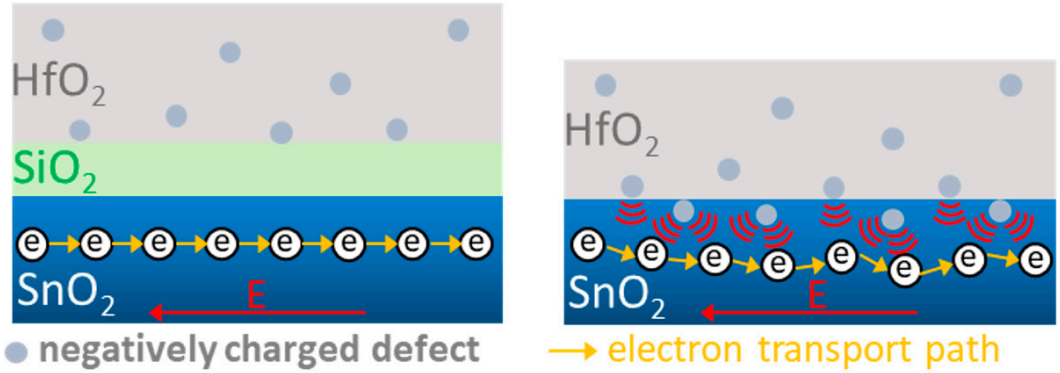


Figure 5. The schematic diagrams for electron transport in (**a**) with (**b**) without an SiO_2 interfacial layer. Negative charges formed in HfO_2 for a device without an SiO_2 layer will increase the electron scattering and lower the mobility.

The moisture degradation of TFT devices is a significant issue for an IC. Figure 6 illustrates the I_{DS}-V_{GS} characteristics for the as-fabricated top-gate coplanar and bottom-gate staggered SnO_2 TFTs in ambient air after 7 days and 30 days of exposure to air. The I_{DS}-V_{GS} characteristics of the bottom-gate SnO_2 TFT are shifted as high as 1.5 V after 7 days of exposure, and the I_{OFF}, SS, and I_{ON} further degrade significantly after 30 days of exposure to air. This is because the top SnO_2 layer can react with H_2O molecules in the air and form Sn-OH bonds [14,19,20], resulting in charged defects that lower the I_{DS} and μ_{FE}. The penetration of OH^- into the SnO_2 could also form defects and lead to a higher I_{OFF} by defect conduction [26]. In sharp contrast, only a slight V_{TH} shift of −0.09 V was observed in the top-gate device because the gate dielectric HfO_2 layer can behave as a passivation layer on the SnO_2 channel layer. The slight V_{TH} shift might be attributed to the intrinsic defects of the HfO_2 layer and the charge trapping and de-trapping phenomena of those defects [33,34].

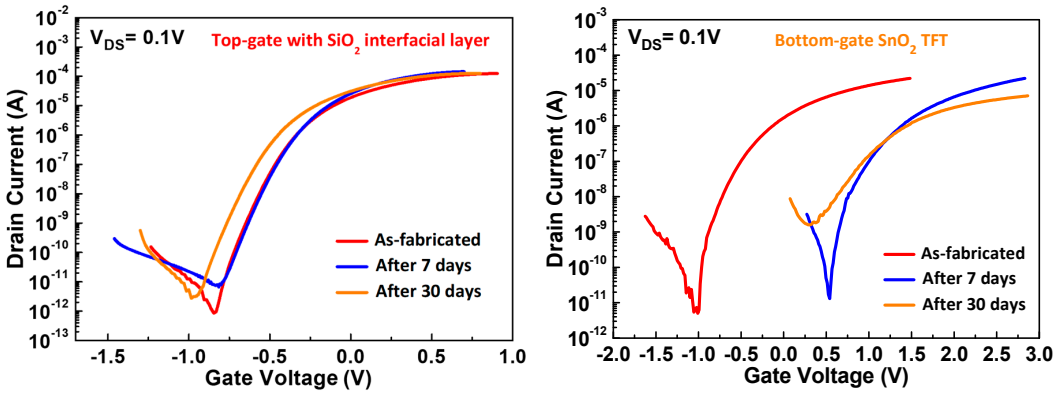


Figure 6. The I_{DS}-V_{GS} characteristics of the (**a**) top-gate and (**b**) bottom-gate SnO_2 TFT devices measured as-fabricated after 7 days and after 30 days of exposure to ambient air.

In Table 1, we summarize the important device characteristics and compare them with the published data on top-gate TFTs made on amorphous SiO_2 substrates [21–25]. Our device with an ultra-thin channel thickness of 4.5 nm exhibits the highest μ_{FE}, a sharp *SS* for low-voltage operation, and a sufficiently large I_{ON}/I_{OFF}, which are crucial for display, low-leakage DRAM access transistors, and monolithic 3D IC applications. Further improvement of μ_{FE} and *SS* may be reachable by using a thicker SnO_2 layer than the 4.5 nm thickness and a Fin Field-Effect Transistor (FinFET) or gate-all-around structure, respectively.

Table 1. Important device performance comparison of various top-gate TFT devices on SiO_2 substrate.

Channel Materials	Channel Thickness (nm)	μ_{FE} ($cm^2/V{\cdot}s$) @V_{DS}(V)	I_{ON}/I_{OFF}	SS (mV/Decade)
a-Si [21]	100	0.9 @ 0.1	10^5	380
Poly-Si [22]	100	40 @ 0.1	1.5×10^6	310
IGZO [23]	40	11.44 @ 10	10^8	360
ZnO [24]	50	16.8 @ 0.1	2.4×10^9	102
SnO_2 [25]	30	4.43 @ 1	4.19×10^6	300
SnO_2 this work	4.5	136 @ 0.1	1.5×10^8	108

4. Conclusions

An excellent device integrity was achieved for a top-gate TFT made on an amorphous SiO_2 substrate using a low process temperature of 350 °C with a high μ_{FE} of 136 cm^2/Vs, a sharp SS of 108 mV/dec for low-voltage operations, and a sufficiently large I_{ON}/I_{OFF} of 1.5×10^8. Such a top-gate structure is preferred for monolithic IC as compared to bottom-gate devices. In addition, a much better resistance to moisture can be achieved than in the bottom-gate device without passivation. Such a superb device performance is strongly related to the inserted ultra-thin SiO_2 layer between the HfO_2 and SnO_2. The outstanding device performance with top-gate structure is a crucial technology for future-generation high-resolution displays, low-leakage DRAM access transistors, and monolithic 3D brain-mimicking ICs.

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Conflicts of Interest: The authors declare no conflict of interest.

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