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An Implementation of Parallel Buck Converters for Common Load Sharing in DC Microgrid

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Abstract: The increase in demand for clean, safe, and environmentally friendly renewable energy sources faces several challenges such as system design and reliable operations. DC microgrid (MG) is a promising system due to higher efficiency and natural interface to renewable sources. In the hierarchical control of DC Microgrid, the V-I droop control is deployed usually in primary control level for common load sharing between converters. However, conventional droop control causes improper current sharing, voltage variations, and circulating current regulation due to the presence of droop and line resistance between converters. The aim of this paper is to presents the primary control level design of buck converters in current mode control according to the concepts of time constant and time delay, and secondary control design for parallel operations in distributed manners by combining methods, namely, low bandwidth communication (LBC), circulating current minimization techniques, and average voltage/current control. Moreover, different time delays are used for two converters to testify the effects of communication delays on current sharing and voltage restoration. The simulation is done for 2×2.5 KWdc parallel buck converters in PLECS (a Simulation software used for high speed simulation for power electronics) environment which shows excellent results in minimizing circulation currents, enhancing proportional current sharing, and restoring the grid voltage.

Keywords: DC Microgrid; Distributed Secondary control; low bandwidth communication; V-I droop control; buck converter

1. Introduction

The blackouts, usual shutdown of centralized grids, CO₂ emission, damage to the Ozone layer, dependency on biomass fuel and its increasing price, global warming, etc. brought the concept of a safe, renewable, environmental friendly, clean and green energy source to the fore. In the last decade, the use of renewable energies such as photovoltaic, wind, tidal, etc. has increased dramatically due to a lot of advantages such as low dependency on biomass, decrease in CO₂ emission, fuel prices, and unusual shutdown of centralized grids. The concept of these green energies also brought the idea of a Microgrid (MG) which is unique, diverse, controllable, interactive, as well as independent.

A Microgrid is the parallel interconnection of different distributed energy sources such as photovoltaic arrays, wind turbines, Micro CHP (Combined heat and power), diesel generators etc.; different loads, a control and communication system for energy sharing within the MG or other grids; as well as an Energy storage system (ESS) and Electric vehicle (EV) station. The concept of the Microgrid was presented by CERTS of USA in their whitepaper which further provides the information

of Distributed energy resources (DERs) within a Microgrid [1]. A microgrid is an essential system for a future Smart grid [2]. Big brand companies such as SMA Solar Tech. of USA and Fronius GMBH provide AC microgrid solutions with DERs. The devices used by these manufacturers are, namely, a Cluster controller and data logger for control and communication of multiple DERs or Microgrid. However, these devices act as central controllers which could possibly be a single point of failure. Recently, a new trend in Microgrids for energy trading and sharing is introduced, called peer to peer (P2P) energy trading which is based on DERs. A small scale DERs owner using P2P technology can become a prosumer of energy as P2P trading allows prosumers to sell or purchase electricity directly from their neighbors which means this technology can provide bidirectional energy exchange within a microgrid. A good explanation of P2P energy trading is proposed and discussed in [3,4].

A lot of research has been conducted on MGs' architecture, control, and communication and still many things are needed to develop truly distributed and independent MGs with several distributed DERs. Microgrids are basically of two types according to the nature of electric current, namely AC MG and DC MG, respectively. A hierarchical control of droop controlled AC and DC Microgrids consisting of primary, secondary, and tertiary level control is proposed in [5], and because the nature of electronic interfaces are DC and generation of DC power by most renewable sources, DC MG is considered better than AC MG as the DC system does not associate with problems such as harmonic current, injection current from the transformer, reactive power flow etc. However, ESS and super capacitors are naturally DC sources, and conversion power efficiency from AC to DC decreased by at least 5%. Eneko et al. [6] compared and analyzed autonomous primary control strategies in AC and DC microgrids using the virtual synchronous machine (VSM) technique for ACMG and a virtual impedance based algorithm for DC MG, respectively. Moreover, DC MG also does not need synchronization as well as AC–DC–AC power conversion as required in AC MG [6].

A detailed discussion about architecture, design, communication networks, AC interfaces grounding schemes, challenges, and standardization aspects for DC MG is presented in [7] and a DC MG diagram is shown in Figure 1.

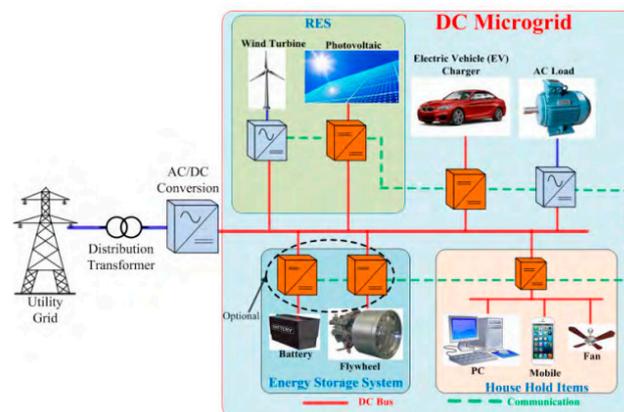


Figure 1. Distributed energy resources (DERs) connected in a DC Microgrid (MG) [7].

Manoj et al. [8] provided a literature overview of DC MG control and operation which explains that the main causes of power disturbance in DC MG are power variations between ESS and DERs, sudden load changes, and exchange of power between other grids and the DC MG, respectively. The DC bus voltage variation control is needed in a protective scheme suggesting hierarchical control in case of large number of DC MGs. Authors in [9,10] presented a detailed overview of hierarchical control where primary control is lower level control and is responsible for direct control of local voltage and the current of the converter; secondary is on top of primary which is responsible for power regulation; and tertiary is the top level management control which controls energy balance of ESS, energy sharing to other grids, and overall system regulations. Droop index based adaptive droop controller is proposed for load sharing in [11,12]. Using input-to-state theory, a non-linear current limiting droop

controller is proposed in [13] by limiting the inductor's current when the output power demand exceeds the converter's capacity. Communication based logical switch in distributed secondary control is presented in [14]. An average voltage and current are utilized in distributed secondary control using low bandwidth communication (LBC) as presented in [15]. A hybrid dynamic controller is proposed [16] in distributed secondary control via discrete time interaction. Daniel et al. [17] presented a centralized secondary control in parallel operation of buck converters. Energy storage system, vehicle to grid (V2G) control, tertiary or management level control, and entire energy management in DC Microgrids are well presented in [18–23].

This paper presents a combined way to design distributed secondary controllers for buck converters in DC Microgrid using low bandwidth communication, average voltage, and controllers for maximizing current sharing and circulation current minimization theory. Section 2 discusses the modeling for the buck converter, issues in parallel connecting converters for load sharing and primary control. Section 3 provides the detail of the distributed secondary control. Sections 4 and 5 analyzes the details of simulation results in PLECS, and conclusion, respectively.

2. Modeling and Paralleling of the Buck Converters

2.1. Buck Converters

A buck converter is the basic switch mode non-isolated step down converter which converts a high voltage DC to low output DC voltage. Figure 2 shows the practical power conversion PLECS model of the Buck converter where

- V_g = the source voltage
- V_o = the output voltage
- S_w = the switch (IGBT)
- I_g = Input Current
- I_L = Inductor's current
- I_o = Output current
- D = the diode
- L = inductor
- C = Capacitor
- DCR = Inductor's resistance
- ESR = Equivalent series resistance

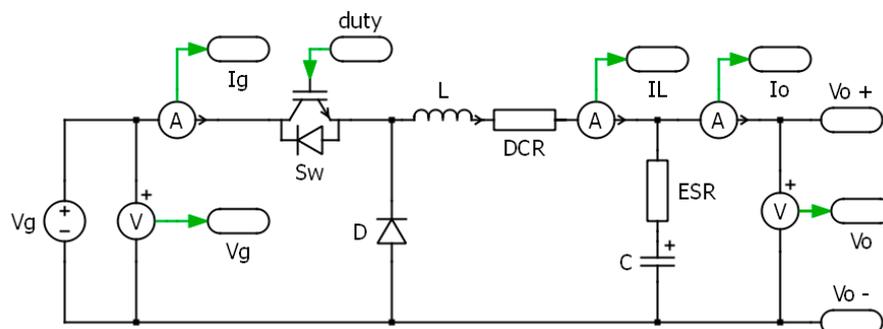


Figure 2. Power Conversion stage of Buck converter modeled in PLECS.

In the continuous conduction mode (CCM), the switching frequency is $f_s = 1/T_s$, where $T_s = T_{ON} + T_{OFF}$ is sampling time. T_{ON} is the time when the switch is closed or ON while T_{OFF} is the time when switch is open or off. The duty cycle of Buck converter is given by

$$k = V_o/V_g = T_{ON}/T_s \quad (1)$$

The values of inductor and capacitor can be found using the following equations:

$$L = (V_g - V_o)k/2\Delta i_L f_S \tag{2}$$

$$C = \Delta i_L/8\Delta V_0 f_S \tag{3}$$

where Δi_L and ΔV_0 represent desired peak ripple of inductor current and output voltage, respectively. Table 1 shows Buck converter parameter given in [17].

Table 1. Buck converter parameters and values.

Parameters	Values
Input voltage V_g	100 V
Output voltage V_o	48 V
Switching frequency f_S	10 kHz
Converter capacity	2.5 kW
Inductor L	0.479 mH
Capacitor C	271.25 μ F
ESR	0.03 Ω
DCR	0.002 Ω
Percentage peak to peak ripple inductor current $2\Delta i_L$	10%
Percentage peak ripple output voltage ΔV_0	0.5%

2.2. Small Signal Modeling of Open Loop Buck Converters

A small signal equivalent model of open loop Buck converter (s-domain) is shown in Figure 3, which is essential to find the transfer functions for closed loop operation. In order to work on the practical model and considering the converter’s internal losses cause by inductor and capacitor internal resistances (DCR and ESR), we have considered an internal resistance $r_{eq} = DCR + ESR$ as shown in Figure 3. This consideration can simplify the equation such as $v_C(s)$ becomes $v_o(s)$ as well as this assumption avoids working on 3rd order transfer function in s-domain [24].

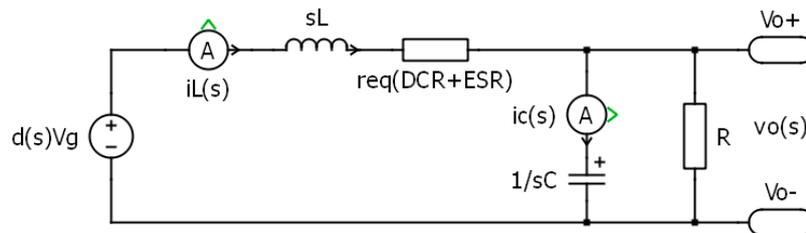


Figure 3. A small signal equivalent open loop Buck converter.

Based on Kirchoff’s voltage and current laws, we can get following equations from Figure 3:

$$C = \Delta i_L/8\Delta V_0 f_S \tag{4}$$

$$sCv_o(s) = i_L(s) - v_o(s)/R \tag{5}$$

where $i_L(s)$, $v_o(s)$, and $d(s)$ are small ac perturbations in values of inductor current $I_L(s)$, output voltage V_o , and duty cycle k , respectively.

In order to work on CCM, the transfer function from duty cycle to output voltage is necessary in voltage mode control and vital for describing the voltage loop in current mode control [25]. In current mode control, we assume the perturbation in input voltage is negligible.

The transfer function from duty cycle to output voltage is given by

$$G_{vod} = \frac{v_o(s)}{d(s)} = \frac{(V_o\eta/M)}{\tau\tau_d s^2 + \tau s + 1} \tag{6}$$

The transfer function from duty cycle to inductor current is necessary in current control mode to find out the effect of change in duty cycle on inductor current. The transfer function from duty cycle to inductor current is given by

$$G_{iLd} = \frac{i_L(s)}{d(s)} = \frac{\left(V_o \eta \frac{C}{M}\right) \left(s + \left(\frac{1}{\tau_d}\right)\right)}{\tau \tau_d s^2 + \tau s + 1} \tag{7}$$

where $M = \eta \frac{V_o}{V_g} = \eta k$ represents the voltage conversion ratio for Buck converter with energy losses and η is the efficiency for buck converter. τ and τ_d are the time constant and damping time constant, respectively. Theories of these time constants are well explained by Dr. Luo and Dr. Yeinin Digital Power Electronics and application [26]. For converters with internal power loss, time constant is given by

$$\tau = 2T \frac{EF}{1 + CIR} \left(1 + CIR \frac{1 - \eta}{\eta}\right) \tag{8}$$

$$\tau_d = 2T \frac{EF}{1 + CIR} \left(CIR \frac{1}{\eta + CIR(1 - \eta)}\right) \tag{9}$$

In (8) and (9), EF is the energy factor and CIR is the capacitor-inductor ratio given by (10) and (11), respectively.

$$EF = \frac{SE}{PE} = \frac{\sum_{j=1}^m W_{Lj} + \sum_{j=1}^n W_{Cj}}{V_g I_g T} \tag{10}$$

$$CIR = \frac{\sum_{j=1}^n W_{Cj}}{\sum_{j=1}^m W_{Lj}} \tag{11}$$

where SE and PE are the storage and pumping energy, m and n represents number of inductors and capacitors in the circuit, W_L and W_C are stored energy in j th inductor and capacitor, and I_g is the input current to the system according to digital power electronics, respectively.

Transfer function for outer voltage loop in current control mode is necessary which is used to obtain the effect of inductor current on output voltage and is given by (12).

$$G_{v_o i_L} = \frac{G_{v_o d}}{G_{i_L d}} = \frac{\frac{1}{C}}{s + \frac{1}{\tau_d}} \tag{12}$$

2.3. Issues in Parallel Connected Converters

Figure 4 shows two converters are connected in parallel and sharing a common load R . Let us suppose V_{o1} and V_{o2} are output voltages of converter No. 1 and converter No. 2. Similarly, I_{o1} and I_{o2} are output currents of converter No. 1 and converter No. 2, respectively. I_L and V_L are the load current and voltage, R_{Line1} and R_{Line2} are line resistances of converter No. 1 and 2 to load, respectively. Applying KVL, we get following equations:

$$V_{o1} = I_{o1} R_{Line1} + I_L R \tag{13}$$

$$V_{o2} = I_{o2} R_{Line2} + I_L R \tag{14}$$

According to [26], the output voltage equations of the open-loop buck converters with internal energy losses are given by

$$V_{o1} = M_1 \frac{V_{g1}}{\eta_1} \tag{15}$$

$$V_{o2} = M_2 \frac{V_{g2}}{\eta_2} \tag{16}$$

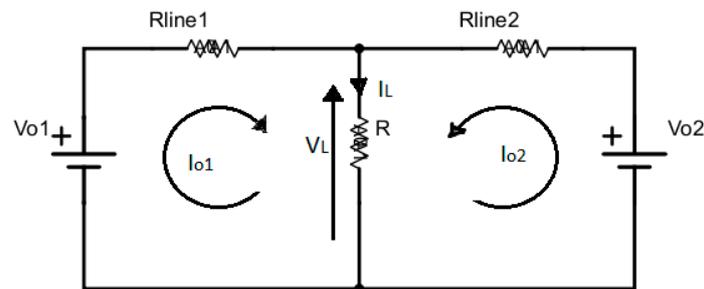


Figure 4. Parallel connected converters sharing a common load.

Droop resistor is normally used in primary level control of converters for current sharing and avoiding voltage deviation. Considering reference voltage source V_{ref} , as mentioned in [15], (15) and (16) become

$$V_{ref} = V_{o1} + I_{o1}R_{d1} \tag{17}$$

$$V_{ref} = V_{o2} + I_{o2}R_{d2} \tag{18}$$

where R_{d1} and R_{d2} are the droop resistances of converter No. 1 and 2, respectively.

All the above Equations (13)–(18) clearly show that the output voltage of converters must be influenced by the line resistances, droop resistors, as well as the efficiency of converter. Similarly, whenever there is a change in load or output power of parallel converters, it generates circulating currents from one converter to another which eventually affects the output voltage. The equation for circulating current considering Figure 4 is given by

$$I_{cir1} = -I_{cir2} = \frac{V_{o1} - V_{o2}}{R_1 + R_2} \tag{19}$$

3. Primary and Secondary Control Design in Current Control Mode

3.1. Primary Control Design

Figure 5 shows the block diagram of primary control of the Buck converter in current control mode. The control system consists of two loops, namely, an inner and outer loop. Both loops are designed using PI controllers, i.e., Current and voltage PI controllers. In order to make the design stable, the inner current controller should be faster as compared to the outer voltage controller. Transfer functions from the duty cycle to the inductor current (7) and from the inductor current to output voltage (12) are used in the inner current control loop and the outer voltage control loop, respectively, and the transfer function of the pulse width modulator (PWM) block is given by

$$G_{PWM} = \frac{1}{V_M} \tag{20}$$

where V_M is the peak-to-peak amplitude of the triangular waveform and is used by the PWM block in comparison to the control voltage $V_C(s)$. The transfer functions for both voltage and current PI (Proportional–Integral) controllers are given by

$$G_{PI}(s) = K_P + \frac{K_I}{s} = K_P \left(1 + \frac{1}{sT_i} \right) \tag{21}$$

where K_P , K_I are the proportional and integral gains, respectively. $T_i = \frac{K_P}{K_I}$ is a constant.

The current PI controller gains, i.e., K_P and K_I can be found using the Cohein-Hrones-Reswick (CHR) method for PID tuning, which is a modification of the Ziegler-Nichols method. The CHR method uses the time constant to dead time constant ratio, i.e., $R = T_p/\tau_{dd}$ of the plant explicitly. The CHR tuning formula for set point regulation with 0% overshoot is given in Table 2 [27], where “ K ” is the steady state level of the voltage waveform. The voltage PI controller gains can be found by transforming the

equations $I_{ref}(s)$ and $i_L(s)$ into time domain using inverse Laplace transformation and then equating both equations.

$$I_{ref}(s) = [V_{ref}(s) - V_0(s)] \left[K_P + \frac{K_I}{s} \right] \tag{22}$$

$$i_L(s) = \frac{\left(V_o \eta \frac{C}{M} \right) \left(s + \left(\frac{1}{\tau_d} \right) \right)}{\tau \tau_d s^2 + \tau s + 1} \left(\frac{D}{s} \right) \tag{23}$$

Table 2. With 0% overshoot Cohein-Hrones-Reswick (CHR) formula for Proportional-Integral (PI) tuning [27].

Parameters	Formulae
R	$R = T_p / \tau_{dd}; 7.5 < R < 10$
K	$\frac{0.35 R}{K_I}$
T_i	$1.2 T_p$

The above equations after transforming into time domain would be in the form given by (24) and (25), respectively.

$$i_{ref}(t) = a_1 + e^{-\sigma t} (b_1 \cos \omega t + c_1 \sin \omega t) \tag{24}$$

$$i_L(t) = a_2 + e^{-\sigma t} (b_2 \cos \omega t + c_2 \sin \omega t) \tag{25}$$

a_{1-2} , b_{1-2} , and c_{1-2} are the residue of partial fraction. σ and ω represents damping factor and frequency, respectively. The transfer function in (6) and (7) are 2nd order functions with couple of conjugated poles located at the left hand side in s-domain. The values of σ and ω can be found using (26) and (27), respectively.

$$\sigma = 1/2\tau_d \tag{26}$$

$$\omega = \frac{\sqrt{\tau \tau_d - \tau^2}}{2\tau \tau_d} \tag{27}$$

3.2. Secondary Control Design

Secondary control is used on the top of primary control in distributed system. It controls the power regulation, power quality, and coordination in connecting or disconnecting to and from the main grid. It is necessary in a DC Microgrid to maintain the grid level voltage in each single distributed system as well as minimizing the circulating currents. The secondary controller must take rapid action if there is any disturbance within system level such as change in load resistance. Therefore, the proposed secondary control design mainly focuses on the average voltage and proportional current controller [15], and additionally the circulating current minimizing technique.

Figure 5a shows the external view of proposed secondary controller in PLECS, where V_{o1} and I_{o1} are the local voltage and current parameters, respectively. V_{o2} and I_{o2} are the voltage and current of nth converter, respectively. The local secondary controller obtains V_{o2} and I_{o2} through a low bandwidth communication channel with the time delay transfer of $G_{td} = \frac{1}{1+\tau_{td}s}$ as proposed in [15], where τ_{ds} represents communication delay. VMG in Figure 5a represents the Microgrid’s reference voltage. Figure 5b,c shows the design of average voltage and average proportional current controller where $K1$ and $K2$ are the proportion used in current sharing for converter 1 and converter 2, respectively, which is given by $\frac{i_{o1}}{i_{o2}} = \frac{K1}{K2}$, where, i_{o1} and i_{o2} are the output currents of converter 1 and converter 2, respectively.

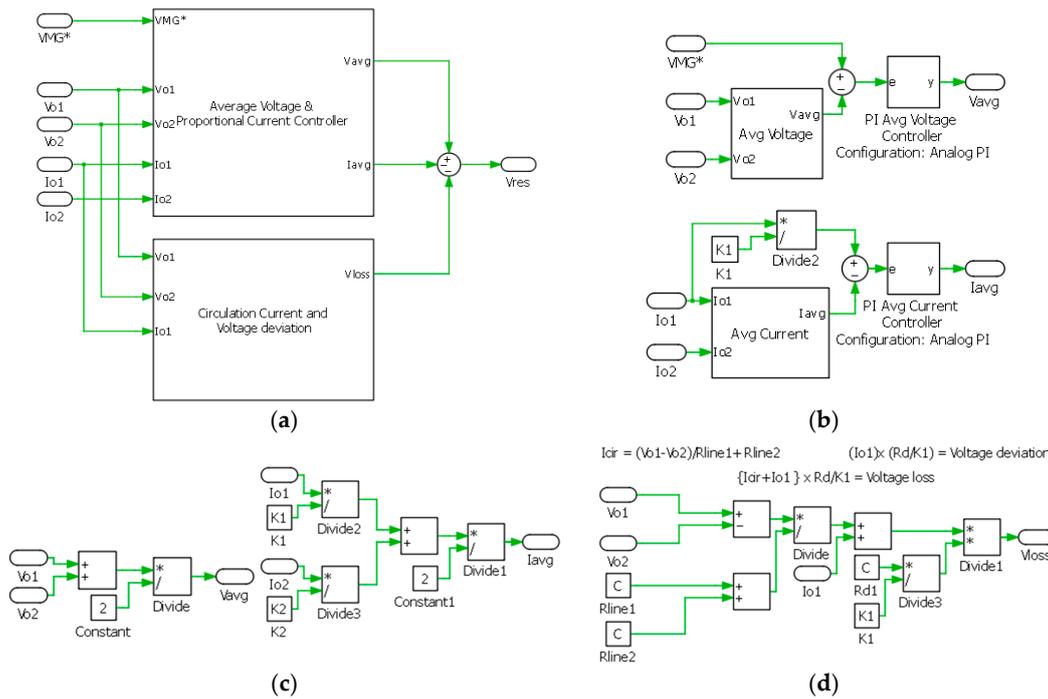


Figure 5. The Secondary controller design: (a) The proposed Secondary controller, (b) The average voltage and average proportional current controller, (c) Internal view of average voltage and average proportional current controller, (d) The circulating current and voltage deviation controller.

Drop resistance or controller is normally adopted in primary level control for energy sharing. Unlike conventional or other secondary controllers presented in the literature, the fixed droop resistance $R_{droop} = \frac{\epsilon_V}{I_0}$ (ϵ_V is maximum output voltage deviation and I_0 is maximum output current) is added with circulating current minimizing loop in the proposed secondary control shown in Figure 5d, where R_{line1} and R_{line2} represent line resistances of converter 1 and converter 2, respectively. Hence, a combined average voltage, proportional current and circulating current minimizing control with fixed droop resistance using low bandwidth communication in secondary control is proposed in this research. The proposed secondary controller provides voltage restoration “Vres” (Figure 5a) which eventually controls the local primary controller.

4. The Simulation Results and Discussion

Figure 6 shows the complete simulation of a parallel Buck converter modeled in PLECS. Normally, the line resistance is much lesser than the droop resistance. However, the line resistances are still considered in this research. Different scenarios such as proportional current sharing, different line resistances, and change in common load resistance and different communication delays have been apprehended in this simulation. The controller design and simulation parameters of each converter are shown in Table 3.

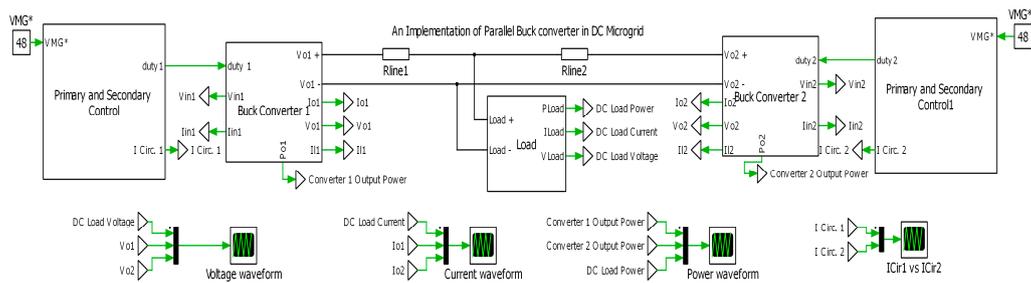


Figure 6. Complete simulation model of parallel Buck converters in DC Microgrid in PLECS.

4.1. Scenario 1

Scenario 1 is considered as the best case scenario in this simulation where equal current sharing $K1 = K2$, equal line resistances $R_{line1} = R_{line2} = 0.001 \Omega$ and, no communication delay $\tau_{ds} = 0$ are considered. Initially, the load resistance was 0.4608Ω , however, at $t = 0.99$ s the load was changed to 0.9216Ω , and again changed to 0.4608Ω at $t = 1.48$ s. Figure 7a shows the output voltages of each converter and load. It took about 0.064 s to restore the voltage to 48 V during each step change in load resistance. Current waveforms are shown in Figure 7b and the reaction times during step changes are found to be about $t = 0.06$ s. It is worth mentioning that current sharing is equal after the reaction time. Similarly, the power waveforms are shown in Figure 7c and circulating currents are shown in Figure 7d. The circulating currents in each converter in scenario 1 are nearly zero except during step changes.

4.2. Scenario 2

In scenario 2, equal line resistances but unequal current sharing, i.e., $K1 = 1$ and $K2 = 2$, and communication delay of $\tau_{ds} = 5$ ms are introduced. Initially in this case, the load of 2.5 KW (0.9216Ω) was used and then changed to 2 KW (1.152Ω) at $t = 1.02$ s. In Figure 8a, it took $t = 0.03$ s to stabilize the grid voltage of 48 V as the LBC starts after $\tau_{ds} = 5$ ms and also during the step change in the load resistance. Figure 8b shows the proportional current sharing of each converter. Converter 2 provides twice the current of converter 1, i.e., $i_{o2} = 34.5$ A and $i_{o1} = 17.47$ A and, after the load change, converter 2 provides $i_{o2} = 27.64$ A and converter 1 shares $i_{o1} = 14.08$ A, respectively. Figure 8c shows the power waveform of scenario 2 where two loads of 2500 W and 2000 W are visible. The circulating current minimization is shown in Figure 8d. It is worth mentioning that after the communication delay of 5 ms and the load change at $t = 1.02$ s, the controller took almost 0.03 s and 0.05 s, respectively, to minimize the circulating currents.

4.3. Scenario 3

This scenario is considered as the worst case scenario of the simulation. Different line resistances $R_{line1} = 0.0001 \Omega$ and $R_{line2} = 0.00015 \Omega$, communication delays for two converters $\tau_{ds1} = 100$ ms and $\tau_{ds2} = 50$ ms, current proportion of $K1 = 1$ and $K2 = 3$ are considered, respectively. However, a fixed load of 0.9216Ω is used. Because of huge communication delays, different line resistances, and different current sharing proportions, the controllers took $t = 0.8$ s to stabilize the grid voltage to 48 V shown in Figure 9a. Similarly, the current, power, and circulating current waveforms are shown in Figure 9b,c,d, respectively. Conversely, the controllers still work and gain stability even after the large communication gap.

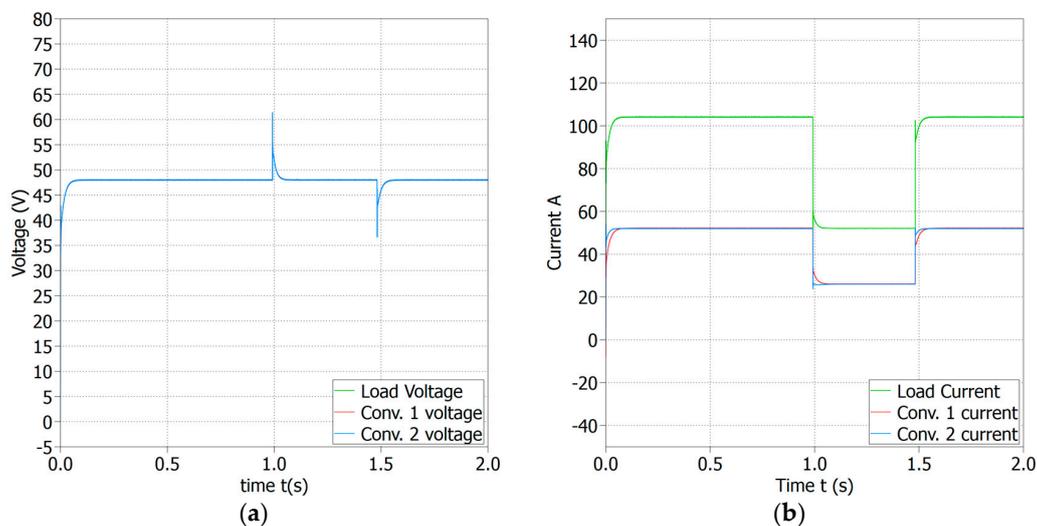


Figure 7. Cont.

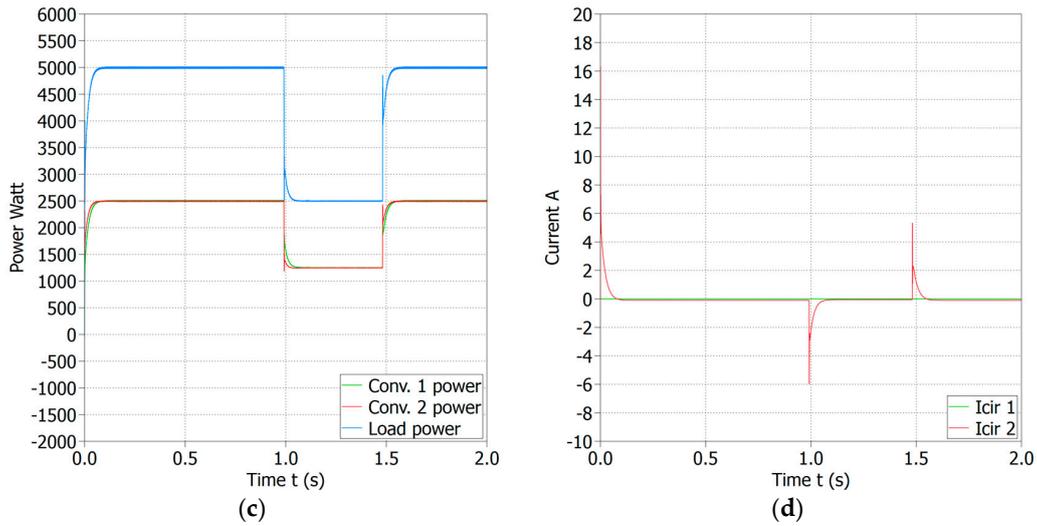


Figure 7. Scenario 1 outputs with load resistance of 0.4608Ω , $K1 = K2 = 1$, $R_{line1} = R_{line2} = 0.001 \Omega$, $\tau_{ds} = 0$, (a) Converters' output voltages and the load voltage, (b) Converters' output currents and the load current, (c) Converters' output power and the load power, (d) Circulating currents.

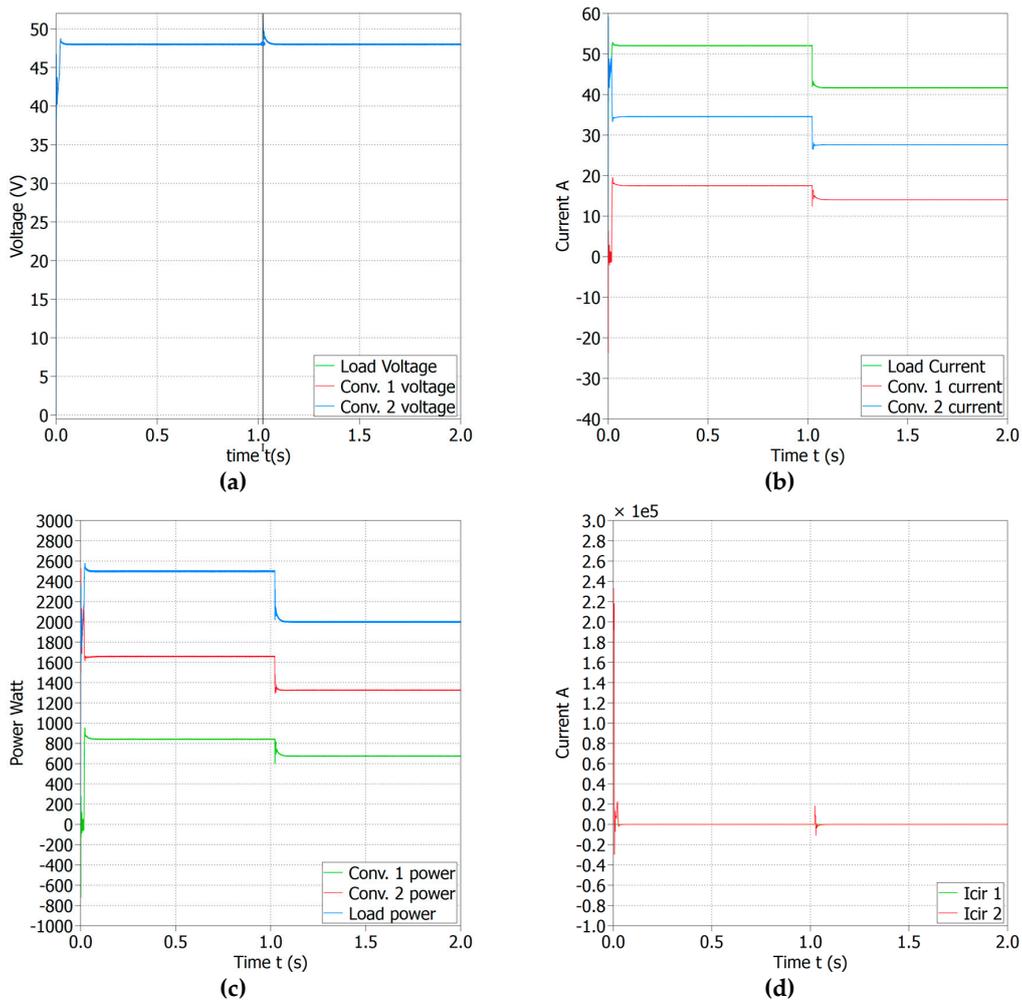


Figure 8. Scenario 2 outputs with load resistance of 0.9216Ω , $K1 = 1$ and $K2 = 2$, $R_{line1} = R_{line2} = 0.0001 \Omega$, $\tau_{ds} = 5 \text{ ms}$, (a) Converters' output voltages and the load voltage, (b) Converters' output currents and the load current, (c) Converters' output power and the load power, (d) Circulating currents.

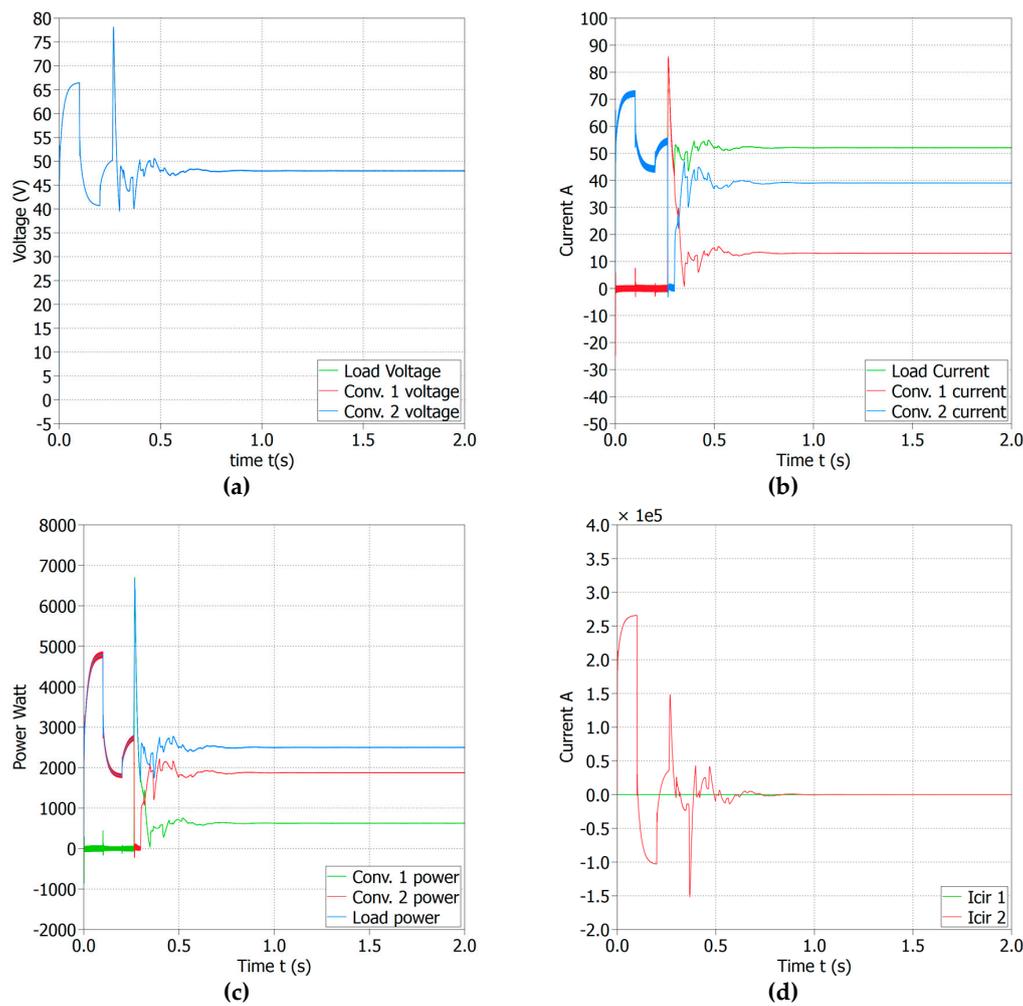


Figure 9. Scenario 3 outputs with load resistance of 0.9216Ω , $K1 = 1$ and $K2 = 3$, $R_{line1} = 0.0001 \Omega$, $R_{line2} = 0.00015 \Omega$, $\tau_{ds1} = 100 \text{ ms}$, $\tau_{ds2} = 50 \text{ ms}$. (a) Converters’ output voltages and the load voltage, (b) Converters’ output currents and the load current, (c) Converters’ output power and the load power, (d) Circulating currents.

Table 3. Controller design and simulation parameter.

Parameters	Values
Simulation Time t	2 s
Communication delay τ_{ds}	0~100 ms
Current proportion of converter 1 K1	1
Current proportion of converter 2 K2	1~4
Inner current controller Ki	0.993
Inner current controller Kp	790
Outer voltage controller Ki	0.077
Outer voltage controller Kp	5.7
Avg. voltage controller Ki of converter 1	0.05
Avg. voltage controller Kp of converter 1	50
Avg. current controller Ki of converter 1	90
Avg. current controller Kp of converter 1	0.002
Avg. voltage controller Ki of converter 2	58
Avg. voltage controller Kp of converter 2	0.009
Avg. current controller Ki of converter 2	0.9
Avg. current controller Kp of converter 2	0.01

5. Conclusions

In this paper, paralleling of buck converters is done. The theory of time constant and damping time constant is utilized in primary control design. A simply combined average voltage and proportional current sharing controller and a circulating current minimization technique with fixed droop resistance based on LBC in secondary control is proposed and implemented in PLECS software. The system is analyzed by different scenarios such as different line resistances between parallel converters, different time delays in communication for each converter, change in load, and proportional current sharing. A general guideline for implementing the proposed method and the results obtained from simulation is presented. The line resistances should be less than the droop resistance, i.e., $R_{line} \ll R_{droop}$, for proper operation. The tested system shows rapid response during the transient state in restoring the grid and output voltages of converters during a sudden change in load. The proposed system also shows stability in communication delays of each neighboring converter up to 100 ms and circulating current minimization. For best system operation, it is suggested to select scenario 1. However, the proposed system design guarantees fulfilling the worst case scenario as well.

In the future work, tertiary or management level control must be added and a large number of buck converters would be considered with practical implementation. Furthermore, tertiary control would not only guarantee the energy sharing to other grids but would also detect/disconnect abnormal connected distributed converters because of communication link failure or insufficient energy balance.

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