Article

Normally-Off p-GaN Gated AlGaIn/GaN MIS-HEMTs with ALD-Grown Al₂O₃/AlN Composite Gate Insulator

Hsien-Chin Chiu ^{1,2,*} , Chia-Hao Liu ¹, Chong-Rong Huang ¹, Chi-Chuan Chiu ¹, Hsiang-Chun Wang ¹, Hsuan-Ling Kao ¹ , Shinn-Yn Lin ^{2,3} and Feng-Tso Chien ⁴

¹ Department of Electronics Engineering, Chang Gung University, Taoyuan 333, Taiwan; r3287133@gmail.com (C.-H.L.); gain525252@gmail.com (C.-R.H.); wade03030333@gmail.com (C.-C.C.); smallflgt@hotmail.com (H.-C.W.); snoopy@mail.cgu.edu.tw (H.-L.K.)

² Department of Radiation Oncology, Chang Gung Memorial Hospital, Chang Gung University, Taoyuan 333, Taiwan; rt3126@gmail.com

³ Department of Medical Imaging and Radiological Sciences, College of Medicine, Chang Gung University, Taoyuan 333, Taiwan

⁴ Department of Electronics Engineering, Feng Chia University, Taichung 407, Taiwan; ftcchien@fcu.edu.tw

* Correspondence: hcchiu@mail.cgu.edu.tw; Tel.: +886-3-2118800-3350

Abstract: A metal–insulator–semiconductor p-type GaN gate high-electron-mobility transistor (MIS-HEMT) with an Al₂O₃/AlN gate insulator layer deposited through atomic layer deposition was investigated. A favorable interface was observed between the selected insulator, atomic layer deposition–grown AlN, and GaN. A conventional p-type enhancement-mode GaN device without an Al₂O₃/AlN layer, known as a Schottky gate (SG) p-GaN HEMT, was also fabricated for comparison. Because of the presence of the Al₂O₃/AlN layer, the gate leakage and threshold voltage of the MIS-HEMT improved more than those of the SG-HEMT did. Additionally, a high turn-on voltage was obtained. The MIS-HEMT was shown to be reliable with a long lifetime. Hence, growing a high-quality Al₂O₃/AlN layer in an HEMT can help realize a high-performance enhancement-mode transistor with high stability, a large gate swing region, and high reliability.

Keywords: p-GaN E-mode HEMT; normally-off; gate insulator; lifetime; reliability

Citation: Chiu, H.-C.; Liu, C.-H.; Huang, C.-R.; Chiu, C.-C.; Wang, H.-C.; Kao, H.-L.; Lin, S.-Y.; Chien, F.-T. Normally-Off p-GaN Gated AlGaIn/GaN MIS-HEMTs with ALD-Grown Al₂O₃/AlN Composite Gate Insulator. *Membranes* **2021**, *11*, 727. <https://doi.org/10.3390/membranes11100727>

Academic Editor:
Annarosa Gugliuzza

Received: 7 August 2021

Accepted: 18 September 2021

Published: 23 September 2021

Publisher's Note: MDPI stays neutral with regard to jurisdictional claims in published maps and institutional affiliations.

Copyright: © 2021 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (<https://creativecommons.org/licenses/by/4.0/>).

1. Introduction

High-electron-mobility transistors (HEMTs) are crucial for high-frequency and high-power applications because of their outstanding thermal properties, high breakdown fields, and high mobility levels. For fail-safe reasons, the power integrated circuits usually require high-performance normally-off devices [1]. Several strategies, such as the use of fluorine ion treatment [2], gate recess [3], and a p-type GaN cap layer [4,5], have been employed in normally-off HEMT devices. Normally-off devices fabricated with p-GaN gate technology offer low on-state resistance and large positive threshold voltage. However, to uniformly etch away the p-GaN in the non-gated access region and to overcome the plasma-induced damage during the p-GaN removal are extremely challenging tasks. Therefore, several teams are investigating the p-GaN etching process, such as etching stop technique [6], oxidation technique [7], and H plasma technique [8]. A positive threshold voltage can be obtained in HEMTs with p-type GaN layers, without affecting channel mobility; therefore, strategies involving the use of a p-type GaN layer are widely considered as the most effective among the strategies mentioned above. However, uniformly etching p-GaN away from the ungated access region and mitigating plasma-induced damage [9] during p-GaN removal are challenging. Cl₂-based ion etching is typically used to remove the p-GaN layer. If the etching is imprecise, the surface becomes rough with plasma bumps and in-surface defects, which may cause gate lag [10]. To control the etching depth, an AlN etch stop layer [6] is inserted between the p-GaN and barrier layers. This helps achieve highly

selective etching to obtain superior etching uniformity, lower gate leakage, and lower dynamic on-resistance. Usually, the low hole concentration of p-GaN limits the threshold voltage; when this occurs, the resulting product is unsatisfactory practical applications. Moreover, the p–n junction gate turns on at strong forward bias, leading to a considerably high gate leakage current. In this study, to minimize the defects that may arise after p-GaN etching and increase the gate swing region, we deposited Al_2O_3 and AlN layers [11] on the surface of the device through atomic layer deposition (ALD); these layers also improved the device performance, increased the turn-on voltage, reduced the gate leakage current, and increased the device stability at high temperatures.

2. Device Structure

The HEMT structures used for proposed devices were grown on 6-inch Si (111) substrates through metal–organic chemical vapor deposition (MOCVD). A 300-nm-thick undoped GaN channel was deposited on top of a 4- μm -thick undoped GaN buffer transition layer. Subsequently, a 12-nm-thick $\text{Al}_{0.17}\text{Ga}_{0.83}\text{N}$ layer, a 1-nm-thick AlN layer, and a 70-nm-thick p-type GaN top layer were deposited. The Al_2O_3 /AlN interlayer was deposited through ALD. A schematic representation of the device is shown in Figure 1a.

The device was thermally annealed in an MOCVD chamber at 720 °C for 10 min in a N_2 atmosphere. The activated Mg concentration was determined to be $1 \times 10^{18} / \text{cm}^3$ using the Hall measurement. The device was fabricated using mesa isolation with inductively coupled plasma (ICP) in the first step. Second, a p-GaN layer was etched through ICP etching with $\text{Cl}_2/\text{BCl}_3/\text{SF}_6$ as the etching gas. When the mixed gas reached the AlN layer, the SF_6 plasma [12] reacted with the Al atoms and formed a thin AlF_3 etch stop layer. Subsequently, the sample was soaked in a diluted $\text{HF}/\text{NH}_4\text{F}$ solution to remove AlF_3 . Then, a Ti/Al/Ni/Au (25/120/25/150 nm) ohmic metal stack was deposited through electron beam (e-gun) evaporation to serve as the source and drain; the metal stack was annealed at 875 °C for 30 s in a N_2 atmosphere in an RTA system, and the contact resistance of the MIS-HEMT and SG-HEMT were 7.6×10^{-6} and $8.1 \times 10^{-6} \Omega \cdot \text{cm}^2$, respectively. The oxide/insulator layer Al_2O_3 /AlN (9/2.5 nm) was deposited through ALD, as shown in Figure 1b. In addition, Trimethylaluminum, O_2 , and N_2 were used as metal precursors, O and N source, respectively. The RF power and chamber temperature were 60 W and 300 °C. Then, an ohmic via was etched using buffered oxide etching. Ti/Au (25/120 nm) layers were then deposited through e-gun evaporation to serve as gate electrodes. By contrast, the gate metal of the SG-HEMT was just a deposited Ti/Au (25/120 nm) layer.

Figure 2 shows the conduction bands of the MIS-HEMT and SG-HEMT, which were obtained through TCAD simulation. The aim of this study was to increase V_{TH} and the gate voltage swing of the device by using Al_2O_3 /AlN to increase the conduction band. The 2DEG height of the MIS-HEMT was more than that of the SG-HEMT, which resulted in the MIS-HEMT exhibiting better characteristics than the SG-HEMT.

Figure 1. (a) Schematic of the device structure with $L_{\text{GS}}/L_{\text{G}}/L_{\text{GD}}/W_{\text{G}} = 2/4/10/100 \mu\text{m}$. (b) transmission electron microscopy (TEM) photograph of the device.

Figure 2. Energy band diagrams of schottky-gated high electron mobility transistor (SG-HEMT) and metal–insulator–semiconductor-high electron mobility transistor (MIS-HEMT) obtained through TCAD simulation.

3. Experimental Result and Discussion

For examining the effect of the $\text{Al}_2\text{O}_3/\text{AlN}/\text{p-GaN}$ interface on device performance and for investigating the relationship of the AlN layer formed through ALD with an AlN etch stop layer at the sidewall and ungated region, we measured the I–V characteristics of the devices. Because an $\text{Al}_2\text{O}_3/\text{AlN}$ layer can fill the nitrogen vacancies on the surfaces of p-GaN and AlN, depositing an $\text{Al}_2\text{O}_3/\text{AlN}$ layer had the same effect as passivation. The I–V curve revealed that the gate leakage current was suppressed. Furthermore, because the polarization effect was enhanced due to the presence of the $\text{Al}_2\text{O}_3/\text{AlN}$ layer, the MIS-HEMT had a higher drain current density and on/off ratio than the SG-HEMT. The off-state drain currents of the MIS-HEMT and SG-HEMT were 6×10^{-6} and 2×10^{-4} mA/mm, respectively, at $V_{\text{GS}} = 0$ V and $V_{\text{DS}} = 10$ V, as shown in Figure 3a. The $I_{\text{DS}}-V_{\text{DS}}$ characteristics are shown in Figure 3b. The saturated drain currents of the MIS-gate and metal-gate devices were 363 and 247 mA/mm at $V_{\text{DS}} = 10$ V. Figure 3c shows the MIS-gate HEMT data. The figure indicates that the $\text{Al}_2\text{O}_3/\text{AlN}$ layer had a high gate voltage swing of more than 20 V [13]. To determine the device reliability, we measured off-state breakdown voltage; when measuring the off-state breakdown voltage, the device gate must be biased to 0 V to ensure that the device is in the off state. The results are plotted in Figure 3d. Because the $\text{Al}_2\text{O}_3/\text{AlN}$ layer exhibited an effect similar to passivation and minimized any damage that might have been caused by etching, the $\text{Al}_2\text{O}_3/\text{AlN}$ gate device had a higher off-state breakdown voltage of 656 V.

To analyze the higher off-state breakdown voltage of the MIS-HEMT, we simulated the electric field distributions of the MIS-HEMT and SG-HEMT using TCAD. Figure 4 shows the schematic cross-sections of the two devices. The electric field was always concentrated at the gate edge in the drain side, and the electric field distributions of both devices were simulated at $V_{\text{GS}} = 0$ V and $V_{\text{DS}} = 650$ V. A comparison of the two devices shows that the electric field of the MIS-HEMT was low at the gate edge owing to the electric field being dispersed by the insulator layer. Negative charges appeared at the interface between the insulator and AlGaIn owing to the negative polarization, which reduced the electric field near the gate edge at the drain side [14]. Consequently, MIS-HEMT had a higher off-state breakdown voltage due to the presence of the AlN/ Al_2O_3 stack.

Figure 3. (a) Log-scale I_D - V_{GS} transfer characteristics, (b) I_D - V_{DS} output characteristics, (c) I_{GS} - V_{GS} characteristics, and (d) off-state breakdown voltages of the MIS-HEMT and SG-HEMT.

Figure 4. Electric field distributions of the SG-HEMT and MIS-HEMT simulated using TCAD.

Typical C-V characteristics were measured at 500 kHz, as shown in Figure 5. As the gate bias increases above a certain voltage, the capacitance value starts increasing and satu-

rates. MIS-HEMT showed higher capacitance than SG-HEMT due to the $\text{Al}_2\text{O}_3/\text{AlN}$ stacking. Figure 6a shows the dynamic on-resistance to static on-resistance ratio ($R_{\text{Dynamic, on}}/R_{\text{Static, on}}$) at different quiescent gate voltages. There are two bias conditions that must be considered: pulse voltage ($V_{\text{GSP}}, V_{\text{DSP}}$) and quiescent voltage ($V_{\text{GSQ}}, V_{\text{DSQ}}$). During the measurement, when the pulse voltage switched to the quiescent voltage rapidly with a 2 μs pulse width and 200 μs period, the charge carriers were trapped by defects. The quiescent gate bias was swept from 0 to -15 V in increments of -5 V. As seen in the figure, the MIS-HEMT had a lower dynamic R_{on} than the SG-HEMT; the MIS-HEMT had a dynamic R_{on} of 1.18, whereas the SG-HEMT had a dynamic R_{on} of 2.13. Therefore, the MIS-HEMT had a lower surface trap density surface, which inhibited current collapse. In this study, forward TDDDB measurements were performed on the MIS-HEMT to assess the strength of the $\text{Al}_2\text{O}_3/\text{AlN}$ gate dielectric. Figure 6b shows the variation in gate current during the TDDDB experiments at three different gate voltages (14, 15, and 16 V). The gate current was initially low, owing to the accumulation of negative charges under the gate. Then, the gate leakage current became noisy owing to the formation of a percolation path. This was followed by a sudden increase in the gate leakage current owing to the hard breakdown of the gate dielectric [15]. A Weibull plot was drawn based on the time-to-breakdown distributions. The slope shows a tight distribution and less variability, as shown in Figure 6c. Moreover, lifetimes of 1% and 63.2% were investigated and are shown in Figure 6d. The gate leakage mechanisms at the measured gate bias region were determined to be 8.5 V at a failure rate of 63.2% and 6.1 V at a failure rate of 1%. Therefore, the MIS p-GaN can effectively suppress the trapping/detrapping behavior and then enhance the gate reliability. Figure 7 compares the $V_{\text{G_BD}}-I_{\text{G}}$ characteristics of the MIS-HEMT with that of other reported p-GaN gate HEMTs [5,16–22]. The MIS-HEMT fabricated in this study exhibited the highest $V_{\text{G_BD}}$ and lowest gate leakage current.

Figure 5. C–V characteristics of SG-HEMT and MIS-HEMT.

Figure 6. (a) Gate lag behavior and dynamic Ron, (b) TDDDB gate current with three different gate voltages, (c) Weibull plot of the time-to-breakdown distributions, and (d) lifetime prediction with failure rate of 63.2% and 1% of MIS-HEMT.

Figure 7. Comparison between the $V_{G,BD}$ - I_G characteristics of the proposed device and those of other devices [5,16–22].

4. Conclusions

A normally-off p-GaN HEMT with an Al₂O₃/AlN layer was investigated. The device exhibited excellent I–V characteristics. The turn-on voltage was higher than 20 V, with a threshold voltage of 3 V and a high saturation drain current of approximately 363 mA/mm. Moreover, the gate leakage current and instability were suppressed. The device off-state breakdown voltage in the MIS gate was increased because of the presence of the Al₂O₃/AlN layer deposited using ALD; this layer helped form an excellent interface between p-GaN and AlN. The lower trap density and trapping/detrapping effects were analyzed using pulse measurement. Overall, an Al₂O₃/AlN dielectric gate layer considerably improves the performance, reliability, and stability of HEMTs. Therefore, the as-developed design has a high potential for use in the manufacture of normally-off p-GaN gate HEMTs, which would allow them to be used in practical applications.

Author Contributions: Project administration, H.-C.C., C.-H.L., C.-R.H., C.-C.C., H.-C.W., H.-L.K.; Investigation, F.-T.C., S.-Y.L. All authors have read and agreed to the published version of the manuscript.

Funding: This research received no external funding.

Institutional Review Board Statement: Not Applicable.

Informed Consent Statement: Not Applicable.

Conflicts of Interest: The authors declare no conflict of interest.

References

- Saito, W.; Takada, Y.; Kuraguchi, M.; Tsuda, K.; Omura, I.; Ogura, T.; Ohashi, H. High breakdown voltage AlGaIn-GaN power-HEMT design and high current density switching behavior. *IEEE Trans. Electron Devices* **2003**, *50*, 2528–2531. [\[CrossRef\]](#)
- Cai, Y.; Zhou, Y.; Chen, K.J.; Lau, K.M. High-performance enhancement-mode AlGaIn/GaN HEMTs using fluoride-based plasma treatment. *IEEE Electron Device Lett.* **2005**, *26*, 435–437. [\[CrossRef\]](#)
- Palacios, T.; Suh, C.; Chakraborty, A.; Keller, S.; DenBaars, S.P.; Mishra, U.K. High-performance E-mode AlGaIn/GaN HEMTs. *IEEE Electron Device Lett.* **2006**, *27*, 428–430. [\[CrossRef\]](#)
- Hwang, I.; Oh, J.; Choi, H.S.; Kim, J.; Choi, H.; Kim, J.; Chong, S.; Shin, J.; Chung, U.I. Source-Connected p-GaN Gate HEMTs for Increased Threshold Voltage. *IEEE Electron Device Lett.* **2013**, *34*, 605–607. [\[CrossRef\]](#)
- Wu, T.-L.; Marcon, D.; You, S.; Posthuma, N.; Bakeroort, B.; Stoffels, S.; Van Hove, M.; Groeseneken, G.; Decoutere, S. Forward Bias Gate Breakdown Mechanism in Enhancement-Mode p-GaN Gate AlGaIn/GaN High-Electron Mobility Transistors. *IEEE Electron Device Lett.* **2015**, *36*, 1001–1003. [\[CrossRef\]](#)
- Chiu, H.-C.; Chang, Y.-S.; Li, B.-H.; Wang, H.-C.; Kao, H.-L.; Chien, F.-T.; Hu, C.-W.; Xuan, R. High Uniformity Normally-OFF p-GaN Gate HEMT Using Self-Terminated Digital Etching Technique. *IEEE Trans. Electron Devices* **2018**, *65*, 4820–4825. [\[CrossRef\]](#)
- Liu, X.; Chiu, H.-C.; Liu, C.-H.; Kao, H.-L.; Chiu, C.-W.; Wang, H.-C.; Ben, J.; He, W.; Huang, C.-R. Normally-off p-GaN Gated AlGaIn/GaN HEMTs Using Plasma Oxidation Technique in Access Region. *IEEE J. Electron Devices Soc.* **2020**, *8*, 229–234. [\[CrossRef\]](#)
- Hao, R.; Xu, N.; Yu, G.; Song, L.; Chen, F.; Zhao, J.; Deng, X.; Li, X.; Cheng, K.; Fu, K.; et al. Studies on fabrication and reliability of GaN high-resistivity- cap-layer HEMT. *IEEE Trans. Electron Devices* **2018**, *65*, 1314–1320. [\[CrossRef\]](#)
- Tajalli, A. Impact of sidewall etching on the dynamic performance of GaN-on-Si E-mode transistors. *Microelectron. Reliab.* **2018**, *88–90*, 572–576. [\[CrossRef\]](#)
- Hao, R.; Li, W.; Fu, K.; Yu, G.; Song, L.; Yuan, J.; Li, J.; Deng, X.; Zhang, X.; Zhou, Q.; et al. Breakdown Enhancement and Current Collapse Suppression by High-Resistivity GaN Cap Layer in Normally-Off AlGaIn/GaN HEMTs. *IEEE Electron Device Lett.* **2017**, *38*, 1567–1570. [\[CrossRef\]](#)
- Takhar, K. Al₂O₃ formed by post plasma oxidation of Al as a Gate dielectric for AlGaIn/GaN MIS-HEMTs. *Appl. Surf. Sci.* **2019**, *481*, 219–225. [\[CrossRef\]](#)
- Buttari, D.; Chini, A.; Chakraborty, A.; McCarthy, L.; Xing, H.; Palacios, T.; Shen, L.; Keller, S.; Mishra, U.K. Selective dry etching of GaN over AlGaIn in BCl₃/SF₆ mixtures. *Proc. IEEE Lester Eastman Conf. High Perform. Devices* **2004**, *14*, 756–761. [\[CrossRef\]](#)
- Pu, T.; Wang, X.; Huang, Q.; Zhang, T.; Li, X.; Li, L.; Ao, J.-P. Normally-Off AlGaIn/GaN Heterojunction Metal-Insulator-Semiconductor Field-Effect Transistors with Gate-First Process. *IEEE Electron Device Lett.* **2019**, *40*, 185–188. [\[CrossRef\]](#)
- Chen, K.J. AlN passivation by plasma-enhanced atomic layer deposition for GaN-based power switches and power amplifiers. *Semicond. Sci. Technol.* **2013**, *28*, 074015. [\[CrossRef\]](#)
- Degraeve, R. Degradation and breakdown in thin oxide layers: Mechanisms, models and reliability prediction. *Microelectron. Reliab.* **1999**, *39*, 1445–1460. [\[CrossRef\]](#)
- Ľapajna, M.; Hilt, O.; Bahat-Treidel, E.; Würfl, J.; Kuzmík, J. Gate Reliability Investigation in Normally-Off p-Type-GaN Cap/AlGaIn/GaN HEMTs Under Forward Bias Stress. *IEEE Electron Device Lett.* **2016**, *37*, 385–388. [\[CrossRef\]](#)

17. Tallarico, A.N. Perimeter driven transport in the p-GaN gate as a limiting factor for gate reliability. *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)* **2019**, 1–10. [[CrossRef](#)]
18. He, J.; Wei, J.; Yang, S.; Wang, Y.; Zhong, K.; Chen, K.J. Frequency- and Temperature-Dependent Gate Reliability of Schottky-Type p-GaN Gate HEMTs. *IEEE Trans. Electron Devices* **2019**, *66*, 3453–3458. [[CrossRef](#)]
19. Stockman, A.; Masin, F.; Meneghini, M.; Zanoni, E.; Meneghesso, G.; Bakeroot, B.; Moens, P. Gate Conduction Mechanisms and Lifetime Modeling of p-Gate AlGaIn/GaN High-Electron-Mobility Transistors. *IEEE Trans. Electron Devices* **2018**, *65*, 5365–5372. [[CrossRef](#)]
20. Wang, C.; Hua, M.; Yang, S.; Zhang, L.; Chen, K.J. E-mode p-n Junction/AlGaIn/GaN HEMTs with Enhanced Gate Reliability. In Proceedings of the 2020 32nd International Symposium on Power Semiconductor Devices and ICs (ISPSD), Vienna, Austria, 13–18 September 2020; pp. 14–17. [[CrossRef](#)]
21. Zhang, L.; Zheng, Z.; Yang, S.; Song, W.; He, J.; Chen, K.J. p-GaN Gate HEMT With Surface Reinforcement for Enhanced Gate Reliability. *IEEE Electron Device Lett.* **2021**, *42*, 22–25. [[CrossRef](#)]
22. Zhou, G.; Wan, Z.; Yang, G.; Jiang, Y.; Sokolovskij, R.; Yu, H.; Xia, G. Gate Leakage Suppression and Breakdown Voltage Enhancement in p-GaN HEMTs Using Metal/Graphene Gates. *IEEE Trans. Electron Devices* **2020**, *67*, 875–880. [[CrossRef](#)]