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A Comparative Study on the Effects of Passivation Methods on the Carrier Lifetime of RIE and MACE Silicon Micropillars

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Abstract: Silicon micropillars have been suggested as one of the techniques for improving the efficiency of devices. Fabrication of micropillars has been done in several ways—Metal Assisted Chemical Etching (MACE) and Reactive Ion Etching (RIE) being the most popular techniques. These techniques include etching through the surface which results in surface damage that affects the carrier lifetime. This paper presents a study that compares the carrier lifetime of micropillars fabricated using RIE and MACE methods. It also looks at increasing carrier lifetime by surface treatment using three main approaches: surface passivation by depositing Al_2O_3, surface passivation by depositing SiO_2/SiN, and surface passivation by etching using KOH and Hydrofluoric Nitric Acetic (HNA) solution. It was concluded that passivating with SiO_2 and SiN results in the highest carrier lifetime on the MACE and RIE pillars.

Keywords: silicon; micropillars; passivation; reactive ion etching; and metal assisted ion etching

1. Introduction

Micro and nanoscale structures have improved the performance of many electronic devices such as solar cells [1,2], light emitting diodes [3], detectors [4], and batteries [5]. Patterning the surface of planar silicon with micropillars results in broadband antireflection [6–8], enhanced light trapping [9,10] and high carrier collection efficiency by separating the path for light absorption and carrier collection using a core-shell p-n junction and increasing the junction area [11]. At the same time, the large junction area and surface area on the pillar arrays compared to traditional planar junction silicon solar cells makes it challenging to fabricate high performance devices due to an increase in surface defects. This makes the choice of the micropillar fabrication technique very critical since it has an impact on the quality of the surface of the pillars. Micropillars can be formed using a bottom-up approach such as the metal-catalyzed Vapor–Liquid–Solid (VLS) technique or using top-down approaches such as Metal Assisted Chemical Etching (MACE) and Reactive Ion Etching (RIE), which are the most commonly used [12,13].

Over the past few years, RIE has been used extensively for surface texturing of silicon, mainly due to its relative ease in controlling process parameters which means that good reliability and reproducibility can be obtained [14]. In the RIE process a silicon substrate is put in contact with a noble metal mask (gold or silver). The substrate is placed on a high frequency driven and dc-biased electrode [15]. After ignition of the plasma, a capacitive coupled electrode acquires a negative charge because the electron mobility is much greater than that of the ions. Glow-discharge plasma is used to generate the gas-phase etching environment, which consists of positive and negative ions, electrons, radicals, and neutrals from a feed gas (CF4). The material on the electrode is thus exposed to energetic bombardment by positive ions. At the same time chemical reactions between radicals and neutrals

and the material being etched (silicon) occur at the surface and produce either volatile species or their precursors. Also, positive ions are accelerated across the plasma sheath and remove material by sputtering. The combination of the chemical activity of reactive species and sputtering can result in much higher material erosion rates in the vertical than in the lateral direction which forms the sharp edges of the pillars [16].

MACE is a wet etching technique that produces high aspect ratio semiconductor micro- and nanostructures. This technique has been used in photonic, photovoltaic, and diffusion membrane applications [17]. To fabricate micro- or nano-features using this application, metal particles or films are deposited at the silicon surface prior to chemical etching to enhance silicon dissolution. This step can be done using different techniques such as sputtering, thermal evaporation, electrochemical deposition. or electroless deposition in HF solutions [18]. Wet etching of most semiconductors occurs isotropically. This usually results in the loss of lateral resolution defined by the used mask. One of the exceptions is the use of crystal dependent wet etch. For example, the etch rate of Si (111) in KOH solution can be over two orders of magnitude slower than Si (110); therefore a Si (110) surface can be etched to produce deep trenches with (111) sidewalls [18]. Both RIE and MACE etching methods result in surface damage that affects the carrier lifetimes.

Surface damage has been mitigated using various surface passivation methods that either etch away the damaged surface using material such as KOH or passivate the surface using material such as Al_2O_3 [19], SiO_2 [20], or SiN [21] to passivate dangling bonds. The effect of the above approaches varies in nature and the intent of this paper is to quantify the surface damage and investigate the best passivation method that provides the highest carrier lifetime. First the paper will present the details of the fabrication methods of the micropillars. The paper will then discuss the steps of the passivation methods and the measurements obtained. Finally the paper will present a discussion on the results.

2. Materials and Methods

Two silicon micropillar samples were studied. P-type Cz (100) wafers with resistivity of 5–10 Ω-cm were used for the experiments. The first was fabricated using RIE and the second using MACE. The procedure for fabricating RIE is as follows. P-type silicon wafer (11–22 μm) was used to fabricate the vertical silicon micropillars using dry etching. The microdisk arrays were patterned in LOR3A and Shipley S1805 photoresist using photolithography. After the pattern was developed, aluminum was deposited to a thickness of 100 nm and lifted off to leave aluminum microdisk arrays on the starting Si wafer. A highly doped n-type conformal shell for the crystalline p-n junction was formed using the spin-on doping (SOD) method. After spinning an n-type doping source (P509, Filmtronics, Inc.) on a dummy Si wafer, we position the device wafer containing the micropillars so that it faces the dummy wafer coated with doping source, and then anneal the pair of wafers at high temperature (900–950 °C) for 10 min in a 20% O_2 and 80% N_2 environment. The process of the MACE fabrication is as follows. Au was used as the etch catalyst because it has been known to produce a solid and smooth surface compared with other catalysts [22]. The mesh patterns were generated by soft lithography with a liftoff process. The MACE solution to produce solid micropillar was a mixture of concentrated HF, H_2O_2, and ethanol. The oxidizing agent generates free holes (h+) when catalyzed by the metal. The holes oxidize Si at the metal-Si interface and HF dissolves oxidized Si [23]. As a result the material directly underneath the metal is preferentially removed and the metal descends into the semiconductor.

Figure 1 represents the RIE micropillars with a diameter of 2.2 μm and a spacing of 1.75 μm. Figure 2 represents the MACE micropillars with diameter of 2.1 μm and spacing of 2 μm. All samples were rinsed with deionized water and dipped in an HF solution (45% for 5 min) before any surface treatment. Surface treatment with KOH was performed by rinsing the sample with deionized water and dipping the samples in a KOH solution with concentration of 45% for 30 s. Surface treatment for Hydrofluoric Nitric Acetic (HNA) solution was performed by rinsing the sample with deionized water and dipping the sample in 50% HNA solution for 5 s. The samples were passivated with Al_2O_3 by depositing 20 nm of the film using the atomic layer deposition approach and annealing the sample at 350 °C for 10 min. The Savannah ALD from Cambridge NanoTech was used to perform

the deposition [24]. The system is a thermal deposition system that uses surface adsorption of single mono-layers of reactive precursor gases to form single atomic monolayers. The samples were passivated with SiN by depositing 60 nm of SiN using the Plasma Enhanced Chemical Vapor Deposition (PECVD) technique. The composition of silicon nitride is Si_3N_4. Finally, a set of samples were treated with SiO_2 by depositing 100 nm of SiO_2 using the thermal oxidation technique.

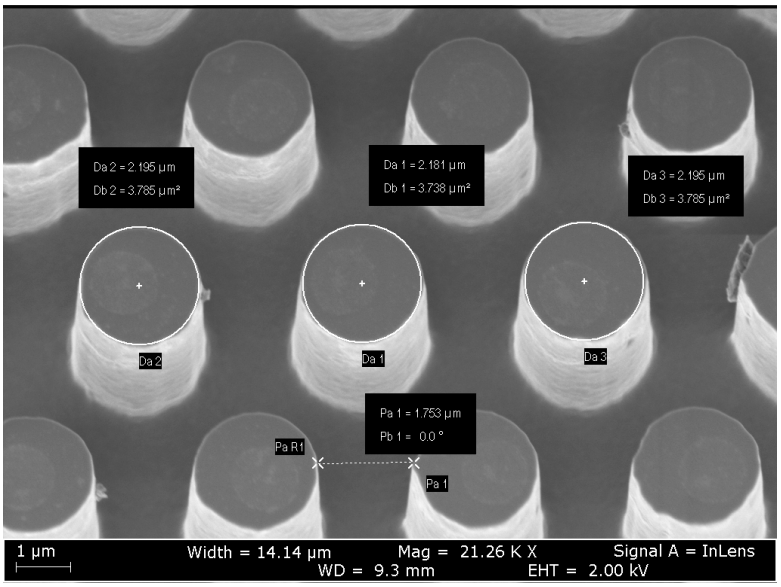


Figure 1. Silicon micropillars etched using the Reactive Ion Etching (RIE) method. The diameter of the pillars is 2.2 µm.

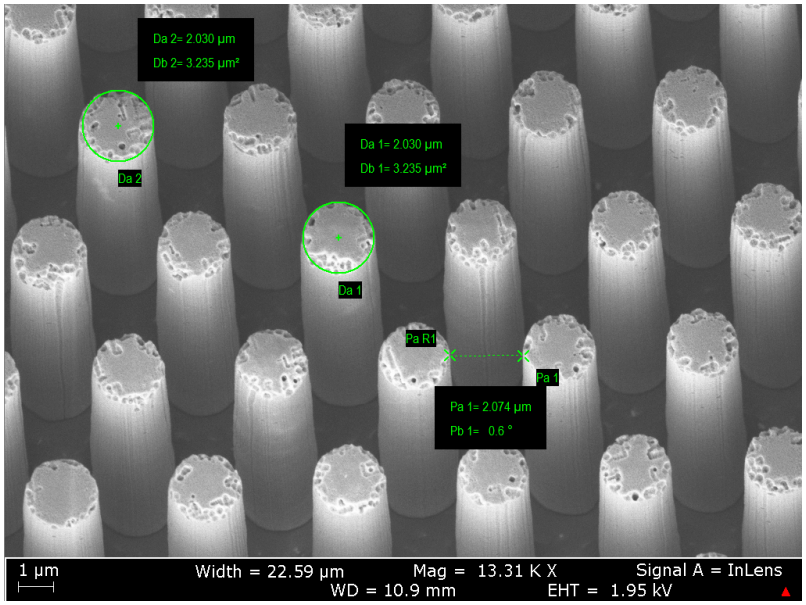


Figure 2. Silicon micropillars etched using the Metal Assisted Chemical Etching (MACE) method. The diameter of the pillars is 2 µm.

3. Results

The carrier lifetimes of the treated samples were studied using microwave PCD (µPCD) which is a Semilab tool that allows carrier lifetime using microwaves to be measured [25]. The results are presented in multiple figures that depict the average carrier lifetime of a plane silicon wafer (total area of the wafer is 1 cm^2), an RIE micropillar silicon wafer, and a MACE micropillar silicon wafer. Figure 3

presents the carrier lifetime of an untreated sample (dark grey) and a sample treated with Al_2O_3 (light grey). It is observed that the average carrier lifetime of a planar sample is 10.7 µs. The average carrier lifetime of a sample with micropillars etched using the reactive ion etching technique is 1.92 µs and a sample with micropillars etched using the Metal Assisted Chemical Etching technique is 9.86 µs.

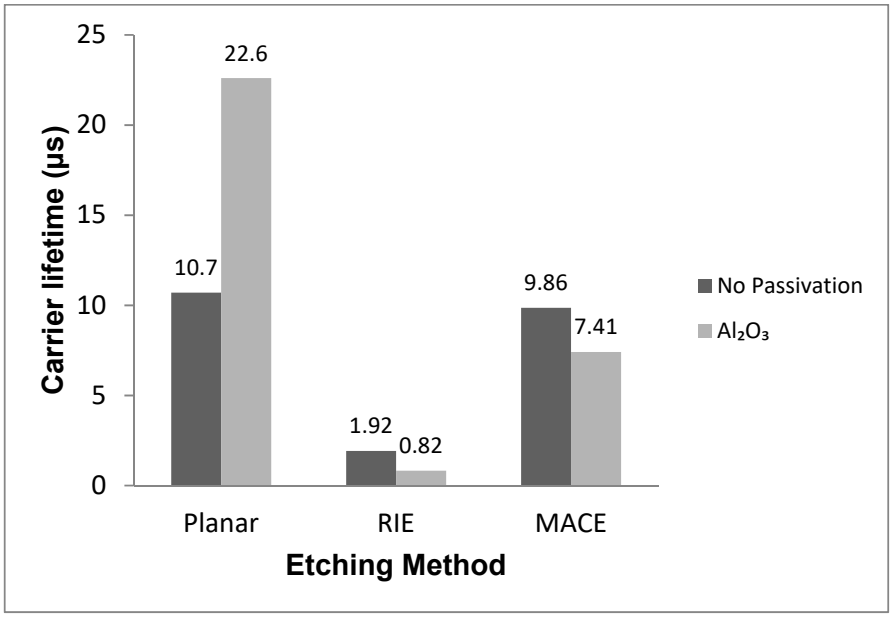


Figure 3. The carrier lifetime of the untreated samples and the samples treated with Al_2O_3.

The average carrier lifetime of the planar sample treated with Al_2O_3 is 22.6 µs which is an increase from the untreated planar. The RIE treated with Al_2O_3 sample has a lifetime of 0.82 µs which is a decrease in the lifetime from the non-treated RIE sample. The MACE sample also shows a decrease from 9.86 µs to 7.41 µs in its lifetime when treated with Al_2O_3.

Figure 4 presents the results of the samples treated with KOH. The average carrier lifetime of the planar sample is 7.33 µs which is a decrease from the untreated planar sample. The RIE treated with KOH sample has a lifetime of 0.92 µs which is a decrease in the lifetime from the untreated RIE sample. The MACE sample also shows a decrease from 9.86 µs to 6.38 µs in its lifetime when treated with KOH.

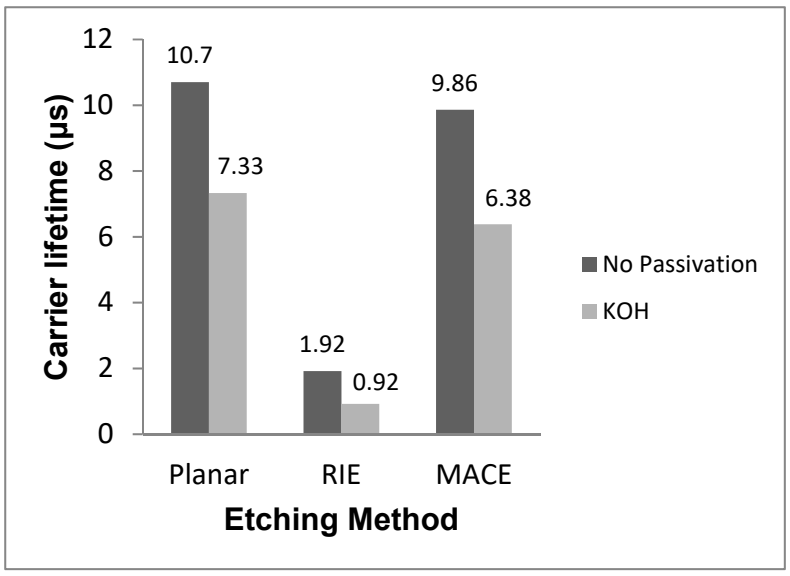


Figure 4. The carrier lifetime of the untreated samples and the samples treated with KOH.

Figure 5 presents the results of the samples treated with SiO_2. The average carrier lifetime of the planar sample is 7.23 µs which is a decrease from the untreated planar sample. The untreated RIE sample has a carrier lifetime of 1.92 µs and the RIE sample treated with SiO_2 has a carrier lifetime of 0.98 µs. The MACE sample also shows a decrease from 9.86 µs to 8 µs in its lifetime when treated with SiO_2.

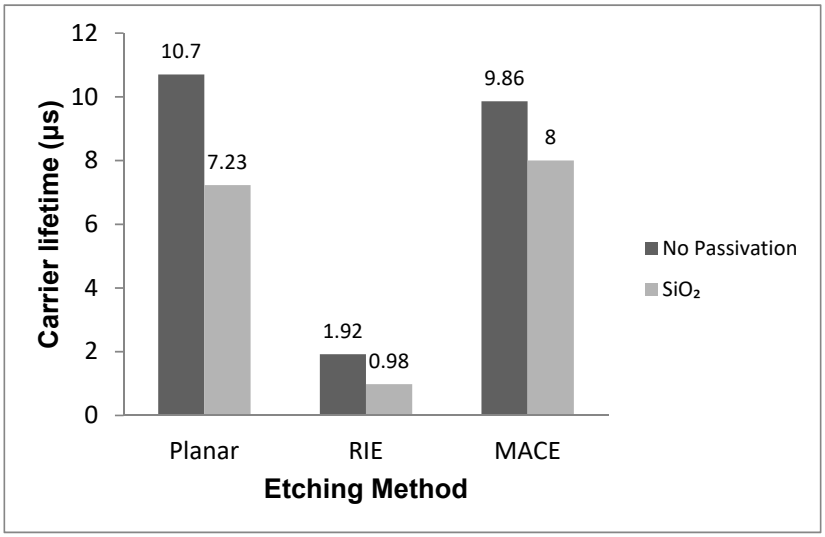


Figure 5. The carrier lifetime of the untreated samples and the samples treated with SiO_2.

Figure 6 presents the results of the samples treated with SiN. The average carrier lifetime of the planar sample is 4.73 µs which is a decrease from the untreated planar sample. The untreated RIE sample has a carrier lifetime of 1.92 µs and the RIE sample treated with SiN has a carrier lifetime of 8.22 µs. The MACE sample also shows a decrease from 9.86 µs to 1.72 µs in its lifetime when treated with SiN.

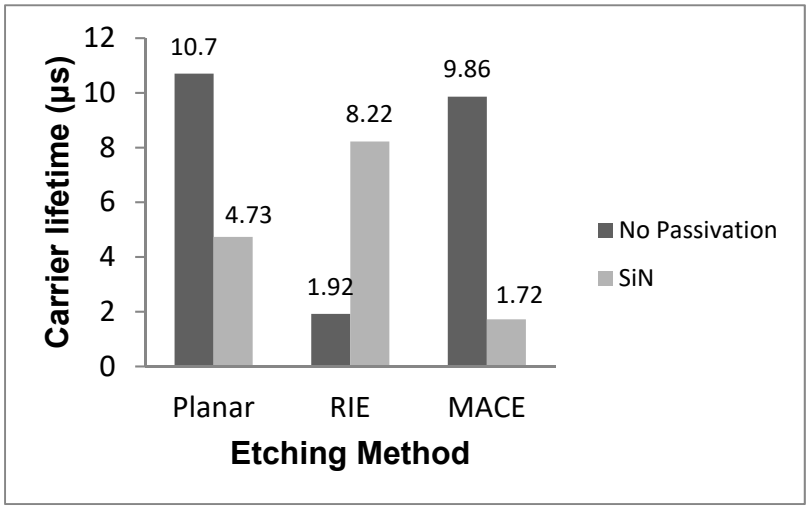


Figure 6. The carrier lifetime of the untreated samples and the samples treated with SiN.

Figure 7 presents the results of the samples treated with SiO_2 and SiN. The average carrier lifetime of the planar sample is 17.75 µs which is an increase from the untreated planar sample. The untreated RIE sample has a carrier lifetime of 1.92 µs and the RIE sample treated with SiO_2/SiN has a carrier lifetime of 14.62 µs. The MACE sample shows an increase from 9.86 µs to 11.09 µs in its lifetime when treated with SiO_2/SiN. Table 1 presents the mapping of the carrier lifetime over the area of the wafer. The table shows the average carrier lifetime in each sample. The second row indicates the mapping of the carrier lifetime over the surface area of the sample.

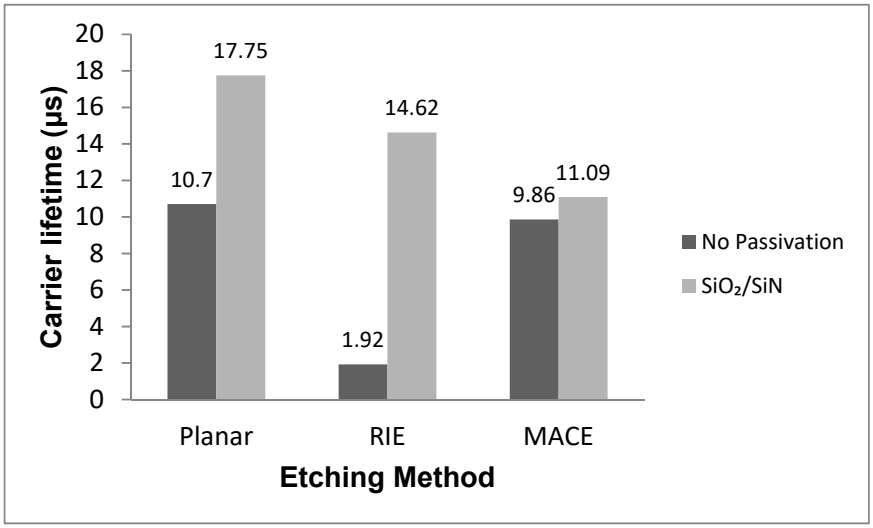
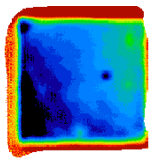
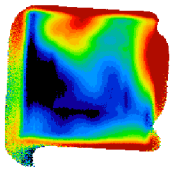
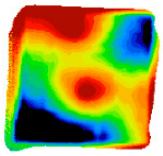
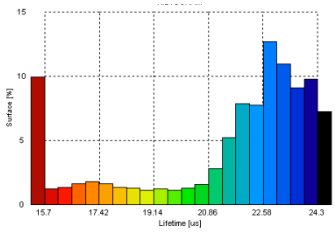
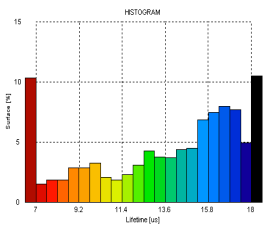
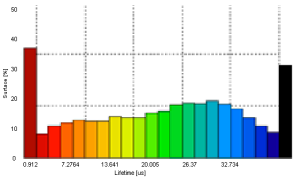


Figure 7. The carrier lifetime of the untreated samples and the samples treated with SiO_2/SiN.

Table 1. Mapping of the Carrier Lifetime of a sample passivated with SiO_2/SiN.

	Planar	RIE	MACE
Average Carrier Lifetime	17.8 µs	14.6 µs	11.1 µs
Image			
Histogram			

4. Discussion

The measurements above show the effective minority carrier lifetime (τ_{eff}) that was obtained for the different passivation cases. It should be noted that back surface passivation was not performed in this experiment which is a reason for the low carrier lifetime readings of the samples, thus the reading gives only an indication of the front lifetime. The minority carrier lifetime could be expressed as [26]:

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{bulk}} + \frac{\left(S^F_{eff} + S^B_{eff}\right)}{d}$$

where τ_{bulk} is the bulk Shockley–Read–Hall (SRH) lifetime, S^F_{eff} and S^B_{eff} are the effective surface recombination velocity at the front surface and at the back surface, respectively, and d is the wafer thickness. It has been demonstrated that by increasing the surface area the front surface recombination velocity increases [26]. Since the combination of SiO_2/SiN provided the highest carrier lifetime, this means that it provided the lowest surface recombination velocity. Previous results have

demonstrated that SiO_2 passivation reduces the Si-SiO_2 interface state density which improves the surface recombination [27]. It has been also noted that high Auger recombination near the surface plays a key role in the lifetime of the carriers [27]. The RIE and MACE processes lead to dislocation and dangling bonds which also lead to severe Shockley–Read–Hall (SRH) recombination [27]. Thus the high recombination (low carrier lifetime) is due to surface, Auger, and SRH recombination. SiO_2 passivates the surface and SiN provides bulk passivation because during the deposition of SiN, hydrogen, which is found in the deposition chamber, diffuses in the material. The presence of hydrogen reduces the defect state density and suppresses the Auger recombination near the surface and the SRH recombination in the bulk of the material. Thus, when SiO_2 and SiN are deposited together the highest carrier lifetime is obtained since the surface dislocations are passivated by SiO_2 and the dangling bonds in the bulk of the material bond with hydrogen due to SiN deposition. It also must be noted that in almost all of the measurements the MACE pillars had a carrier lifetime greater than the RIE pillars and this is due to the fact that the micropillar surface formed by RIE may be damaged as a result of the plasma. However, the MACE process results in less damage especially when the ratio of HF and H_2O_2 is controlled [28].

5. Conclusions

The above samples were treated with different methods and it was shown that depositing SiN and SiO_2 on a planar and micro structured sample with two different methods increases the lifetime of the sample. Surface passivation of the back of the sample was not performed and is recommended in the future. It is suggested that this method be used for surface recombination treatments.

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