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A Novel Overcurrent Suppression Strategy during Reclosing Process of MMC-HVDC

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Abstract: A modular multilevel converter based high-voltage DC (MMC-HVDC) system has been the most promising topology for HVDC. A reclosing scheme is usually configured because temporary faults often occur on transmission lines especially when overhead lines are used, which often brings about an overcurrent problem. In this paper, a new fault current limiter (FCL) based on reclosing current limiting resistance (RCLR) is proposed to solve the overcurrent problem during the reclosing process. Firstly, a mesh current method (MCM) based short-circuit current calculation method is newly proposed to solve the fault current calculation of a loop MMC-HVDC grid. Then the method to calculate the RCLR is proposed based on the arm current to limit the arm currents to a specified value during the reclosing process. Finally, a three-terminal loop MMC-HVDC test grid is constructed in the widely used electromagnetic transient simulation software PSCAD/EMTDC and the simulations prove the effectiveness of the proposed strategy.

Keywords: modular multilevel converter (MMC); reclosing process; fault current limiter (FCL); short-circuit current calculation; reclosing current limiting resistance (RCLR)

1. Introduction

The modular multilevel converter (MMC), a new type of voltage source converter (VSC), has many advantages over the traditional two or three level topology, such as better harmonic performance, low switching frequency, etc. This advanced technology is envisioned as the most promising option for the integration of renewable energy sources and has been widely investigated in recent years [1–3]. In China, an MMC-HVDC grid usually uses overhead lines because large-scale renewable energy bases are generally far from load centers, as it makes the fault ride-through of MMC-HVDC grid become more thorny [4].

Currently, the half-bridge sub-module (HBSM) is the main topology of a practical MMC-HVDC grid because of better economy [5]. When a short-circuit fault occurs on the DC line, very large fault currents will be caused in the DC lines and converters [6]. Since temporary faults often occur on overhead lines, MMC-HVDC needs reclosing to improve the reliability and continuity of the power supply [7]. Consequently, the vulnerable power electronic elements in the converter will be exposed to overcurrent again when the system attempts to reclose a permanent fault.

The suppression of overcurrent mainly depends on an effective fault current limiter (FCL). Reference [8] limited the overcurrent in HVDC lines by a current limiting inductor (CLI) and studied the impact of different sizes on current rise. Reference [9,10] studied the performance of a superconducting fault current limiter (SFCL) and concluded that the appropriated SFCL can reduce the fault current peak, the size of the CLI and also the fault identification time. Reference [11] presented a solid state FCL in a VSC-HVDC system with MMC converters, but the detailed structure and the configuration method were not clear. Reference [12,13] both proposed a resistive DC fault current limiter. The limiter

was installed in each arm or at the outlet of the converter to increase the damping performance of the DC fault current loop and effectively limit the dc-side current, and then interrupt the fault circuit by a breaker. Reference [14] proposed a RL-FCL which is composed of a reactor, a resistor, a reversed diode and an IGBT connected in parallel to limit the overcurrent and the overvoltage. The aforementioned references mainly focused on the overcurrent limiting when the fault occurred but did not conduct further research on the post-fault and the reclosing process.

There has been little research on reclosing process, especially for MMC-HVDC. Reference [15] used two thyristors in parallel with the sub-modules to realize fault clearance and automatic recovery, but the converter must be blocked for a long time when reclosing a permanent fault. Reference [16] used series braking resistance (SBR) cooperating with a high-temperature superconducting FCL to reduce the fault currents during reclosing, but it did not illustrate how to select the parameter of the SBR. A soft reclosing model (SRM) is proposed in Reference [17] to limit the reclosing over-current of VSC-MTDC. However, the current calculation in this reference is made on the assumption that the voltage discharge voltage remains constant and neglects the restriction of the safety of the equipment. Overcurrent suppression during the reclosing process of MMC-HVDC needs further research.

This paper focuses on the suppression of overcurrent for overhead lines based MMC-HVDC grid during the reclosing process. First, mesh current method (MCM) based short-circuit current calculation is introduced to a loop MMC-HVDC grid. Then a novel FCL, which consists of a CLI, a reclosing current limiting resistance (RCLR) and a bypass switch, is proposed. Compared with traditional FCL, the proposed circuit can limit the maximum arm currents to a specified value during the reclosing process, and the calculation method of RCLR is also given in details.

2. Fault Current Calculation of a Loop MMC-HVDC Grid

2.1. Characteristics of a Pole-to-Pole Fault

A common three-phase MMC is shown in Figure 1. It is composed of six arms and each arm consists of N sub-modules (SMs) connected in series and an arm inductor L_0 . Each SM includes two insulated gate bipolar transistors (IGBTs), two diodes and a DC capacitor C_0 . If the SM is 'ON' state, the output of SM is the dc capacitor voltage. When the SM is 'OFF' state, the output of SM is zero.

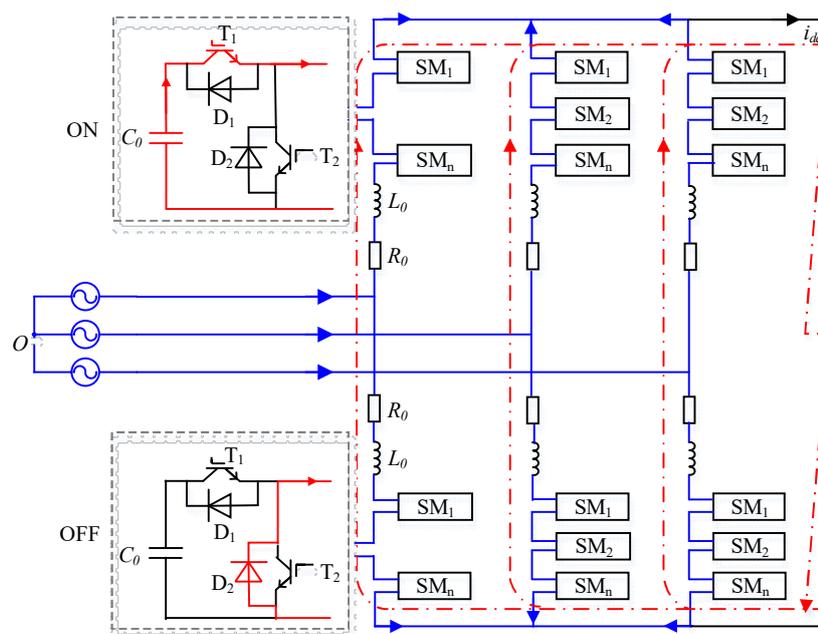


Figure 1. Fault current path of a pole-to-pole fault before converter blocking.

The pole-to-pole fault is the most serious fault in the DC side of MMC-HVDC. The fault process can be divided into two stages according to whether the converter is blocked [18].

Before the converter is blocked, the arm current is shown in Figure 1. During this stage, all the capacitors of SMs in ‘ON’ state will discharge through T_1 immediately (the red line), and thus the currents in the arms and DC lines increase extremely fast. For the AC system, the fault is equivalent to a three-phase short-circuit. So, the AC system also injects short-circuit currents (the blue line) during this stage, whereas they are not capable of flowing into the DC lines, because their contributions sum to zero in the converter. The arm current is a superposition of the discharging current and three-phase short-circuit current. Due to the sorting algorithm within the converter, there are always N SMs being switched in thus all the SMs will discharge during the fault. Given to the high control frequency, the SMs in the upper and the lower arm can be regarded as discharging at the same time. Therefore, the equivalent circuit of the converter during this stage is displayed as Figure 2.

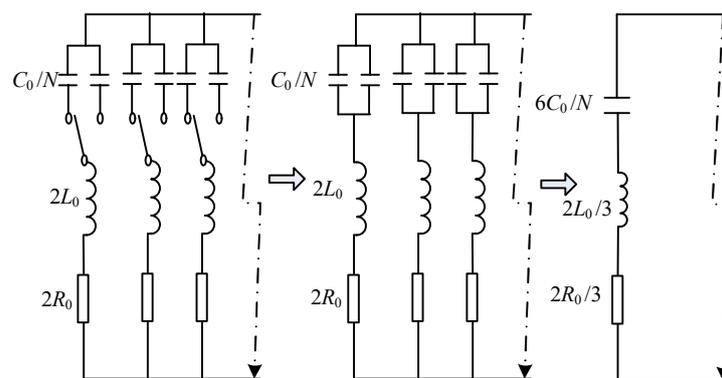


Figure 2. Equivalent circuit of the converter under a pole-to-pole fault before converter blocking.

If the arm current in any arm exceeds the threshold of overcurrent protection of SM, the converter will be blocked immediately. The fault process after blocking can be further divided into two sub-stages. The first one is inductor free-wheeling circuit as is shown in Figure 3a. The fault currents are maintained by the arm inductor. At this stage, each arm still carries a third of the DC line current, and no AC currents are injected in DC line.

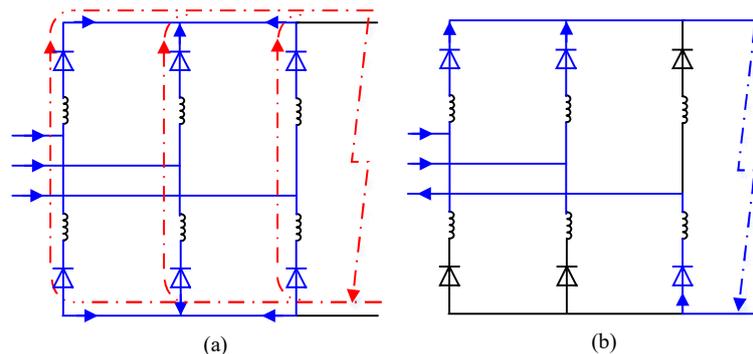


Figure 3. The fault response after converter blocking: (a) free-wheeling; (b) uncontrolled rectifier.

The stage of inductor free-wheeling will end when the inductor free-wheeling current decrease to zero. Then the converter starts to act as an uncontrolled rectifier as Figure 3b. At this stage, the fault currents in the DC lines are fed by the AC system. Generally, the protection time in MMC-HVDC grid is within 5 ms after the fault occurrence [19], so this stage of the uncontrolled rectifier seldom occurs in practical system.

2.2. Short-Circuit Current Calculation Method

The short-circuit current calculation of a loop MMC-HVDC is different from that of a two-terminal MMC-HVDC or a star join multi terminal DC grid as the fault current of the latter can be calculated separately. For a loop MMC-HVDC, as displayed in Figure 4, all the converters inject fault current through different lines to the fault spot, and the currents from different converters cause coupling through problem.

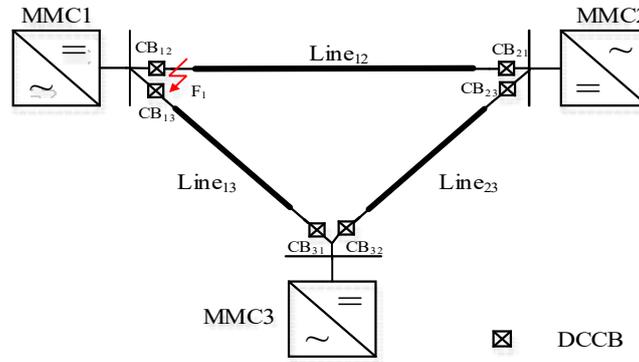


Figure 4. The diagram of the three-terminal loop modular multilevel converter based high-voltage DC (MMC-HVDC) grid.

To handle the current coupling problem, the mesh current method (MCM) is first introduced to a short-circuit current calculation of MMC-HVDC grid before the converters are blocking. For example, when there is a pole-to-pole fault at the DC outlet of MMC1, the whole grid can be divided into four meshes. The equivalent circuit is illustrated in Figure 5. L_i , C_i and R_i represent the equivalent circuit of the converter, r_{ij} and l_{ij} represent the DC overhead lines and L_{ij} is CLI. According to the four meshes, a state equation can be established as Equations (1) and (2). Then the current in different lines can be calculated.

$$\begin{bmatrix} 1 & 0 & 0 \\ 1 & 0 & -1 \\ 0 & 1 & -1 \\ 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} u_{c1} \\ u_{c2} \\ u_{c3} \end{bmatrix} = \begin{bmatrix} R_1 & R_1 & 0 & 0 \\ R_1 & 2r_{13} + R_1 + R_3 & R_3 & 0 \\ 0 & R_3 & 2r_{23} + R_2 + R_3 & R_2 \\ 0 & 0 & R_2 & 2r_{12} + R_2 \end{bmatrix} \begin{bmatrix} i_{14} \\ i_{13} \\ i_{23} \\ i_{24} \end{bmatrix} + \begin{bmatrix} 2L_{12} + L_1 & L_1 & 0 & 0 \\ L_1 & 2(L_{13} + L_{31} + l_{13}) + L_1 + L_3 & L_3 & 0 \\ 0 & L_3 & 2(L_{23} + L_{32} + l_{23}) + L_2 + L_3 & L_2 \\ 0 & 0 & L_2 & 2(L_{21} + L_{13}) + L_2 \end{bmatrix} \begin{bmatrix} \dot{i}_{14} \\ \dot{i}_{13} \\ \dot{i}_{23} \\ \dot{i}_{24} \end{bmatrix} \quad (1)$$

$$\begin{bmatrix} \dot{u}_{c1} \\ \dot{u}_{c2} \\ \dot{u}_{c3} \end{bmatrix} = \begin{bmatrix} 1/C_1 & 0 & 0 \\ 0 & 1/C_2 & 0 \\ 0 & 0 & 1/C_3 \end{bmatrix} \begin{bmatrix} 1 & 1 & 0 & 0 \\ 0 & 0 & 1 & 1 \\ 0 & -1 & -1 & 0 \end{bmatrix} \begin{bmatrix} i_{14} \\ i_{13} \\ i_{23} \\ i_{24} \end{bmatrix} \quad (2)$$

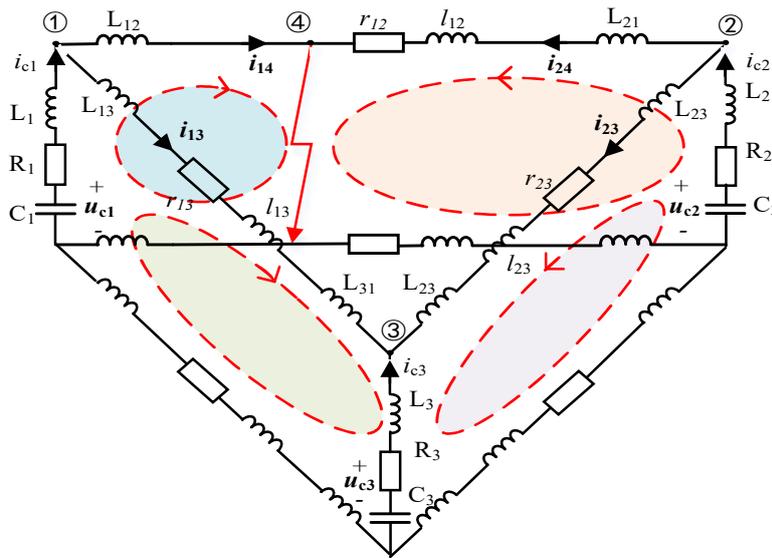


Figure 5. The equivalent circuit of SMs discharging under pole-to-pole fault.

3. Operation Principle of the Reclosing Current Limiting Resistance based Fault Current Limiter

3.1. The Operation Principle of the Fault Current Limiter

The CLI is an effective and mature device to limit fault currents in the MMC-HVDC grid, but it can't further reduce the overcurrent stresses on the power electronic elements in the converter in the reclosing process. Therefore, an additional circuit, which is composed of an RCLR and a parallel switch, is proposed based on the traditional CLI, as shown in the dotted line box of Figure 6.

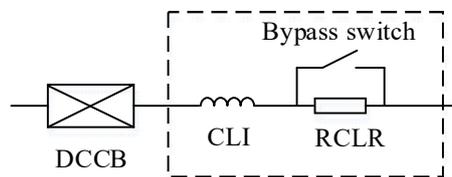


Figure 6. The structure of the proposed current fault limiter.

Similar to an AC system, the fault ride-through of an overhead lines based MMC-HVDC grid needs two or three reclosing attempts to determine whether the fault is temporary. Figure 7 shows the sequence of fault ride-through when reclosing a permanent fault. The fault starts at the instant of t_0 , and the DCCB on the faulty line will be tripped at t_{r1} after the protection identification time of Δt_c . During the deionization time of Δt_d , the bypass switch is opened, and thus the RCLR is inserted into the fault loop. The DCCB is reclosed at t_{p1} and tripped again at t_{r2} after detecting there is still a fault. By using the RCLR, the overcurrent stresses on powering electronic elements can be reduced significantly, and the converter can keep continuous operation. The same reclosing process will be done at t_{p2} and t_{r2} . At last, the DCCB will never be reclosed after the identification of a permanent fault. The bypass switch is opened at t_{R2} and waits for the next operation command.

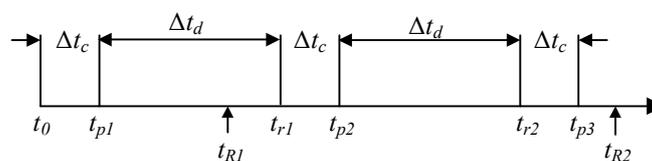


Figure 7. The sequence of fault ride-through when reclosing a permanent fault.

3.2. The Calculation Method of RCLR

There are two main electric elements in the proposed FCL. The main function of CLI is to limit the rise rate of fault currents and ensure the reliable operation of the DCCB, while that of the RCLR is to reduce the overcurrent in the converter during reclosing. Extensive papers have studied the calculation method of the CLI in MMC-HVDC grid [8,20–22], so it will not be discussed in this paper. The main contribution of this paper is to propose a novel calculation method of RCLR, which can limit the arm currents to a specified value. According to the aforementioned analysis, the constraint of the RCLR is denoted by Equation (3). I_{\max} represents the maximum value of arm current during reclosing, I_{th} represents the threshold of SMs overcurrent protection, and k is ratio coefficient which denotes the limiting level of fault currents.

$$I_{\max} \leq k \times I_{th} \quad (3)$$

By using the RCLR, only SMs discharging will appear during reclosing, whereas it is difficult to describe the accurate relations between arm currents and RCLR through mathematical equations. In order to solve this problem, a method of estimating the maximum arm current is proposed. The FCL reduces the discharging speed of the SMs significantly during reclosing, so the AC output can be considered still under control within the several milliseconds after fault. If the circulating currents in the arm are neglected, the maximum current in the arm is approximately equal to Equation (4)

$$I_{arm} = \frac{i_{ac}}{2} + \frac{1}{3} |i_{dc}(\Delta t_c)| \quad (4)$$

where i_{ac} is the amplitude of phase current in the AC side of converter, i_{dc} represents the current measured at positive pole of the converter shown in Figure 1, and the Δt_c is protection time from reclosing time to the trip time of the DCCB. By substituting (4) into (3), the following inequality can be obtained as Equation (5). Define the value satisfying the equation condition of (5) as the critical resistance R_0 .

$$\frac{i_{ac}}{2} + \frac{1}{3} |i_{dc}(\Delta t_c)| \leq k \times I_{th} \quad (5)$$

4. Simulation

4.1. The Test System

A three-terminal MMC-HVDC grid, shown in Figure 4, is modeled based on PSCAD/EMTDC simulation platform. The system adopts the symmetric monopole configuration with a rated DC voltage of ± 20 kV. All the converters are connected by bipolar transmission lines which make use of a frequency-dependent distributed parameter model, and a hybrid DCCB and a FCL are placed at the terminal of each line. MMC1 and MMC3 control the active power, while MMC2 controls the DC voltage. The detailed parameters of the test system are shown in Table 1. Other simulation parameters are set as follows: the protection time Δt_c is 5 ms; the deionization time Δt_d is 150 ms; the threshold of SMs overcurrent protection I_{th} is 2 kA; the CLI on each line is 15 mH. Moreover, the converter will be blocked after the fault current declines to 10 A.

Table 1. The parameters of the test system.

Quantity	Value
AC line voltage	10 kV
Fundamental frequency	50 Hz
Number of SMs per arm	20
SM capacitor	6000 μ F
Arm reactor	15 mH
Arm resistance	0.1 Ω
Transformer leakage reactance	0.1

4.2. The Validation of the FCL

For the test system, a pole-to-pole fault F_1 is applied at the DC outlet of MMC1. The overcurrent in MMC1 is the most serious, and thus it will be taken as the example for simulation. When the RCLR R_{12} is configured, the equivalent circuit in Figure 4 is modified as Figure 8 and Equation (1) is modified as Equation (6). The upper and lower limitation of the RCLR are set to 0 and 15 Ω , respectively, and the calculation step is 0.1 Ω .

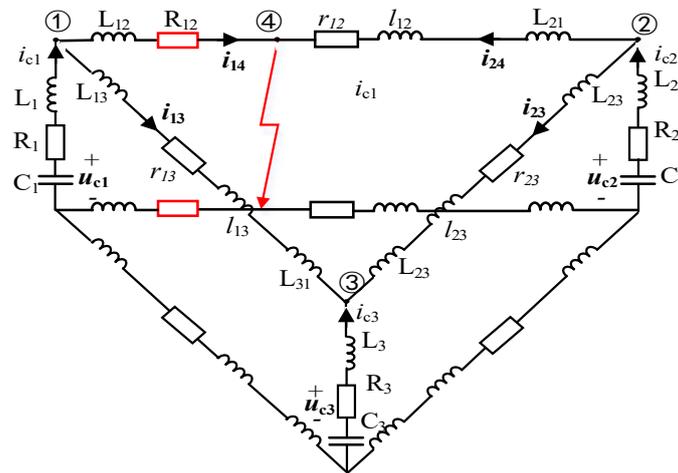


Figure 8. The equivalent circuit of SMs discharging with reclosing current limiting resistance (RCLR).

$$\begin{bmatrix} 1 & 0 & 0 \\ 1 & 0 & -1 \\ 0 & 1 & -1 \\ 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} u_{c1} \\ u_{c2} \\ u_{c3} \end{bmatrix} = \begin{bmatrix} 2R_{12} + R_1 & R_1 & 0 & 0 \\ R_1 & 2r_{13} + R_1 + R_3 & R_3 & 0 \\ 0 & R_3 & 2r_{23} + R_2 + R_3 & R_2 \\ 0 & 0 & R_2 & 2r_{12} + R_2 \end{bmatrix} \begin{bmatrix} i_{14} \\ i_{13} \\ i_{23} \\ i_{24} \end{bmatrix} + \begin{bmatrix} 2L_{12} + L_1 & L_1 & 0 & 0 \\ L_1 & 2(L_{13} + L_{31} + l_{13}) + L_1 + L_3 & L_3 & 0 \\ 0 & L_3 & 2(L_{23} + L_{32} + l_{23}) + L_2 + L_3 & L_2 \\ 0 & 0 & L_2 & 2(L_{21} + L_{13}) + L_2 \end{bmatrix} \begin{bmatrix} i_{14} \\ i_{13} \\ i_{23} \\ i_{24} \end{bmatrix} \quad (6)$$

By solving (2) and (6), the relation between the maximum arm current and the critical resistance R_0 of FCL can be obtained, as shown in Figure 9.

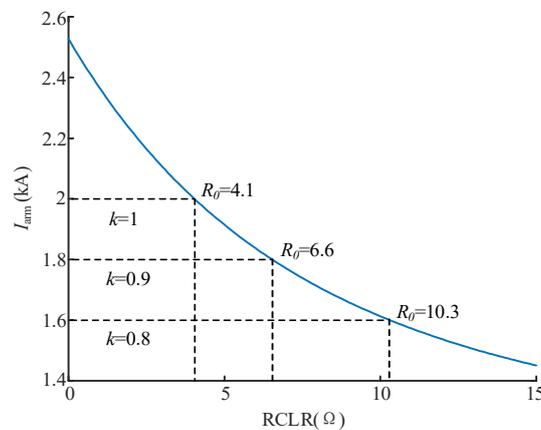


Figure 9. The maximum calculated arm currents with the different RCLR.

Take $k = 1$, $k = 0.9$ and $k = 0.8$ for examples to verify the effectiveness of the proposed calculation method. Figure 10 shows the DC currents on the faulty line where 'k = ×' means without RCLR (only using the CLI). Figure 11 shows the arm currents in MMC1 under different current limiting levels.

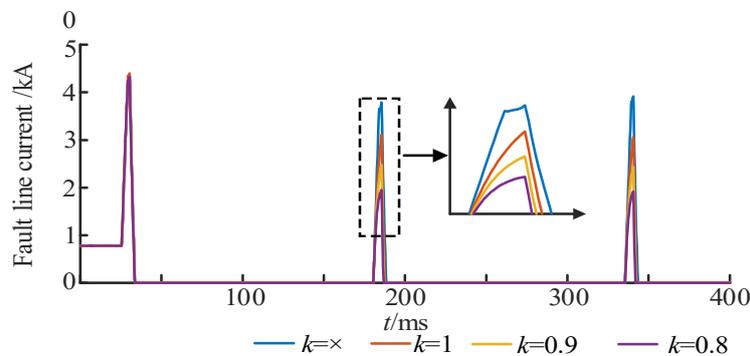


Figure 10. MMC1 DC fault current in $line_{12}$.

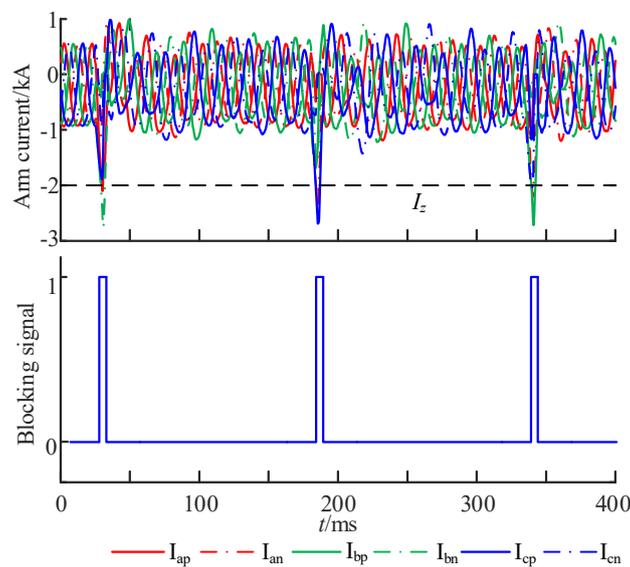


Figure 11. Arm current and blocking signal without RCLR.

As is observed in Figures 10 and 11, serious overcurrent still exists without RCLR during reclosing, and the converter is blocked again when reclosing the DCCB leading to the interruption of power flow for a long time. However, by using the proposed RCLR, the fault currents in both the faulty line and converter will be reduced significantly during reclosing, and the converter can keep continuous operation without blocking. As it is observed in Figure 12, the maximum value of arm current under different current limiting level is close to but less than the specified value and the converters are not blocked during the reclosing process. The proposed method can meet the overcurrent limiting requirement with a lower resistance value proving the calculation method is accurate and effective.

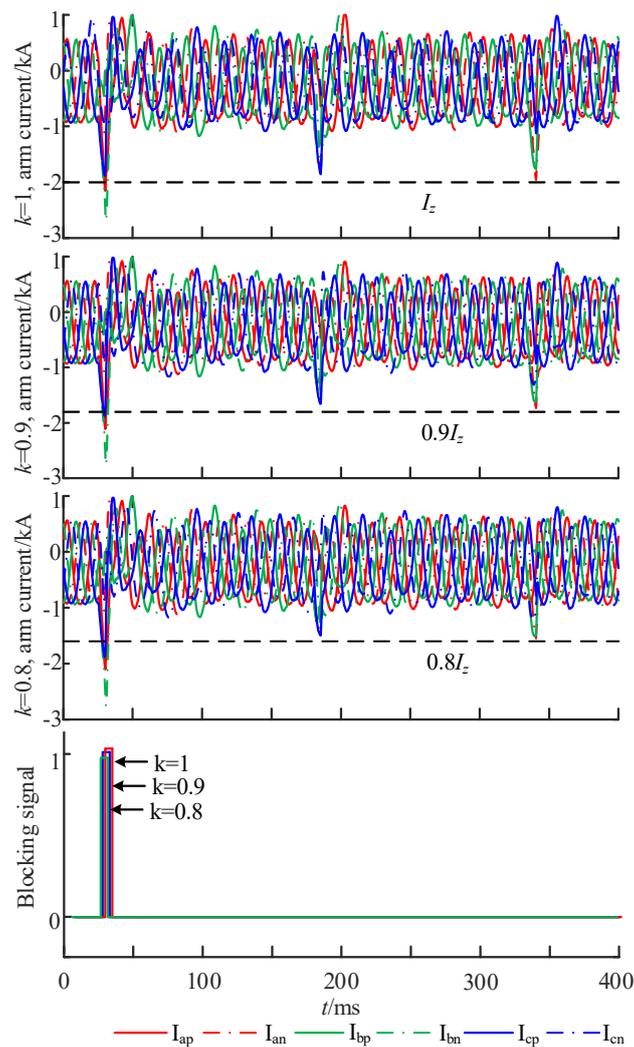


Figure 12. Arm current and blocking signal with RCLR.

5. Discussion

There has been wide research on the fault current limiter (FCL), such as the current limiting inductor (CLI), superconducting fault current limiter (SFCL), Solid State FCL and resistive fault current limiter. All the limiters will work when the fault occurs to limit the current to a lower amplitude and then break the fault circuit. For CLI, it is capable of limiting the overcurrent rise, but too many inductors in the DC grid will influence the transient response, stability and the speed for DCCB interrupting the fault current. Moreover, a large value inductor will bring large size and manufacturing burdens. For SFCL, it can reduce the fault current peak and the size of CLI, but it costs too much. A solid state FCL can interrupt the DC fault current very quickly in even hundreds of microseconds but the extra large amount of power electronic components bring much conduction loss. Resistive fault current limiter usually aims to accelerate the process of fault current decaying and is often activated by electronic switches but neglects the high voltage exerted on the electronic components at the switching. The above current limiting strategies all mean to limit the current to some level making the DCCB or other breakers to interrupt the fault current more quickly and easily. None of them pay attention to the post-fault process.

Research on the current limiting during the reclosing process for MMC-HVDC is really rare. Reclosing is necessary for an MMC-HVDC system to determine whether the fault is temporary or permanent. For a permanent pole-to-pole fault, the arm will undergo overcurrent again during each

reclosing process. So, the overcurrent suppression during the reclosing process is of great significance. In the present literature, resistive limiters have been proposed but there are two problems remaining unsolved. Firstly, none of them accurately calculated the overcurrent, which is the base of current limiting. Secondly, a detailed configuration method of the limiter, especially of the calculation of the resistor, was not given or well-thought-out. In this paper, accurate current is calculated based on the proposed mesh current method, and the detailed calculation method of RCLR is conducted. The selection of resistor is based on different limiting levels of the fault current which is flexible for different thresholds of SMs overcurrent protection. The proposed method in this paper can limit the overcurrent to a required level with a lower resistance value.

6. Conclusions

Overcurrent will recur during the reclosing process without any current limiting strategy under a permanent pole-to-pole fault in MMC-HVDC which may threaten the safety of the power electronic elements and even the system. Moreover, the overcurrent will make the converter block repeatedly. To configure a reasonable FCL, the key is to calculate the overcurrent accurately and figure out the tolerance for the overcurrent. In this paper, a mesh current method (MCM) is proposed to calculate the short-circuit current based on the state equation. Based on the current calculation and the threshold of SMs overcurrent protection, the configuration principle of the reclosing current limiting resistance is proposed. The simulations constructed in PSCAD/EMTDC prove that the proposed method in this paper can limit the overcurrent in the arm to a required level under different limiting levels to protect the power electronic elements and preventing the converter frequently blocking during the reclosing process which may shorten the recovery time for the system. So, the overcurrent suppression strategy during the reclosing process of MMC-HVDC proposed in this paper is effective from the perspective of security and operation efficiency.

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References

1. Jiang, B.; Wang, Z. The key technologies of VSC-MTDC and its application in China. *Renew. Sustain. Energy Rev.* **2016**, *62*, 297–304.
2. Jiang, B.; Gong, Y.; Li, Y. Fault Detection and Location of IGBT Short-Circuit Failure in Modular Multilevel Converters. *Energies* **2018**, *11*, 1492. [[CrossRef](#)]
3. Zhang, Y.; Ravishankar, J.; Fletcher, J.; Li, R.; Han, M. Review of modular multilevel converter based multi-terminal hvdc systems for offshore wind power transmission. *Renew. Sustain. Energy Rev.* **2016**, *61*, 572–586. [[CrossRef](#)]
4. Han, X.; Sima, W.; Yang, M.; Li, L.; Yuan, T.; Si, Y. Transient Characteristics Under Ground and Short-Circuit Faults in a ± 500 kV MMC-Based HVDC System with Hybrid DC Circuit Breakers. *IEEE Trans. Power Del.* **2018**, *33*, 1378–1387. [[CrossRef](#)]
5. Zhang, L.; Zou, Y.; Yu, J.; Qin, J.; Vittal, V.; Karady, G.G.; Shi, D.; Wang, Z. Modeling, control, and protection of modular multilevel converter-based multi-terminal HVDC systems: A review. *CSEE J. Power Energy Syst.* **2017**, *3*, 340–352. [[CrossRef](#)]
6. Cwikowski, O.; Wickramasinghe, H.R.; Konstantinou, G.; Pou, J.; Barnes, M.; Shuttleworth, R. Modular multilevel converter dc fault protection. *IEEE Trans. Power Del.* **2018**, *33*, 291–300. [[CrossRef](#)]
7. Stumpe, M.; Ruffing, P.; Wagner, P.; Schnetzler, A.; Schnetzler, A. Adaptive single-pole auto-reclosing concept with advanced dc fault current control for full-bridge MMC VSC systems. *IEEE Trans. Power Del.* **2018**, *33*, 321–329. [[CrossRef](#)]
8. Sneath, J.; Rajapakse, A.D. Fault Detection and Interruption in an Earthed HVDC Grid Using ROCOV and Hybrid DC Breakers. *IEEE Trans. Power Del.* **2016**, *31*, 973–981. [[CrossRef](#)]

9. Mokhberdorani, A.; Carvalho, A.; Silva, N.; Leite, H.; Carrapatoso, A. Application study of superconducting fault current limiters in meshed HVDC grids protected by fast protection relays. *Electr. Power Syst. Res.* **2017**, *143*, 292–302. [[CrossRef](#)]
10. Lv, C.; Tai, N.; Jin, Z.; Zheng, X. Research on application of superconducting fault current limiter in MMC-MTDC. *J. Eng.* **2017**, *13*, 1307–1311. [[CrossRef](#)]
11. Larruskain, D.M.; Iturregi, A.; Abarrategui, O.; Etxegarai, A.; Zamora, I. Fault Current limiting in VSC-HVDC systems with MMC converters. In Proceedings of the 2016 International Symposium on Power Electronics, Electrical Drives, Automation and Motion (SPEEDAM), Anacapri, Italy, 22–24 June 2016; pp. 332–337.
12. Xie, S.J.; Qiu, Y.F.; Bi, T.S. Resistive DC fault current limiter. *J. Eng.* **2017**, *13*, 1682–1685.
13. Li, J.; Ding, X.B.; Liu, S.; Chen, Z.H.; Li, Z.H. DC fault current-limiting and isolating technique for the MMC-based DC system. In Proceedings of the 2017 China International Electrical and Energy Conference (CIEEC), Beijing, China, 25–27 October 2017; pp. 543–548.
14. Wang, Y.; Yuan, Z.; Wen, W.; Ji, Y.; Fu, J.; Li, Y.; Zhao, Y. Generalised protection strategy for HB-MMC-MTDC systems with RL-CFL under dc faults. *IET Gener. Transm. Distrib.* **2018**, *12*, 1231–1239. [[CrossRef](#)]
15. Li, X.; Liu, W.; Song, Q.; Rao, H.; Xu, S. An enhanced MMC topology with DC fault ride-through capability. In Proceedings of the 39th Annual Conference of the IEEE Industrial Electronics Society (IECON 2013), Vienna, Austria, 10–13 November 2013; pp. 6182–6188.
16. Sanusi, W.; Hosani, M.A.; Moursi, M.E. A novel dc fault ride-through scheme for MTDC networks connecting large-scale wind parks. *IEEE Trans. Sustain. Energy* **2017**, *8*, 1086–1095. [[CrossRef](#)]
17. Ji, S.; Wang, S.L.; Liu, T.Q. A Soft Reclosing Model for Hybrid DC Circuit Breaker in VSC-MTDC System. In Proceedings of the 2018 IEEE 4th Southern Power Electronics Conference (SPEC), Singapore, 10–13 December 2018; pp. 1–5.
18. Li, Y.; Gong, Y.; Jiang, B. A novel traveling-wave-based directional protection scheme for MTDC grid with inductive DC terminal. *Electr. Power Syst. Res.* **2018**, *157*, 83–92. [[CrossRef](#)]
19. Cwikowski, O.; Wood, A.; Miller, A.; Barnes, M.; Shuttleworth, R. Operating DC Circuit Breakers with MMC. *IEEE Trans. Power Del.* **2018**, *33*, 260–270. [[CrossRef](#)]
20. Kontos, E.; Rodrigues, S.; Pinto, R.T.; Bauer, P. Optimization of limiting reactors design for DC fault protection of multi-terminal HVDC networks. In Proceedings of the Energy Conversion Congress and Exposition (ECCE), Pittsburgh, PA, USA, 14–18 September 2014; pp. 5347–5354.
21. Kontos, E.; Bauer, P. Reactor design for DC fault ride-through in MMC-based multi-terminal HVDC grids. In Proceedings of the Annual Southern Power Electronics Conference (SPEC), Auckland, New Zealand, 5–8 December 2016; pp. 1–6.
22. Tzelepis, D.; Dysko, A.; Fusiek, G.; Nelson, J.; Niewczas, P.; Vozikis, D.; Orr, P.; Gordon, N.; Booth, C.D. Single-ended differential protection in MTDC networks using optical sensors. *IEEE Trans. Power Del.* **2017**, *32*, 1605–1615. [[CrossRef](#)]

