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Classic Discrete Control Technique and 3D-SVPWM Applied to a Dual Unified Power Quality Conditioner

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Abstract: The unified power quality conditioners (UPQCs) are useful to correct distortions in voltage and current waveforms in case of problems related to harmonics, flicker, and power factor. The dual topology of the UPQC allows a loop control in the inverters less demanding in terms of switching functions; however, the control techniques proposed in the literature have some disadvantages as large computation time and some calculation delays. Therefore, this paper presents the application of a classic discrete-time control model for a three-dimensional space vector pulse width modulation (3D-SVPWM) to be used with the dual UPQC, obtaining a fixed commutation frequency and a low computation cost. The results show that the applied method helps to reduce the harmonics in the source, voltage sags and load current and improve the power factor of the electrical circuit tested. Furthermore, the high frequency created by the switching of elements in the UPQC is filtered by the impedance of the power source and it does not represent a problem for the circuit. Due to the simplicity of the model, simulations demonstrate that the application of this classical control technique is enough to achieve good results to compensate harmonics and power factor with the dual UPQC. The development of the controllers is carried out by discretization of the transfer functions of the control in continuous time and their application with the three-dimensional space vector pulse width modulation (3D-SVPWM) technique.

Keywords: active power filter (APF); series compensator; shunt compensator; three-dimensional space vector pulse width modulation (3D-SVPWM); classic control

1. Introduction

Most efforts to improve power system operation are focused on using the most advanced technical solutions such as flexible AC transmission systems (FACTS) [1,2], and for distribution networks, there is a wide variety of options that includes series and shunt compensators to improve power quality or reduce harmonics problems [3,4]. Therefore, the unified power quality conditioner (UPQC) is considered as a good solution because it gives versatility when compensating several problems simultaneously [5].

An UPQC consists of two power inverters operating as active filters that share the same direct current (DC) bus [6–11]; and they are widely used as energy controllers [12–15]. The active power filters (APFs) are connected to the power system generally by means of coupling inductors for the shunt active power filters (shunt APF), and coupling transformers for the series active power filters

(series APF). Both the shunt and the series inverters operate as controlled voltage or current sources in the system, mitigating the effects of power quality problems such as voltage and current harmonics, voltage sags, momentary voltage swells, flicker, unbalanced source, and unbalanced load.

The schematic diagram of the UPQC is presented in Figure 1 [16–18], where the series and shunt APFs are used to improve the harmonics. The term i_{ia}, i_{ib}, and i_{ic} are the currents of the main electrical circuit that considers the source and load, which is supplied through phases a, b, and c, respectively; R_{rda}, R_{rdb}, and R_{rdc} are the resistances of the power grid in phases a, b, and c, respectively; L_{rda}, L_{rdb}, and L_{rdc} are the inductances of the power grid in phases a, b, and c, respectively; V_B is the DC link voltage; C_{b1} and C_{b1} are the corresponding capacitors in the DC bus; i_{csa}, i_{csb}, and i_{csc} are the currents of the series APF in phases a, b, and c, respectively; i_{cpa}, i_{cpb}, and i_{cpc} are the currents of the shunt APF in phases a, b, and c, respectively; L_{sa}, L_{sb}, and L_{sc} are the inductances of the series APF in phases a, b, and c, respectively; and finally, L_{pa}, L_{pb}, and L_{pc} are the inductances of the shunt APF, in phases a, b, and c.

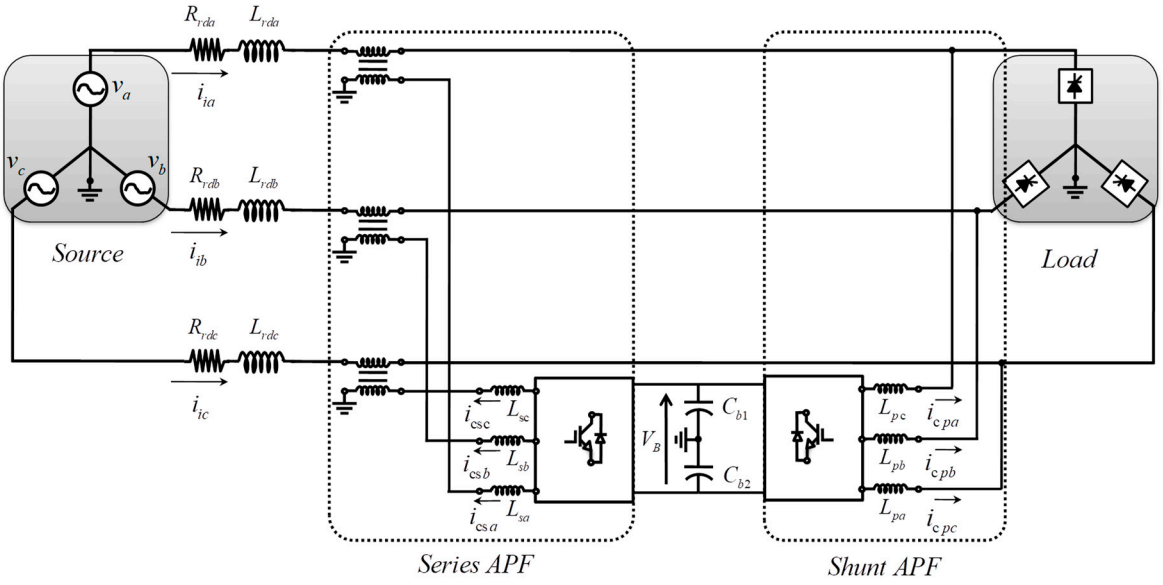


Figure 1. Diagram of power quality unified conditioner (UPQC).

The traditional topology and the dual topology of the UPQC have identical devices in their circuit configuration, as shown in Figures 2 and 3. Thus, the traditional topology of the UPQC considers a series of APF that work as a controlled voltage source and a shunt APF that works as a controlled current source (see Figure 2). On the other side, the filters in the dual topology of the UPQC are interchanged and now the shunt APF works as a controlled voltage source and the series APF works as a controlled current source [19–23] (see Figure 3); where the terms v_f and i_f are the controlled voltage and current sources of the APFs, respectively.

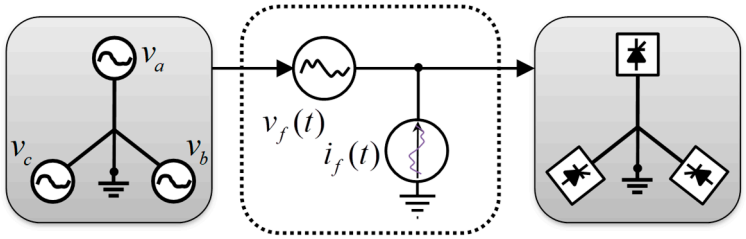


Figure 2. UPQC in traditional topology.

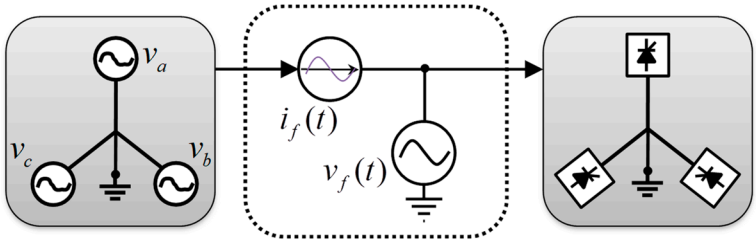


Figure 3. UPQC in dual topology.

The main advantage of the dual topology of the UPQC lies in the loop control of the inverters. In the traditional UPQC model, the voltage and current reference signals are highly distorted, and consequently, the control effort in power devices is considerable when trying to generate these distorted waveforms. On the other hand, in the dual UPQC, the compensation voltage references are pure sinusoidal, which allows a less demanding in the inverters in terms of switching frequency.

The use of UPQCs in distribution networks and their performance analyses are widely found in the literature. For example, in [24] the authors verify the static and dynamic performance of the power quality conditioners PQC operating as UPQC. Besides, in [25], authors propose the use of three isolated H-bridge with a voltage source at the DC side of series active power filter with capability to protect sensitive loads against harmonics, sags, swells and unbalances of the power system voltages. Furthermore, in [17], the authors present an experimental evaluation of a digital control system based on a dual digital signal processor architecture for a three-phase UPQC; where the results show the minimization of delays caused by the processing time and the increment of the UPQC performance.

On the other side, several control techniques have been proposed in the literature [5], such as the based on artificial neural networks to separate the harmonics in the nonlinear load [26,27], which can present delays and large computation time. Other authors have used wavelet analysis techniques to represent a time-varying signal to control the UPQC [5], such as in [28] where a control strategy is proposed to extract the compensating signals for the control of series and shunt converters of the UPQC, or in [29] where it is used for power quality improvement with the UPQC. Other techniques based on *pq* and *dq* theories have been proposed [5], such as in [30] where the authors proposed a solution for power quality issues with the UPQC under-voltage and load unbalances conditions; or in [31], where the authors use a UPQC to inject a minimum active power and with limitations in the rated voltage capacities of the series compensators and the phase difference during voltage sags events; however these techniques use low pass and high pass filters that can affect the performance of the controller [5].

The literature shows that the UPQC has been used to improve power quality and the harmonics of the system; however; the control techniques have some disadvantages as large computation time and calculation delays. Therefore, this paper presents the application of a classic discrete-time control model for a three-dimensional space vector pulse width modulation (3D-SVPWM). The proposed control technique enables the UPQC to isolate the load from a harmonic-contaminated power supply and the momentary variations of the signals. At the same time, the current harmonics are eliminated and the power factor of the load is corrected, generating an ideal system at the common connection point. The designed model allows us to quickly implement the control technique as a prototyping system with a low computational cost. The classic discrete-time control has the advantage of obtaining a fixed commutation frequency [32] what for industrial application helps to reduce audible noise, size of electrical equipment, eliminate subharmonics in the output signal, and others. Besides, PID controllers are developed for the series APF, shunt APF, DC bus voltage, DC bus unbalance voltage, and PWM.

The rest of the document is divided into four more sections. Section 2 describes the UPQC in dual topology, defining the detailed models of the series and shunt APFs. Section 3 presents the discrete controllers designed in the frequency domain and the 3D-SVPWM. Section 4 presents the results obtained from the application of the dual UPQC to a three-phase system. Finally, Section 5 presents the conclusions of the document.

2. UPQC in Dual Topology

To model the UPQC, the split capacitor configuration in the DC bus was selected, allowing to develop each three-phase inverter like three independent single-phase inverter. Furthermore, series and shunt APFs were considered in the UPQC model.

2.1. Series Active Power Filter (Series APF)

The simplified circuit in Figure 4 represents the series APF of the UPQC. Additionally to the terms defined in Section 1 for Figure 1, V_{ia}, V_{ib}, and V_{ia} are voltages in the power grid between the series compensator and the network for phases a, b, and c, respectively; C_{sa}, C_{sb}, and C_{sc} are the power grid capacitance of phases a, b, and c, respectively; and i_{fsa}, i_{fsb}, and i_{fsc} are the filtered currents supplied to the load using the series APF. Moreover, Q_1–Q_6 are the duty cycles for the three-phase inverter; V_d^* is a reference for the unbalance voltage between the two DC capacitors; V_B^* is a reference for the DC link voltage; and i_{cs}^* is a reference for the current supplied by the series APF.

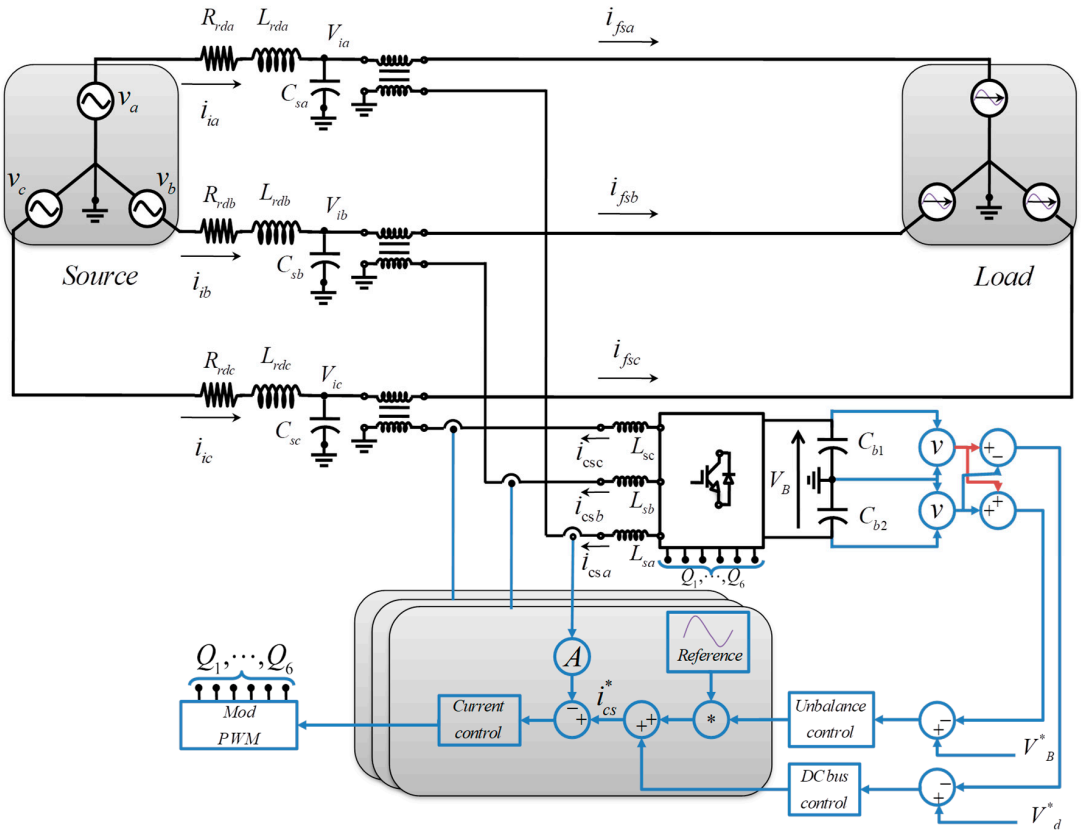


Figure 4. Series active power filter (series APF) for the UPQC in dual topology.

From the control scheme, there are three control loops. The first control loop corresponds to the current in the source side, responsible for controlling independently the current of each phase in the source. The second control loop corresponds to the voltage in the DC bus of the inverter to keep constant the voltage. The third control loop is required because of the DC branch that divides capacitors, and it is used to maintain the same voltage values in capacitors.

The block diagram in Figure 5 represents the control system of the series APF, which illustrates the three control loops previously mentioned only for phase a; this diagram is the same for phases b and c. Herein, $V_B^*(t)$ is the required voltage in the DC bus of the power inverter applied as a reference with positive and negative values, according to the requirements in the capacitors of more or less energy drained through bi-directional inverter. Besides, the term Hv is a voltage sensor gain. Furthermore, inside the "phase A control loop" the term Hi represents the current sensor gain, Vm is the PWM gain,

$Gi(s)$ is the current loop transfer function, and Ki is the current sensor gain ($Ki = 0.44$). Moreover, Hd is the unbalanced voltage sensor gain, Gd represents the unbalanced voltage transfer function, Gv refers to the voltage loop transfer function, Kv is the voltage control attenuation ($Kv = 0.64$), and Kd denotes the unbalanced voltage control attenuation ($Kd = 319$). Finally, the output of the circuit is represented by two voltages: V_d that refers to the unbalance voltage between two DC capacitors and V_B defined as the DC link voltage.

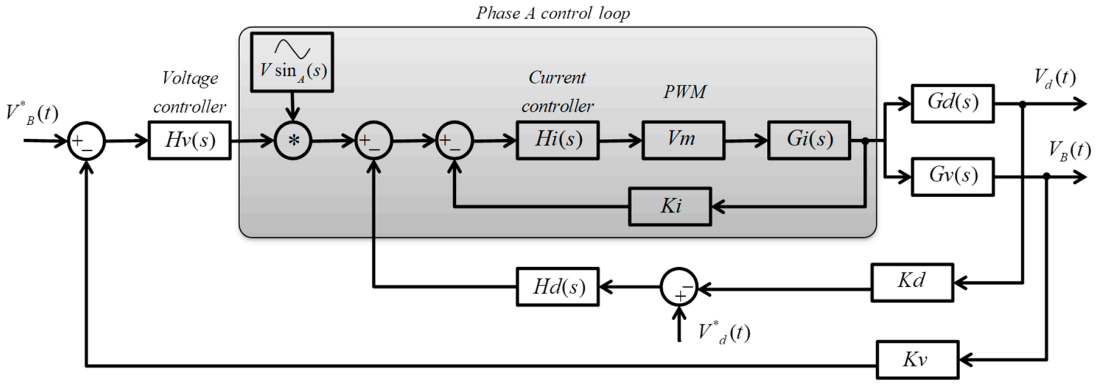


Figure 5. Series APF diagram.

The unbalance voltage is expected to have a small value so it can be neglected. Finally, the current reference is a sinusoidal signal synchronized with the fundamental frequency of the power network, so the load in conjunction with the series APF behaves as a pure resistive load.

The split capacitor configuration has several advantages. From the circuit point of view, a midpoint that allows correcting the unbalanced current of the load. From the modeling point of view, three independent single-phase inverters that allow analyzing the three-phase inverter, as this simplifies the circuit. Hence, the equivalent model of the series APF used in the UPQC is represented in Figure 6; where, Figure 6a presents the single-phase circuit; Figure 6b shows the circuit referred to the primary of the transformer; and finally, Figure 6c displays the final equivalent circuit per phase in which the switching period is much lower than the network frequency. Thus, the terms $V_{rd}(t)$ and $V_0(t)$ are constant in the switching periods.

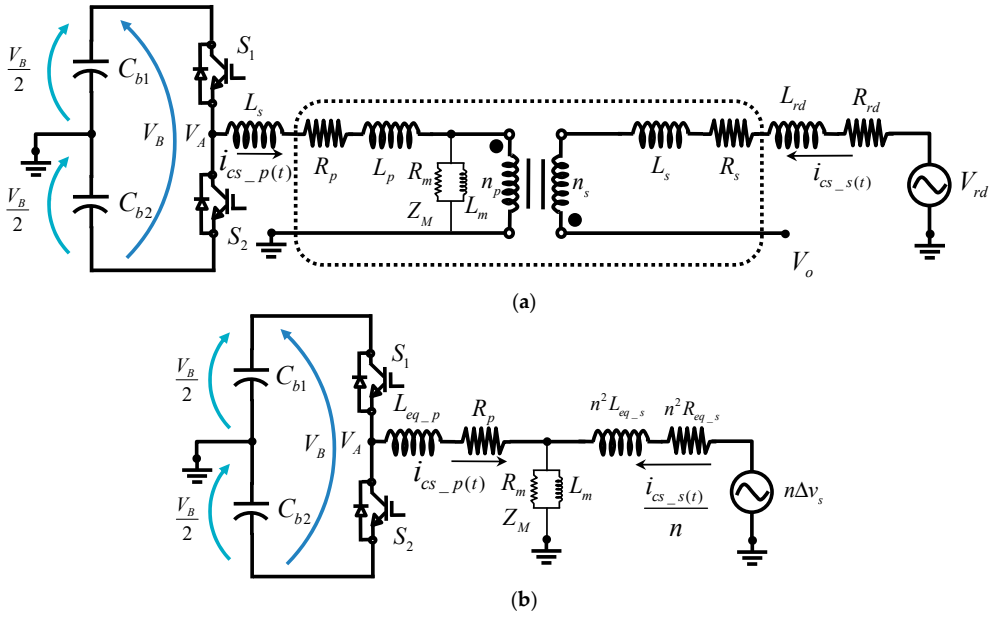


Figure 6. *Cont.*

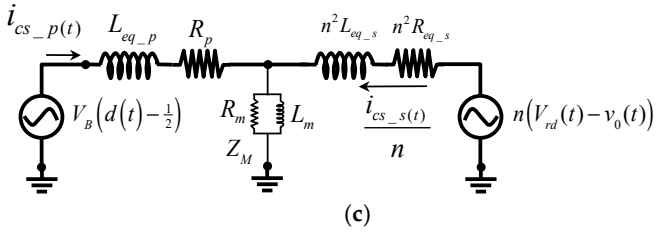


Figure 6. Circuit to model the series APF in the UPQC, (**a**) single-phase circuit, (**b**) circuit referred to the primary of the transformer, and (**c**) equivalent circuit.

The equivalent resistances and inductances in the primary and secondary of the transformer are calculated as described next. Equation (1) obtains the equivalent resistance in the secondary (R_{eq_s}) using the term R_{rd} as the resistance of the power grid and R_s as the secondary scattering resistors of the transformer. Equation (2) obtains the equivalent inductance in the secondary of the transformer (L_{eq_s}), by using the term L_{rd} as the inductance of the power grid and L_s as the secondary scattering inductance of the transformer. Equation (3) represents the output difference voltage in the transformer (Δv_s), calculated as the difference between the power grid network (V_{rd}) and the output voltage (V_0). Equation (4) represents the transformer relation n, calculated using n_p as the number of turns in the primary coil of the transformer and n_s as the number of turns in the secondary coil of the transformer. Finally, Equation (5) is the equivalent inductance in the primary of the transformer (L_{eq_p}), calculated using the terms L_s and L_p defined as the secondary and primary scattering inductances of the transformer, respectively.

$$R_{eq\_s} = R_{rd} + R_s \tag{1}$$

$$L_{eq\_s} = L_{rd} + L_s \tag{2}$$

$$\Delta v_s = V_{rd}(t) - V_0(t) \tag{3}$$

$$n = \frac{n_p}{n_s} = 1 \tag{4}$$

$$L_{eq\_p} = L_{se} + L_p, \tag{5}$$

Additionally, in previous figures the term R_p is the primary scattering resistors of the transformer, C_{b1} and C_{b1} are the corresponding capacitors in the DC bus, V_A is the PWM voltage in the output of the inverters. Furthermore, i_{cs_p} and i_{cs_s} are the currents of the shunt APF in the primary and secondary of the transformer, respectively. Finally, Z_M is the magnetizing impedance of the transformer model that considers R_m as the magnetizing resistance and L_m as the magnetizing inductance.

The DC-AC inverter can be modeled as a half-bridge controlled by the two switches S_1 and S_2, obtaining an output voltage V_A [33,34], as shown in Figure 7; where d is the duty cycle and T_s is the commutation period.

For the final equivalent circuit presented in Figure 6c, the state-space model is obtained as expressed in Equation (6):

$$\begin{bmatrix} V_B D(s) \\ 0 \end{bmatrix} = \begin{bmatrix} R_p + SL_{eq\_p} + Z_M & Z_M \\ Z_M & SL_{eq\_s} + R_{eq\_s} + Z_M \end{bmatrix} \begin{bmatrix} I_{cs\_p}(s) \\ I_{cs\_s}(s) \end{bmatrix} \tag{6}$$

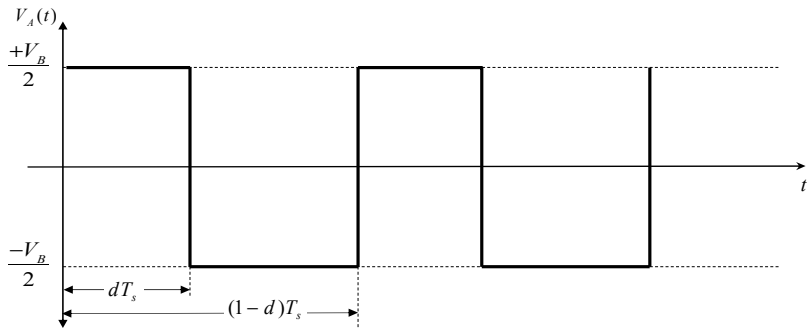


Figure 7. Representation of the switching period.

From the state-space model, the current loop transfer function $Gi(s)$, which relates the output current of the inverter $I_{cs\_p}(s)$ with the duty cycle of the circuit breakers $D(s)$, a new expression is obtained as shown in Equation (7):

$$Gi(s) = \frac{I_{cs\_p}(s)}{D(s)} = V_B * \frac{s^2k_1 + sk_2 + k_3}{s^3k_4 + s^2k_5 + sk_6 + k_7}, \tag{7}$$

where k_1–k_7 are terms that represent the equivalent resistances and inductances of the circuit and they are defined follows:

$$\begin{gathered} k_1 = L_{eq_s}L_m \\ k_2 = R_{eq_s}R_m \\ k_3 = R_{eq_s}L_m + R_mL_m + R_mL_{eq_s} \\ k_4 = L_{eq_p}L_{eq_s}L_m \\ k_5 = R_pL_{eq_s}L_m + L_{eq_p}L_{eq_s}R_m + L_{eq_p}R_{eq_s}L_m + R_mL_mL_{eq_p} + R_mL_mL_{eq_s} \\ k_6 = R_pL_{eq_s}R_m + L_mR_pR_{eq_s} + R_pR_mL_m + L_{eq_p}R_{eq_s}R_m + R_mL_mR_{eq_s} \\ k_7 = R_pR_{eq\_s}R_m. \end{gathered}$$

Herein, R_m is the magnetizing resistance, L_m is the magnetizing inductance, R_{eq_s} is the equivalent resistance in the secondary of the transformer, L_{eq_s} is the equivalent inductance in the secondary of the transformer, L_{eq_p} is the equivalent inductance in the primary of the transformer, and R_p is the primary scattering resistors of the transformer.

To represent the equivalent voltage in the DC bus ($\overline{V}_B$), the bidirectional three-phase inverter will be considered as a current source ($\bar{I}_{eq}$) that feeds the circuit in the DC side of the same inverter, and with a current value equal to the average value of the load current $\bar{I}_b$, as illustrated in Figure 8.

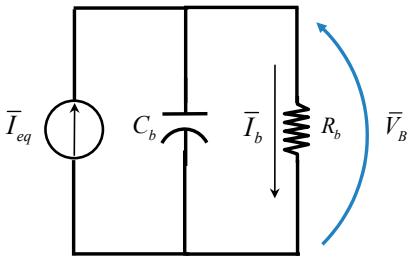


Figure 8. Equivalent circuit of the DC bus.

In the circuit of Figure 8, a fictitious load R_b has been included because the capacitor (C_b) does not consume active power, so it would not make sense to represent an average current $\bar{I}_{eq}$ charging the capacitor in the steady-state. However, the power is considered null from the point of view of the power grid frequency, but not so for the switching frequency of the inverter switches, in which case if

an instantaneous power consumption is required to maintain the desired average voltage between DC bus terminals and for which this fictitious load R_b is included.

By means of power balance analysis, the power supplied to the DC bus (P_b), is given by the sum of the power per phase in the inverter (P_{cs}), according to Equation (8).

$$P_b = \bar{I}_{eq}\overline{V}_B = 3P_{cs} \ . \tag{8}$$

Writing the input power P_{cs} as a function of the peak of the network voltage V_{rd_pk} and the peak of the fundamental current I_{cs_pk}; then, the expression in Equation (9) is obtained:

$$P_{cs} = \frac{nV_{rd\_pk}}{\sqrt{2}}\frac{I_{cs\_pk}}{\sqrt{2}} = \frac{nV_{rd\_pk}I_{cs\_pk}}{2}. \tag{9}$$

By replacing P_{cs} of Equation (9) in Equation (8) and then clearing $\bar{I}_{eq}$, the expression presented in Equation (10) is obtained:

$$\bar{I}_{eq} = \frac{3}{2}\frac{nV_{rd\_pk}I_{cs\_pk}}{\overline{V}_B}. \tag{10}$$

The average current $\bar{I}_{eq}$ can be considered equal to the effective current circulating through the impedance of the equivalent circuit of the DC bus, so the equivalent voltage in the DC bus $\overline{V}_B$ is obtained as shown in Equation (11):

$$\overline{V}_B(s) = \frac{\bar{I}_{eq}}{\frac{1}{R_b} + sC_b}. \tag{11}$$

With Equations (10) and (11), the transfer function that relates the voltage in the DC bus to the peak of the input current in the inverter is obtained, as shown in Equation (12). For the voltage mesh, this current is seen as a low-frequency component, for this reason, it is considered as a sinusoidal component, in the following way:

$$Gv(s) = \frac{\overline{V}_B(s)}{I_{cs\_pk}(s)} = \frac{3}{2}\frac{nV_{rd\_pk}}{\overline{V}_B}\frac{1}{\frac{1}{R_b} + sC_b}. \tag{12}$$

For the analysis performed in this research, the resistance R_b was assumed on the impedance of the DC side with the inverter as an active filter. Then, it can be assumed that $R_b \to \infty$, as no current flows through it. Finally, the transfer function can be represented as shown in Equation (13).

$$Gv(s) = \frac{3}{2}\frac{V_{rd\_pk}}{\overline{V}_B}\frac{n}{sC_b}. \tag{13}$$

The unbalanced grid transfer function must relate the voltage difference in the capacitors to the current injected from the bidirectional inverter to them. In the circuit of Figure 9, the current through the switches S_1 and S_2 have been represented as two current sources feeding each capacitor, where the midpoint allows each phase to be analyzed separately.

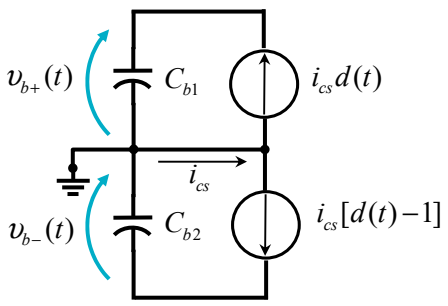


Figure 9. Equivalent circuit of the current loop.

From Figure 9, and considering the switching functions as complementary, Equations (14) and (15) are defined as follows:

$$i_{cs}(\mathrm{t}) * d(t) = C_{b1}\frac{dv_{b+}(t)}{dt} \tag{14}$$

$$i_{cs}(\mathrm{t}) * [d(t) - 1] = C_{b2}\frac{dv_{b-}(t)}{dt}. \tag{15}$$

After transforming and applying zero initial conditions to Equations (14) and (15), then Equations (16) and (17) are obtained.

$$V_{b+}(s) = \frac{D}{sC_{b1}}I_{cs}(s) \tag{16}$$

$$V_{b-}(s) = \frac{(D-1)}{sC_{b2}}I_{cs}(s). \tag{17}$$

Knowing that $C_B = \frac{C_{b1}}{2} = \frac{C_{b2}}{2}$, or that $2C_B = C_{b1} = C_{b2}$, then the expression in Equation (18) is obtained:

$$\frac{V_{b+}(s) - V_{b-}(s)}{I_{cs}(s)} = \frac{1}{2sC_B}. \tag{18}$$

This is the transfer function of the represented single-phase system. Thus, if the contribution of each phase is considered, the transfer function of the unbalance voltage loop is given by Equation (19):

$$Gd(s) = \frac{V_{b+}(s) - V_{b-}(s)}{I_{cs}(s)} = \frac{3}{2sC_B}. \tag{19}$$

2.2. Shunt Active Power Filter (Shunt APF)

The shunt APF of the dual UPQC aims to provide the load with a sinusoidal voltage of low harmonic distortion and maintain the balance on the three-phase system. The APF consists of a bi-directional power electronics inverter to which a capacitor must be added in parallel to the output.

The transfer function of the shunt APF relates the output voltage with the duty cycle (see Figure 10). Additionally to the parameters defined previously for Figures 1 and 4, the term V_{oa}, V_{ob}, and V_{oc} are the voltage in the load of the power grid; i_{fsa}, i_{fsb}, and i_{fsc} are the filtered currents supplied to the load using the series APF; C_{pa}, C_{pb}, and C_{pc} are the capacitors of the shunt APF; Q_1-Q_6 are the duty cycle for three-phase inverter; and v_{ref} is a voltage reference for the voltage controller.

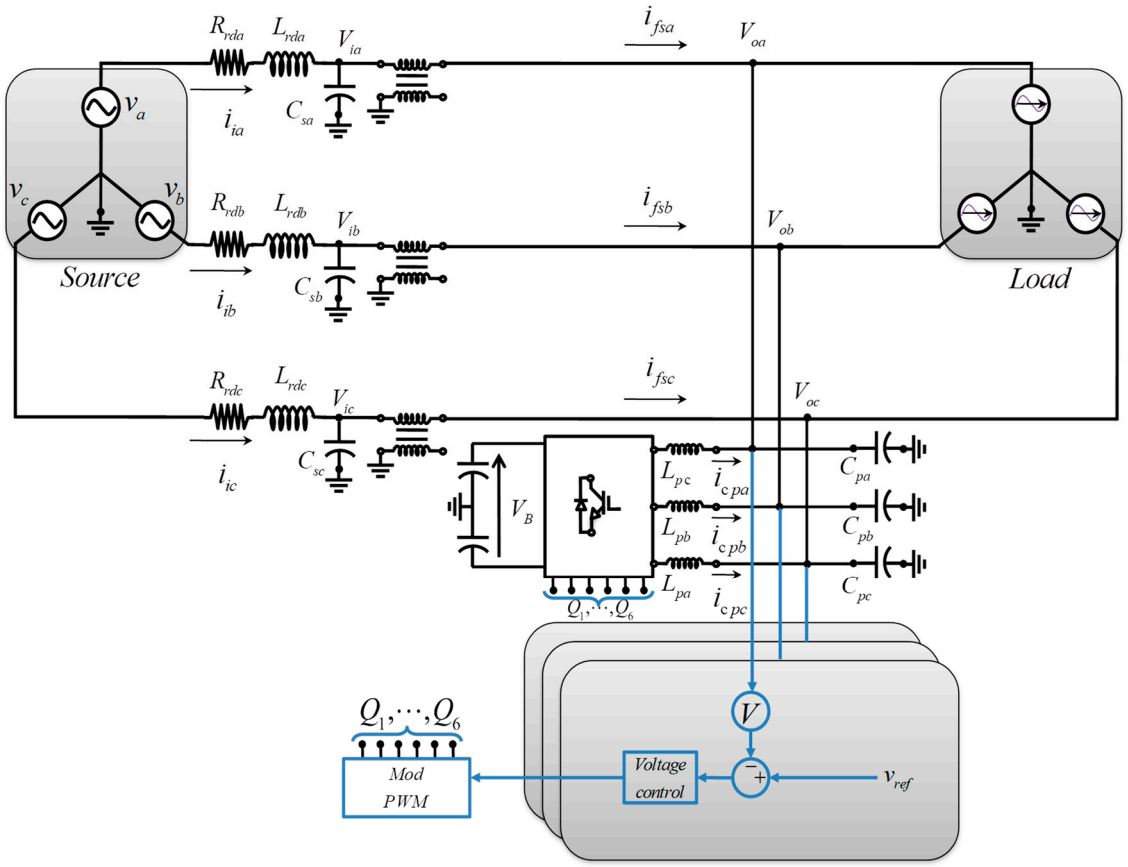


Figure 10. Shunt active power filter (shunt APF) for the UPQC in dual topology.

The shunt inverter can be modeled as a single-phase equivalent by the split capacitor characteristic on the DC bus. The circuit in Figure 11 illustrates the equivalent circuit for voltage plant analysis.

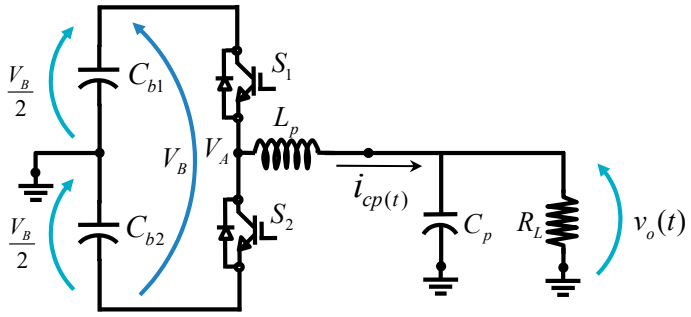


Figure 11. Single-phase circuit of the shunt APF.

From the circuit presented in Figure 11, an equivalent circuit can be obtained as shown in Figure 12, for which the transfer function is given by Equation (20).

$$Gp(s) = \frac{V_o(s)}{D(s)} = \frac{V_B}{L_p C_p} \frac{1}{s^2 + \left(\frac{1}{C_p R_L}\right)s + \frac{1}{L_p C_p}}. \tag{20}$$

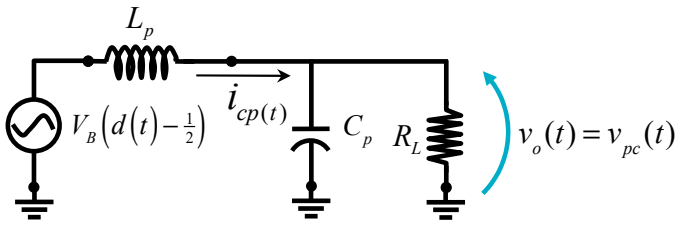


Figure 12. Shunt active power filter single-phase equivalent circuit.

3. Design of Controllers

From the extracted models, the transfer functions for the control can be projected. The controllers will be projected by the method of frequency response for each of the loops of the plant. In order to project controllers, it is necessary to know the frequency response of the system without a controller. Afterward, the frequency and gain requirements of each control actions are determined from the responses. When the transfer function of the controller has been projected, then it is discretized.

3.1. Current, DC bus, and DC bus Unbalance Controllers

The current controller of the series APF is given by Equation (21), using zero-order hold technique on the input; where the term *Hi* represents the current sensor gain.

$$H_i(z) = \frac{2.735z - 2.629}{z^2 - 1.73z + 0.73}. \tag{21}$$

Starting from the proportional action, the controller will raise the zero-cross frequency of the system to the required 5 kHz (one-quarter of the switching frequency); the integral action reduces the error in the system and also improves the rejection of disturbances. However, the speed of response is reduced with respect to the proportional action. A pole is added to the PI controller to reduce high-frequency noise. The bode diagram in Figure 13 presents the result of applying the controller to the system.

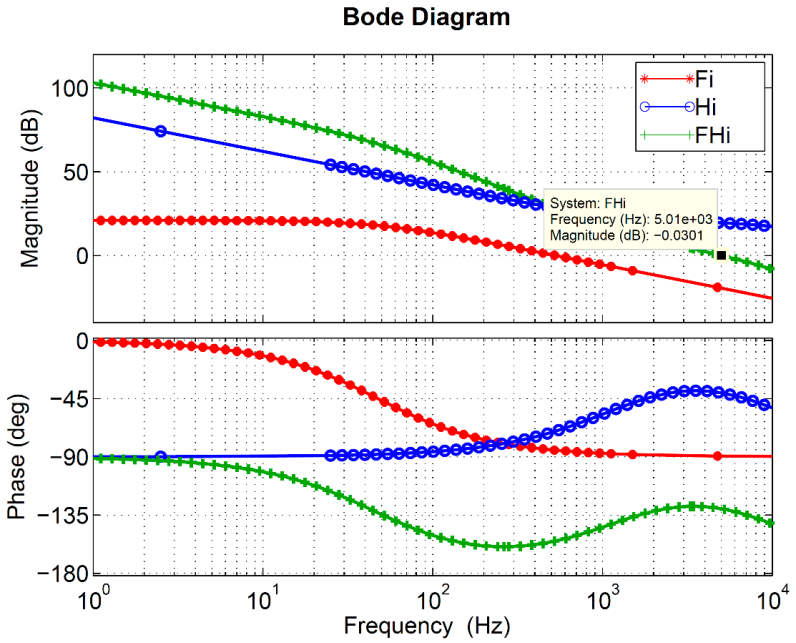


Figure 13. Frequency response in the current loop with and without the controller.

The DC bus controller and DC bus unbalance controllers are described in Equations (22) and (23); where H_{DC} is the transfer function of the DC bus controller and H_{unb} is the transfer function of the DC bus unbalance controller.

$$H_{DC}(z) = \frac{15.2 * 10^{-3}z - 15.2 * 10^{-3}}{z^2 - 1.99z + 0.995} \tag{22}$$

$$H_{unb}(z) = 0.12. \tag{23}$$

The DC bus voltage unbalance control is a proportional gain chosen from the maximum current value required to compensate unbalances during transient events, starting from the maximum time in which it must be compensated.

3.2. Voltage Controller

The control strategy selected for the shunt APF consists of PID actions with two poles and two zeros. One of the poles is placed at the source to reduce the speed error and improve noise rejection, the second is positioned at a higher frequency to attenuate high-frequency noise. On the other hand, the zeros are positioned at the same frequency of the poles of the power plant to reduce their effects. The discretized transfer function of the voltage controller in the shunt APF (H_v) is given by Equation (24).

$$H_v(z) = \frac{30.37z^2 - 59.63z + 29.31}{z^2 - z + 1.12 * 10^{-3}}. \tag{24}$$

3.3. Three Dimensional Space Vector Pulse Width Modulation (3D-SVPWM)

This work proposes the application of a vector modulator for a three-phase split capacitor inverter called three-dimensional three-branch space vector pulse width modulation (3D-3B-SVPWM) [35]. This algorithm has been applied to three-phase inverters switched in parallel connection to compensate current. However, SVPWM modulation is a technique for sinusoidal references; in the case of shunt current compensators, the reference to be generated by the inverter is highly distorted, so the results obtained from the application of this technique do not make sense to give similar results to the SPWM sinusoidal modulation.

The simulation scheme of the controllers is illustrated in Figure 14. In the case of the current controller, the voltage error has been converted to the synchronous reference frame. This transformation allows the use of a single controller for the three phases in the power grid, controlling only the phase components, because the quadrature and zero components are null.

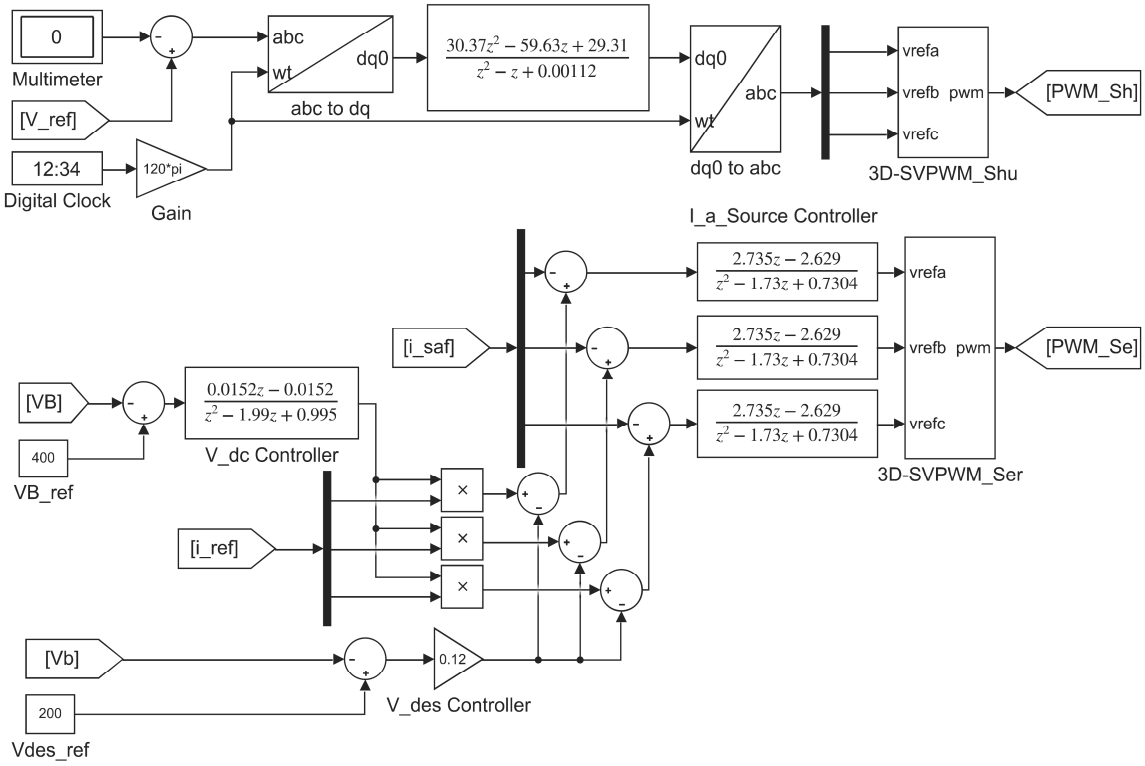


Figure 14. Controllers simulation scheme.

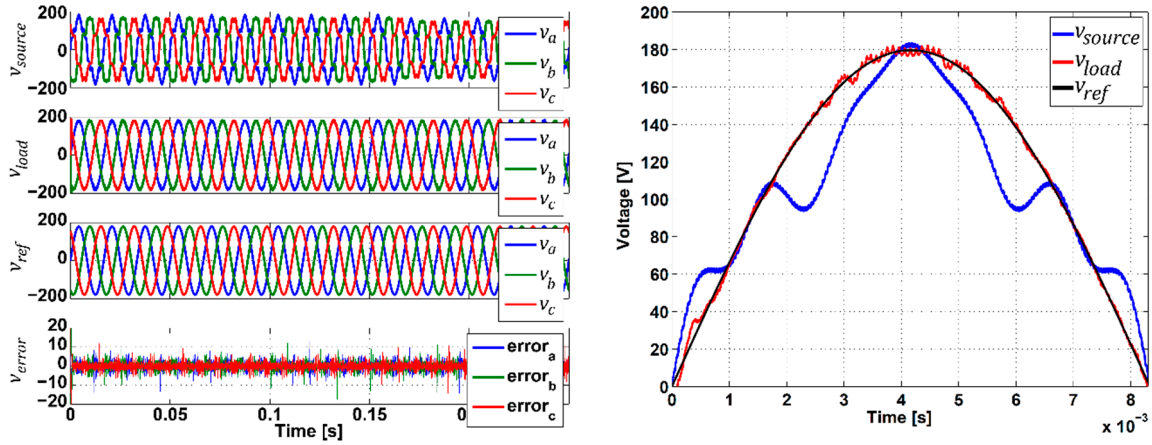
4. Results

The parameters of the transformers, compensators, and the network are given in Table 1. Some of these terms were defined for equations and figures used in Sections 1 and 2 as parameters per phase of the circuit (a, b, and c); however, in this table those parameters and values are given per phase, omitting the letters. The power is supplied by a 110 V_{RMS} three-phase source that is set unbalanced and contaminated by harmonics. Besides, at a certain time during the simulation, a voltage drop of 10% is generated in the three phases of the power source to verify the behavior of the compensator under this type of transient event. The load considered four AC-DC converters, three full-wave rectifiers to generate unbalances in the load, and a full-wave rectifier controlled by six thyristors to handle delays in the current.

Table 1. Parameters of the transformers, compensators, and the network.

Name	Parameter	Value
Inductance of the series APF	L_s	650 µH
Switching frequency	Fs	20 kHz
DC link voltage	V_B	400 V
PWM voltage gain	V_m	0.091 V
Power grid resistance	R_{rd}	0.04 Ω
Power grid inductance	L_{rd}	107 µH
Power grid capacitance	C_s	1 µF
Shunt inductance	L_p	1.2 mH
Shunt and series resistance	$R_p = R_s$	0.44 Ω
Magnetizing resistance of the transformer	R_m	104 Ω
Magnetizing inductance of the transformer	L_m	104 H
Secondary equivalent resistance	R_{eq_s}	0.48 Ω
DC bus total capacitance	C_B	3 mF
Secondary equivalent inductance	L_{eq_s}	757 µH
Primary equivalent inductance	L_{eq_p}	1.85 mH

Figure 15a shows the voltage with harmonic distortion in the source, the voltage improved in the load, the voltage reference, and the voltage error of the circuit with the proposed solution. Figure 15b shows the enlargement of the waves referred to the voltages measured in the source and in the load, compared to the voltage reference.

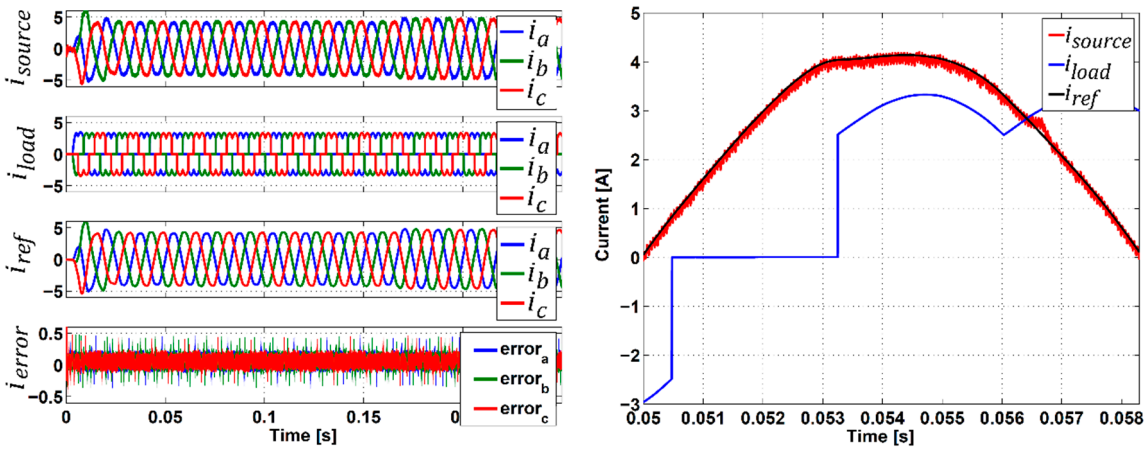


(**a**) (**b**)

Figure 15. Voltage compensation results: (**a**) three-phase signals and (**b**) zoom of the waveform.

A frequency analysis of the voltage waveforms measured in the source and in the load illustrates the improvement in the harmonic distortion index THDv (in percentage) after the action of the voltage compensator. These results show that the value changes from 14.97% to 1.43%, when applying the compensation, demonstrating the effectiveness of the method. When observing the enlargement of the waves, where an approach has been made to one of the positive half-cycles, the results show that the error between the voltage in the load and the voltage reference is very small, thus achieving a good performance of the compensator. The small ripple in the waveform of the voltage in the load (V_{Load}) is given by the commutation of the inverters.

Figure 16a shows the current in the source and in the load, the current reference, and the current error. This figure shows that the current in the load is highly contaminated by harmonics and with a delay of 30° with respect to the current in the source, thus acting as a non-linear inductive load. The error between the current in the source and the current reference is less than 5% except for small peaks due to the switching frequency. The detail of the current compensation is better appreciated in the waveforms of Figure 16b, where a mid-period approach of the waves has been made. It can be seen that the total harmonic distortion in current (THDi) goes from a value of 30.94% to 3.37% taking into account the switching frequency of 20 kHz; and if only the harmonic 50 (3 kHz) is considered, the value of THDi = 2.50%, which is half of the maximum value recommended by the IEEE 519 standard.



(**a**) (**b**)

Figure 16. Current compensation results: (**a**) three-phase signals and (**b**) zoom of the waveform.

At 0.01 s, the current of the source presents a transient behavior when the UPQC is connected, due to the requirements of the capacitor in the DC bus to reach its reference voltage. Besides, in Figure 15a a voltage sag has been generated from the source at 0.17 s in order to verify the performance of the UPQC to compensate for the voltage drop. Finally, Figure 16 shows that at the same time the UPQC requires more current from the power source.

5. Conclusions

The continuous model of the UPQC was developed and the classic discrete control model was applied in a three-phase power grid with harmonic distortion and unbalance in the power source. The load of the system was composed of a power electronic AC/DC inverter with phase control to generate current harmonic distortion and low power factor by displacement. The results showed that the series and shunt APFs worked to give good efficiency in filtering the voltage harmonics of the source and the currents harmonics of the load, and to improve the power factor. There is a high-frequency signal in the compensated signals that is due to the switching of the power elements of the UPQC, due to its magnitude; the high-frequency component does not represent a problem for the system and that ends up being filtered by the impedance of the power grid.

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