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A Cost-Effective Solution to Improving the Electrical Performance of Metal Contacting Interfaces in IC System under Temperature-Humidity Environment

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Abstract: Temperature-humidity (TH) induced failure mechanism (FM) of metal contacting interfaces in integrated circuit (IC) systems has played a significant role in system reliability issues. This paper focuses on central processing unit (CPU)/motherboard interfaces and studies several factors that are believed to have a great impact on TH performance. They include: Enabling load, surface finish quality, and contacting area. Test vehicles (TVs) of Clarkdale package and of Ibex peak motherboard were designed to measure low level contact resistance (LLCR) for catching any failure. Several sets of design of experiments (DOE) were conducted on 85 °C/85% relative humidity and test results were analyzed. A proposal that correlates asperity spots and contact tip design with contact resistance was proposed and thus a cost-effective solution for improving electrical performance under TH was deduced. The proposal has proven to be reasonably effective in practice.

Keywords: system reliability; Temperature-Humidity; induced failure mechanism; asperity; constriction; contacting area; contact resistance; contact tip design

1. Introduction and Motivation

Today, integrated circuit (IC) systems can be found in the majority of electrical devices, from industrial to agricultural areas, from military to civilian use, and from underwater to outer-space fields. They have become an indispensable part of our lives. There are many metal-to-metal contacting surfaces in IC systems, including interfaces between area array packages/printed circuit boards, peripheral component interconnect (PCI) slots, dual-inline-memory modules (DIMM) slots, etc. Under high humidity and high temperatures, foreign materials such as corrosion products may form on those contacting surfaces and grow with time, resulting in electrical failure. This type of failure is typically referred to as temperature–humidity induced failure. Since hot humid environments are commonly used conditions, temperature–humidity (TH) induced failure mechanism (FM) is a factor that must be considered in the product validation process.

There are many circumstances where TH induced FM is actually the first FM to appear and it therefore becomes the gating FM of the system's reliability. For example, the author has come across many scenarios where TH induced FM turned out to be the most vulnerable one among all possible

FMs in the product development stage. Great efforts were made to improve the electrical performance under TH. These experiences sparked the author's interest in studying the mechanism of TH failure, the modulating factors that affect the performance, the possible solutions, etc.

This paper focuses on central processing unit (CPU)/motherboard interfaces. The context of study is based on test vehicles (TVs) of Clarkdale processor package and of Ibex peak motherboard. First, the TH failures that occur during the product development is described and the FM is investigated. Secondly, some main modulating factors are identified, together with supporting theories and possible solutions. Additionally, a new methodology that correlates asperity spots and contact tip design with contact resistance is proposed. Thirdly, the design of experiments (DOEs) of modulating factors are described and test results are analyzed. It turns out that one of the modulating factors has no significant effect on the performance, while the other two modulating factors have a significant effect on the performance. Further, one of the effective solutions is typical but costly, and the other one has proven to be reasonably efficient and cost effective.

Some experiments conducted give a general idea of the proposal that is put forward by the first author when she was working at Intel Corporation. Some other experiments are conducted and a more systematic model is proposed by the authors at Shenyang Jianzhu University with the support from the Overseas Expertise Introduction Project for Discipline Innovation. However, for clarity of the thought process, the experiments and the proposal are not described in chronological order, but in logical sequence.

The main contents of study are as follows:

1. Introduce the test device and low level contact resistance (LLCR) measurement method.
2. Develop enabling load TH test plan and perform TH test program.
3. Analyze TH test results and investigate TH failure mechanism.
4. Identify main modulating factors for TH failure mechanism.
5. Propose a new methodology which correlates contact tip design with contact resistance.
6. Describe TH DOE of modulating factors and discuss the test results.

2. Experiment Setup

2.1. TV Description

TV of Ibex peak motherboard: The enabling test board (ETB) was designed to simulate the performance of the Ibex peak motherboard in order to be used in an in-circuit test (ICT), and to evaluate the interface land grid array (LGA) socket's electrical, mechanical, and reliability performance. The nominal dimension of the ETB and interface socket was 6.315 inches $\times$ 5.58 inches and 42.5 mm $\times$ 42.5 mm, respectively. There were two sets of tooling holes: One set with three tooling holes was designed to simulate the load applied to the substrate steps, and the other set with four tooling holes was to simulate the heat sink load. The schematic representation and picture of ETB are shown in Figures 1 and 2, respectively.

TV of Clarkdale processor package: The nominal dimension of the substrate size was 37.5 mm $\times$ 37.5 mm, as shown in Figure 3. There were two-step loads that were applied to the ears of integrated heat spreader (IHS). There was a heat sink (HS) load on the top surface of the IHS. The loads on the IHS are shown in Figure 4.

Figure 1. Schematic representation.

Figure 2. Enabling Test Board.

Figure 3. Schematic representation of the substrate size.

Figure 4. Load on integrated heat spreader.

2.2. Measurement of LLCR

Daisy chain layout: The pattern was designed by following these strategies: (a) The whole array shall be divided into small chains to get reasonably accurate measurement; (b) the high risk of shorting shall be caught; and (c) the high risk of opening or high resistance shall be caught. There were 119 chains in total. The schematic representation of the daisy chain layout is shown in Figure 5.

Figure 5. Schematic representation of daisy chain layout.

The four-wire measurement technique was adopted: The electrical measurement instrument provided two separate circuits. One was a precision current source to deliver the test current. The other was a precision voltmeter circuit to measure the voltage drop between the desired points. Thus, the total resistance was able to be calculated based on the measured current and voltage from each chain. The total resistance per chain (R_{Total}) measured thus included the resistance of package and package shorting bars, contact LLCRs, solder balls, and motherboard and motherboard shorting bars, as shown in Figure 6.

Figure 6. Schematic representation of the four-wire measurement technique. LGA: Land grid array.

Parasitic resistance: LGA TVs were flush-mounted directly to the motherboard fixtures in order to measure the average parasitic resistance ($\bar{R}_{\text{parasitic}}$), which included the resistance of the package, the motherboard, and solder balls. Thirty samples were used for statistical reasons.

The value of low-level contact resistance R_{LLCR} can be calculated by:

$$R_{\text{LLCR}} = \frac{R_{\text{Total}} - \bar{R}_{\text{parasitic}}}{N_{\text{Chain}}} \quad (1)$$

where N_{Chain} is the number of contacts within the chain.

3. Test Details

3.1. Enabling Load TH Test Legs

3.1.1. Risk Assessment

As part of the validation process, in order to understand if the product would remain in good function until its guarantee period, a bunch of accelerated tests were performed, among which accelerated TH tests, typically testing at 85 °C/85% relative humidity, were adopted to simulate the system performance in hot and humid environments. Such TH tests could either be tested until failure to understand the products' capability or be tested until the equivalent warranty time requirement T_{rep} . The T_{rep} in this paper was chosen as 408 h, based on the calculations using Peck's acceleration model [1].

TH tests were conducted at two extreme load ends. One was conducted under minimum external load, correlating with the risk of insufficient contact force to penetrate through the foreign material that may form during the product life. The other one was conducted under maximum external load, correlating with the risk of contact wiping all the way to the solder resist opening (SRO), which was due to the interaction with SRO, resulting in the reduction of contact force and still ending up with insufficient contact force to penetrate through the foreign material that may form during the product life.

3.1.2. DOE Description

Leg1: The leg with max external load was labeled as leg1 and was tested under 135 lb step load with 50 lb HS load based on the design guide.

Leg2: The leg with min external load was labeled as leg2 and was tested under 60 lb step load. Twelve units were tested for each leg.

3.1.3. Success Criterion

The average part resistance per design $R_{partaverage}$ (hereinafter referred to as part average resistance) was required to be less than 19 milliohms per design guide, as shown in Equation (2).

$$R_{partaverage} = \frac{\sum (N_{Chain} \times R_{LLCR})}{\sum N_{Chain}} \leq 19m\Omega \quad (2)$$

The maximum allowable chain LLCR resistance $R_{LLCR-max}$ (hereinafter referred to as max chain LLCR limit) was defined by assuming that only one contact reaches a maximum of 100 milliohms, while the rest of the contacts within this chain all meet the part average requirement. Thus, the $R_{LLCR-max}$ requirement per chain could be calculated by Equation (3) and is dependent on the number of contacts within the chain, as shown in Table 1.

$$R_{LLCR-max} = \frac{(N - 1) \times R_{partaverage} + 100}{N_{Chain}} \quad (3)$$

Table 1. $R_{LLCR-max}$ per chain.

# of Contacts per Chain	Max Chain LLCR Limit
2	59.50
4	39.25
6	32.50
8	29.12
10	27.10
12	25.75
14	24.78

3.1.4. Enabling Load TH Test Results

The data of R_{LLCR} for the tested units were collected at three different readouts (RO), 192 h, 312 h, and 408 h. They were plotted in the variability chart below, together with R_{LLCR} at time zero (before units being put into chamber), as shown in Figure 7. In the chart, the resistances greater than 100 milliohms were not plotted for scale consideration. It can be seen that the TH tests under high load was good; the TH tests at time zero were good; but for the TH tests under min load, there were many failures. Additionally, note that at each RO, failed units (no more than three) were taken out for failure analysis (FA). These failed units did not go back to chamber to next ROs. This is why the resistances appear to get better with time for the min load case (since some failed units were taken out).

Figure 7. Variability chart for low-level contact resistance.

The measured LLCRs were plotted against the daisy chain layout (as illustrated in Figure 5) for each unit and at each RO. Figure 8 below shows two selected R_{LLCR} maps. The selected maps were from the units at 192 h RO under min load leg. These two units were taken out for FA due to failures.

Figure 8. Selected R_{LLCR} map of failing units. (a) Failing unit No 1; (b) failing unit No 2.

The LLCR map of a unit from another TH leg is shown in Figure 9. The test setup for this leg was the same as the previous min load leg, but the socket supplier was different. This unit was not used for any comparison in this paper, but only to demonstrate that this TH failure could happen at the inner perimeter and could exhibit as an open failure.

Figure 9. Example of temperature-humidity (TH) open failure.

From the LLCR distribution, it can be seen that there was no obvious pattern in terms of the failure location distribution. With step load on the North and South sides, the contact force distribution map is shown in Figure 10 (Note: NFORC3 divided by 10,000 is in gram force). With the package warped upwards in the center, the contact force had a tendency to decrease from the exterior perimeter to the

interior perimeter, whereas the failures were found both around the outer perimeter and the inner perimeter. These were typical TH failure symptoms.

Figure 10. Contact force distribution under step load only.

3.1.5. Failure Analysis and Root Cause Failure

X-sections showed that all contacts remained on pads (even for the open failure chain), as shown in Figure 11. Scanning electron microscope (SEM) showed that, for the pad from failing chains, there was the presence of nickel oxides. For functional chains, there were mostly no signs of other elements besides Au, as shown in Figure 12. Even during the appearance of other elements for good chains, the contact forces were believed to be strong enough to penetrate through the foreign materials in order to make good contact with the pads.

Figure 11. X-section of a failed chain.

Figure 12. Scanning electron microscope (SEM) of pad from failing chain and good chain.

TH FM: The metallurgical surface finish for the package and the contacts was typically electroless nickel and immersion gold plating (ENIG). A typical industry process for ENIG [2] is such that the immersion gold (IG) is deposited on top of electroless Ni (EN), which is on top of the Cu layer. EN serves as a diffusion barrier for copper metallization, whereas IG acts as a protective overcoat to protect Ni from oxidation. Since a gold atom is much larger than a nickel atom, the room between nickel atoms may not be fully filled in by gold atoms, thus small voids are formed during the displacement reaction. The presence of gold pores exposed the nickel underneath, and under high relative humidity environment, diffusion brings nickel ions to the surface, resulting in the formation of nickel oxidation, as shown in Figure 13. At time zero, it was expected that even though the entire contact surface was not all gas tight, the contacting spots could be considered gas tight [3]. Therefore, good LLCR was always established at T0. With time passing, corrosion was accelerated under high relative humidity and stress relaxation occurred. The mating locations could change due to stress relaxation, and this was how corrosion products got between the original contacting spots. In hot humid environments, the high temperature also adversely impacted electrical performance. It not only sped up corrosion, but also caused more severe stress relaxation. In extreme severity, oxidation in TH could lead to electrical failures, such as high resistances or electrical opens.

Figure 13. Schematic of the TH failure mechanism in electroless nickel and immersion gold plating (ENIG) surface finish.

Note that, besides the nickel oxidation type of corrosion, there were some other commonly seen TH FMs, such as fretting, that caused the wear of the coating material on the contact surface, then exposed the EN layer, or even exposed the base material of the Cu layer, resulting in the decrease of the electrical contact performance, such as wiping, dust, industrial corrosive gases, etc.

3.2. Some Main Modulators of TH FM on Electrical Contact

3.2.1. Main Modulators

Based on the TH FM, several main modulators that are believed to have great impacts on TH performance, and can be implemented through relatively non-complicated design applications, were identified. They were:

1. **Enabling load:** The theory is that the possibility of contacting points penetrating through the films/the foreign materials is a function of contact force. Increasing contact force increases the possibility of forming air tight contacting points. Thus, the solution was to increase the enabling load.
2. **Surface finish thickness:** The theory is that increasing the IG plating thickness helps reduce the number of the pores, and thus mitigate the formation of nickel oxidation in order to improve the resistance to TH. The solution was to increase the Au thickness.

3. **Contacting area:** The theory is that increasing contacting area helps improve the contacting efficiency, since larger contacting areas may provide more space for more gas tight contacting points. Note: The larger the contacting area, the smaller the contact pressure. Thus, in order for the contacting area to play a positive role, a minimum contact force was required. The solution was to increase the contacting area with the minimum contact force requirement being met.

The first proposed solution of increasing the enabling load and the second proposed solution of increasing Au plating thickness were more straightforward, but the third one of increasing contacting area was tricky. It had to do with the detailed design of a contact tip. Additionally, the nominal contacting area was not equal to the actual contacting area since not all points within the nominal area were gas tight. It has been a challenge to investigate these gas tight points. There are some papers on this topic. The single-spot first-order model for constriction resistance established by Holm [4] has received international recognition. On the basis of this model, many researchers have studied the influence of many factors such as multi-contact spot, temperature, arc, film, time, etc. A variety of complex theoretical models of contact resistance have been established. Malucci simulated the contact performance by considering the combined effects of surface degradation and interface motion on the change of contact resistance, and proposed a third level multi-spot constriction model [5,6]. Han and Kim studied the effect of normal forces on fretting corrosion in tin-coated electrical contacts, and found that there is a linear relationship between the normal forces and the threshold displacement amplitude [7]. Park and Lee developed an empirical equation to account for the impact of fretting frequency or temperature, and proposed failure-time variation sensitivity for each variable [8]. However, very few studied how to quantifiably correlate the tip design with contact electrical performance. This paper proposed a new methodology to correlate contact tip design with contact resistance.

3.2.2. The Model to Correlate Contact Tip Design with Contact Resistance

Key Parameters

Regarding contact tip design, there were two key parameters identified: Contact tip radius r_t and contacting width W_a , as shown in Figure 14. They are critical to function tip design dimensions that are directly related to contacting area. In this paper, for the simplicity of study, the focus was on the influence of r_t .

Figure 14. Contacting width and contact tip radius.

Asperity Spots

The contacting interfaces of two conductors, no matter how well the surface was processed, were always uneven on the micro level. If the hardness of the material was infinite, the contact force does not cause any deformation. There will be, at most, three contact spots for surface-to-surface contact; two contact spots for line to surface contact; and one contact spot for sphere to surface contact. However, in

reality, the material will deform. Thus, the number of contact spots will increase with the increase of the deformation, until the summation of the forces provided by point contacts is balanced by the external force, and the increase of contact spots stops, as shown in Figure 15. These spots, which actually touch, are called asperity spots (hereinafter referred to as a-spots), and are the ones that can actually conduct electricity.

Figure 15. Real contact state. (a) Nominal contact region and conduct electricity spots; (b) Contacting status under equilibrium.

Assumptions

1. As illustrated in Figure 16, the tip along the contact length direction was viewed as a spherical ball with a radius of r_t and with all a-spots on top of it.
2. The pad was viewed as an ideal spherical surface with an infinite radius of curvature or an ideal plane.
3. The a-spots were treated as a bunch of small balls, all with a radius of r_a (hereinafter referred to as a-spot ball radius).
4. The contacting interface of an a-spot was a circle, with a radius of a (hereinafter referred to as a-spot contacting radius), as shown in Figure 17.
5. When the touch just began, there was only one a-spot touching pad. As the actual contacting area was small, the force on the contact point was large, resulting in deforming the 1st a-spot. With the increasing deformation of the 1st a-spot, the 2nd a-spot started touching the pad. Assuming that, when the 2nd a-spot came into play, the 1st a-spot was still in elastic region. Thus, the classical Hertz formula could be used to calculate the elastic deformation. Additionally, this procedure was repeated for all other a-spots until the supporting forces from a-spots could balance the external force.
6. The number of a-spots was n , and the distance between a-spots was much greater than a-spot contacting radius a , and therefore any interference from the adjacent a-spots could be ignored.

As a result, the a-spot contacting radius could be derived with the classic Hertz Formula [9], which was expressed as:

$$a = \sqrt[3]{\frac{3}{4}P_a r_a \left(\frac{1 - v_1^2}{E_1} + \frac{1 - v_2^2}{E_2} \right)} \quad (4)$$

P_a is the contact force on an a-spot; r_a is a-spot ball radius; and V_1, V_2, E_1, E_2 , are Poisson's ratio and Young's modulus of the two conductor materials, respectively. As both contacting surfaces were Au plated, we have:

$$v_1 = v_2 = v_{Au} = 0.42 \quad (5)$$

$$E_1 = E_2 = E \quad (6)$$

$$a = 1.073 \sqrt[3]{\frac{P_a r_a}{E}} \quad (7)$$

Figure 16. Schematic representation of a contact tip design.

Figure 17. Schematic representation of contact state of an a-spot.

LLCR

As the actual contact interface was a group of a-spots, resistance increased as the path of current flow was elongated when current passes through a-spots. Such resistance was defined as constriction resistance R_c , as depicted in Figure 18.

Figure 18. Schematic representation of constriction resistance.

For the round contacting interface, there was the following relationship:

$$R_{ci} = \frac{\rho}{2a} \quad (8)$$

R_{ci} is the constriction resistance of an a-spot (hereinafter referred to as a-spot constriction resistance); a is a-spot contacting radius; and ρ is resistivity of the contacting material, which is also the resistivity of Au.

Contact resistance consists of bulk resistance, constriction resistance, and film resistance, as shown in Figure 19. A-spot constriction resistances R_{ci} are in parallel at the interface. Thus:

$$R_c = \frac{R_{ci}}{n} \quad (9)$$

Figure 19. Schematic representation of contact resistance.

R_c is the total constriction resistance at the interface (hereinafter referred to as interface constriction resistance). Assuming that film resistance is infinite and its conductive effect could be ignored, then R_c represented the resistance of the interface.

Assuming there were n a-spots in total, Equations (10)–(12) could be:

$$A = \sum_i^n \pi a_i^2 = n\pi a^2 \quad (10)$$

$$a = \sqrt{\frac{A}{n\pi}} \quad (11)$$

$$R_c = \frac{R_{ci}}{n} = \frac{1}{n} \frac{\rho}{2a} = \frac{1}{\sqrt{n}} \left(\frac{\rho}{2} \sqrt{\frac{\pi}{A}} \right) = \frac{1}{\sqrt{n}} \left(\frac{\rho}{2\bar{a}} \right) = \frac{R_{c0}}{\sqrt{n}} \quad (12)$$

A is the total true contacting area; $\bar{a} = \sqrt{\frac{A}{\pi}}$ is the contacting radius of a single point contact with equivalent contacting area of A (hereinafter referred to as equivalent contacting radius); and R_{c0} is the constriction resistance of a single point contact with equivalent contacting area of A (hereinafter referred to as equivalent constriction resistance).

R_c was in series with the bulk resistance of the contact R_{bc} and the bulk resistance of the pad R_{bp} . Thus:

$$R_T = R_{bc} + R_{bp} + R_c \quad (13)$$

$$R_T - R_{bp} = LLCR = R_{bc} + R_c \quad (14)$$

R_T is the total single contact resistance from single contact measurement. When deducting the bulk resistance of the pad, we got LLCR because the pad resistance was a portion of the parasitic resistance, as illustrated in Section 2.2. Thus:

$$LLCR - R_{bc} = R_c = \frac{R_{ci}}{n} = \frac{R_{c0}}{\sqrt{n}} \quad (15)$$

Contact Tip Radius Design

In order to connect the contact tip design with LLCR, the tip radius r_t was chosen to be the same as the radius of the single point contact (hereinafter also referred to as equivalent ball radius) that created equivalent constriction resistance R_{c0} . The following relationship was thus established:

$$R_{c0} = \frac{\rho}{2a} = \frac{\rho}{2 \times 1.073 \sqrt[3]{\frac{Pr_t}{E}}} \quad (16)$$

$$r_t = \frac{\rho^3 E}{9.883 \times P \times R_{c0}^3} = \frac{\rho^3 E}{9.883 \times P \times \left(\frac{\sqrt{n} \times R_{ci}}{n} \right)^3} \quad (17)$$

$P = \sum_{i=1}^n P_a$ is the total contact force. In this paper, the minimum required contact force of 15 gramforce, based on design guide was chosen. R_{ci} is a-spot constriction resistance; n is the total number of a-spots; ρ is the resistivity of Au; and E is Young's modulus of Au.

Design criterion: For a conservative design, no contact resistance was allowed to exceed the requirement of average part resistance $R_{partaverage}$.

$$LLCR \leq R_{partaverage} \quad (18)$$

Besides, to account for the impact from factors not considered in this paper, such as the influence of surrounding a-spots, the influence of the deviations of assumptions from real situations, etc., a safety coefficient of $\zeta = 0.7$ was assumed.

$$LLCR - R_{bc} = R_c \leq \zeta \times (R_{partaverage} - R_{bc}) \quad (19)$$

Bulk resistance of contact R_{bc} was dependent on the contact design. However, once the big picture of a contact was determined, R_{bc} was pretty much settled. Minor modifications on a tip design did not have much effect on its value. In this case, R_{bc} was rounded up to 9 milliohms per design guides. Thus, there is the following relationship.

$$R_c \leq 0.7 \times (19 - 9) = 7 \text{ milliohms} \quad (20)$$

In hot and humid environments, nickel oxides or other foreign materials develop and can cover the a-spots, making a-spots lose their good electrical conductivity. As more and more a-spots are covered by foreign materials, the interface constriction resistance and LLCR keeps increasing, leading to high resistances or open failures in severe cases. Assuming that only one good a-spot was left, the following relationship was observed:

$$R_c = R_{ci} = \frac{\rho}{2 \times 1.073 \sqrt[3]{\frac{P_a r_a}{E}}} = \frac{\rho}{2 \times 1.073 \sqrt[3]{\frac{15 \text{ gf} \times r_a}{nE}}} \leq 7 \text{ milliohms} \quad (21)$$

The resistivity of Au was taken as $2.35 \times 10^{-8} \Omega \cdot \text{m}$. The Young modulus of Au was taken as 790 Mpa. Thus:

$$\frac{r_a}{n} \geq 0.002016305 \text{ mm} \quad (22)$$

For different values of n , a requirement of a-spot ball radius r_a could be obtained. From r_a , a-spot contacting radius a could be derived, then a-spot constriction resistance R_{ci} could be derived, then equivalent constriction resistance R_{c0} could be derived, and then contact tip radius r_t (also referred to as equivalent ball radius) could be derived. Therefore, for a given n , a minimum design requirement of contact tip radius could be calculated, based on the requirements of LLCRC. This minimum tip radius design requirement was called $r_{t \min}$. The maximum tip radius requirement came from the contact wiping tolerance analysis, which was not in the scope of discussion of this paper, and is just denoted with $r_{t \max}$. Therefore, the tip radius fell in the range of:

$$r_{t \min} \leq r_t \leq r_{t \max} \quad (23)$$

As far as n is concerned, it has to do with the surface finish technology, but a very small value and a large value are both not realistic. For a small n , say just one a-spot, once it is covered by foreign material, the contact will fail. For a large n , the a-spot force will be small and the ability to penetrate through foreign materials will be compromised. Additionally, it may require a large tip that exceeds $r_{t \max}$.

As illustrated in Table 2, the recommended design of tip radius r_t was determined. A value smaller than the recommended r_t was no good; a value larger than the recommended r_t may have reasonable risk controls. For example, if there are 10 a-spots: $0.064 \text{ mm} \leq r_t \leq r_{t \max}$; if there are 15 a-spots: $0.117 \text{ mm} \leq r_t \leq r_{t \max}$; and if there are 20 a-spots: $0.180 \text{ mm} \leq r_t \leq r_{t \max}$.

Table 2. Design parameters with different n.

(a)									
n = 1				n = 10					
A-Spot Ball Radius r_a (mm) $\geq$	A-Spot Ball Radius r_a (m)	A-Spot Contacting Radius a (m)	Resistance $R_c =$ $R_{ci} = R_{co}$ (milliohm)	A-Spot Contacting Radius a_i (m)	A-Spot Constriction Resistance R_{ci} (milliohm)	Equivalent Constriction Resistance R_{co} (milliohm)	Interface Constriction Resistance R_c (milliohm)	Contact Tip Radius (Equivalent Ball Radius) $r_{t \min}$ (mm) $\geq$	
0.0020	2.016×10^{-6}	1.679×10^{-6}	7.000						
0.0202	2.016×10^{-5}	3.616×10^{-6}	3.249	1.679×10^{-6}	7.000	2.214	0.700	0.064	
0.0302	3.024×10^{-5}	4.140×10^{-6}	2.838	1.921×10^{-6}	6.115	1.934	0.612	0.096	
0.0403	4.033×10^{-5}	4.556×10^{-6}	2.579	2.115×10^{-6}	5.556	1.757	0.556	0.128	
(b)									
n = 15					n = 20				
A-Spot Contacting Radius a_i (m)	A-Spot Constriction Resistance R_{ci} (milliohm)	Equivalent Constriction Resistance R_{co} (milliohm)	Interface Constriction Resistance R_c (milliohm)	Contact Tip Radius (Equivalent Ball Radius) $r_{t \min}$ (mm) $\geq$	A-Spot Contacting Radius a_i (m)	A-Spot Constriction Resistance R_{ci} (milliohm)	Equivalent Constriction Resistance R_{co} (milliohm)	Interface Constriction Resistance R_c (milliohm)	Contact Tip Radius (Equivalent Ball Radius) $r_{t \min}$ (mm) $\geq$
1.679×10^{-6}	7.000	1.807	0.467	0.117					
1.848×10^{-6}	6.360	1.642	0.424	0.156	1.679×10^{-6}	7.000	1.565	0.350	0.180

3.3. TH DOEs of Modulating Factors

3.3.1. TH DOEs

From Leg1 and Leg2 described previously, it can be seen that increasing the enabling load can be a solution since, even though the min load leg (leg2) failed, the high load leg (leg1) passed.

The focus of this portion was on studying the second main modulator (surface finish thickness) and the third main modulator (contacting area). Note: The contacting area was calculated as $r_t \times W_a$.

Leg 3: Smaller nominal contacting area leg with thinner Au thickness. The change in contacting area was reflected on the contact side by purposely designing a smaller contact tip. The contacting area was 0.007 mm^2 . The Au thickness was controlled on the package side. The average pad Au thickness was $0.38 \text{ }\mu\text{m}$.

Leg 4: Larger nominal contacting area leg with thinner Au thickness. The change in contacting area was reflected on the contact side by purposely designing a larger contact tip. The contacting area was 0.0221 mm^2 . The Au thickness was controlled on the package side. The average pad Au thickness was $0.38 \text{ }\mu\text{m}$.

Leg 5: Larger nominal contacting area leg with thicker Au thickness. The change in contacting area was reflected on the contact side by purposely designing a larger contact tip. The contacting area was 0.0221 mm^2 . The Au thickness was controlled on the package side. The average pad Au thickness was $0.43 \text{ }\mu\text{m}$.

3.3.2. Test Results

Here, $R_{partaverage}$ was used for analyses to get rid of the uncertainty caused by LLCr variation. Since it is typical that under TH, chain LLCr maps do not have an obvious pattern. Thus, only analyses based on part average resistance could tell if the improvement is a random kick in or a true stable help. Three ROs were collected at 192 h, 312 h, and 408 h. They were plotted in the variability chart, as shown in Figure 20. It can be seen from the comparison of leg3 vs. leg4 and leg3 vs. leg5 that the part average was constantly improved by about 1.5 milliohms to 2 milliohms. If compared with the design requirement of $R_{partaverage}$ of 19 milliohms, the improvement was about 7.9%–10.5%. There were more tests conducted to confirm the improvement by implementing the proposed design, even though they were not described in this paper, the improvement on part average resistance always held.

Figure 20. Variability chart for part average.

There is not much difference between leg 4 and leg5. The increase in Au thickness seems to make a negligible difference. It is believed that it is because the typical industrial plating process is reasonably mature already.

Besides, it is noticeable from Figure 20 that the resistance, in general, appears to get slightly better with time, especially from 192 h RO to 312 h RO. The author's suspect that this is due to the system creep and contact relaxation that result in contact force redistribution and contacting status

readjustment. Additionally, typically creep and relaxation happen faster within the early stage, which may explain why the drop in resistance is more obvious from 192 h RO to 312 h RO. More study is needed in future work to further investigate this phenomenon.

3.4. Solutions

From the previous experiments and the theoretical analyses, it is believed that both the enabling load and contacting area play important roles in improving the electrical performance under TH for area array packages/printed circuit board interfaces. To get better TH performance, increasing the enabling load helps, and increasing the contacting area (with a minimum contact force requirement being met) also helps.

There are relationships between metallurgical surface finish and key tip design parameters. Larger contacting areas are able to provide more space for more gas tight contacting points. When the contact force meets the minimum requirement, increasing contacting area actually helps improve the contacting efficiency by giving full play to the potential of metallurgical surface finish. Additionally, with more gas tight contacting points, the possibility of all a-spots being covered by foreign materials under TH is less. This paper proposed a design optimization methodology to correlate tip radius with asperity spots and contact resistance requirements. The proposal proved to be efficient.

Increasing the enabling load is the typical industrial solution, but it leads to extra cost in loading mechanism design, and in printed circuit boards design, etc. For instance, in order to get to higher load, a thicker backing plate and/or a thicker loading plate is needed. The extra material to be used can result in huge costs when it comes to high volume manufacturing. Besides, with a higher enabling load, it is very likely that extra effort is needed to accommodate for the risk due to creep on the maximum load end. More seating plane areas may be needed. This can result in less pin count, and needless to say, it is not desirable.

Thus, in industrial application, the design strategy proposed in this paper shall be a reasonable first step to take in order to optimize the electrical performance under TH and to save cost. If this route is insufficient, other solutions such as increasing the enabling load may come in as a second step.

4. Conclusions

A methodology that correlates asperity spots and contact tip design with contact resistance is proposed and proved to significantly improve the electrical performance for area array packages/printed circuit boards interfaces. With such a design implemented, a reduction in part average resistance of 1.5 milliohms to 2 milliohms, or an improvement of 7.9%–10.5% (in comparison with $R_{partaverage}$ requirement), has been seen in the Clarkdale and Ibex peak platform.

Both increasing contacting area and increasing enabling load proved to be able to effectively improve the electrical performance under hot and humid environments, but increasing Au thickness does not seem to help much. Increasing the enabling load is a typical solution, but it is costly. Increasing contacting area with the proposed methodology is a cost-effective solution and is a reasonable first step to take in industrial practice.

5. Future Work

It is interesting to observe a decrease in resistance with time in general, and the drop is more obvious in the early stage. The authors suspect the observation has to do with system creep and contact relaxation [10]. These will be investigated in the future.

Besides, microprocessors are known with consuming huge power that can lead to local hot spots. These hot spots are formed due to high current flow and poor contacts [11]. Hot and humid environment will have an adverse effect on contacting quality. Poor contacts, in turn, lead to more local hot spots and to a higher probability of physical failures. Thus, adding the impact of power consumption and heat dissipation into the study shall be a very critical and interesting topic as well.

Furthermore, the design criterion for tip width has not been established. This will be illustrated in future work.

Some other factors such as the influence of wiping and fretting are also worth looking into [12].

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