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All-Sputtering, High-Transparency, Good-Stability Coplanar Top-Gate Thin Film Transistors

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Abstract: In this work, transparent, stable coplanar top-gate thin film transistors (TFTs) with an active layer of neodymium-doped indium oxide and zinc oxide (Nd-IZO) were successfully fabricated on a glass substrate by all sputtering processes. The devices with a post-annealing temperature of 400 °C exhibited good electrical performances with a saturation mobility (μ_{sat}) of 4.25 $cm^2 \cdot V^{-1} \cdot S^{-1}$, I_{on}/I_{off} ratio about 10^6, V_{th} of −0.97 V and SS about 0.34 V/decade. Furthermore, the devices exhibited excellent negative and positive bias stability (NBS, PBS) of only a ΔV_{th} shift of about −0.04 V and 0.05 V after 1 h, respectively. In addition, the devices showed high transparency about 96% over the visible-light region of 400–700 nm, which indicates a great potential in transparent displays.

Keywords: thin film transistors; stability; top-gate; Nd-IZO

1. Introduction

Amorphous oxide semiconductors (AOS) have attracted significant attention due to their superior advantages such as high mobility, high transparency, good uniformity and low processing temperature [1,2]. As an alternative material for amorphous silicon (a-Si) and low temperature poly silicon (LTPS), AOS faces potential application in active matrix (AM) flat-panel displays (FPDs) [3]. Although AOS has numerous promising properties in dark conditions (without illumination), its bias stress-induced instability is still a critical issue [4]. In general, TFTs for driving unit must keep stable over time as a minor V_{th} shift would change the brightness of an individual pixel and would cause display nonuniformity. Traditional bottom gate TFTs show a large V_{th} shift under bias due to a donor effect of charged chemisorbed H_2O or O_2 molecules in the back-channel region [5]. Therefore, a passivation layer is essential for preventing the active layer from experiencing the ambient impact [6]. However, top-gate structure TFTs have attracted lots of attention with the merits of being self-passivated and compatible with the AMOLED process [7,8]. Jeong et al. have reported top-gate InGaZnO thin film transistors with Al_2O_3 and Al_2O_3/SiN_X gate dielectrics and found larger degradation in devices with a SiN_X interfacial layer due to the trapped charge located at energetically shallower states [9]. Lin et al. have reported top-gate staggered IGZO TFTs by adopting the SiO_X/SiN_X bilayer gate-insulator stack, and finally integrated the devices into a working OLED panel [10]. Work by Fakhri et.al reported ozone based atomic layer deposition at low temperature for fabricating

top-gate dielectric, and the resulting devices showed outstanding stability vs bias stress due to its self-encapsulation [11].

According to our previous study, bottom gate TFTs with Nd-IZO active layer on polyimide (PI) substrate were fabricated and it showed large V_{th} shifts under PBS/NBS [12]. As we know, sputtering technique is a convenient and efficient method for large area fabrication. Here we report an all sputtering way to fabricate high transparency, good stability top-gate metal oxide thin film transistors. The devices exhibited excellent negative/positive bias stability due to isolating with the atmosphere. But the negative/positive bias stability under illumination (NBIS, PBIS) still shifted −2.3 V and −0.78 V due to the trapping of the photogenerated holes in the gate insulator and/or at the insulator/channel interface. Moreover, the transparency exceeds 96% over the visible-light region of 400–700 nm, which indicates a great potential in transparent displays.

2. Experimental

The structure of all-sputtered TFTs is illustrated in Figure 1, in which the fabricated process is given as follows. First, a thickness of 30 nm SiO_2 buffer layer was deposited on the pre-cleaned glass by radio frequency (RF) sputtering that isolates the H_2O or O_2 to penetrate the functional layers, which is critical to the sensitive channel layer as adsorbed H_2O or O_2 could induce electrical properties that are variational. Second, an active layer about 7 nm was deposited on SiO_2 buffer layer with the condition of 5 mTorr, 80 W and O_2/Ar ratio of about 5%. This was followed by an annealing process at 300 °C for 30 min in ambient for eliminating part of defects in the semiconductor. Then, the source/drain electrodes were prepared using an ITO target by DC sputtering. The channel length (L) and width (W) were 160 and 635 μm, respectively. Next, a 350-nm-thick Al_2O_3 layer was deposited by RF sputtering as an insulator layer. Subsequently, top-gate electrode was defined in the same way with S/D electrodes. All the layers were patterned by shadow masks and the sputtering conditions of functional layers were listed in Table 1. For reducing the plasma bombardment on the active layer [13], the devices were post-annealed at 200 °C, 300 °C and 400 °C for 1 h, respectively.

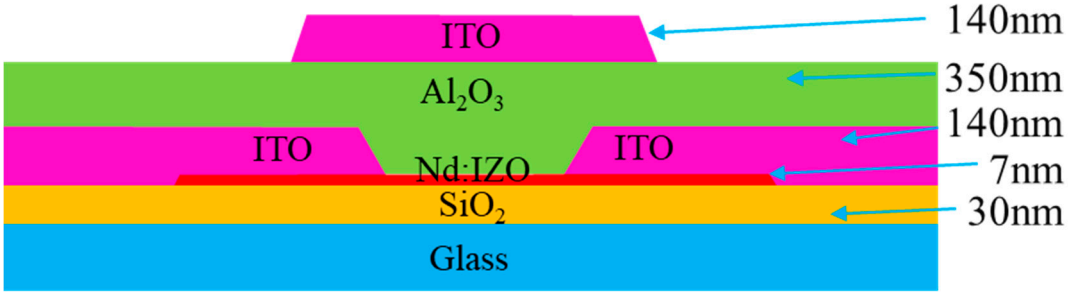

Figure 1. The cross-sectional image of the all sputtered Nd:IZO TFT with coplanar top-gate configuration.

Table 1. The detailed sputtering conditions of each functional layer.

Layer	Pressure (mTorr)	Power (W)	O_2/Ar ratio (%)	Time (s)	Thickness (nm)
SiO_2	1	100	0	900	30
Nd-IZO	5	80	5	300	7
ITO	5	100	0	600	140
Al_2O_3	1	120	0	12600	350
ITO	5	100	0	600	140

All the functional layers were deposited by using the physics vapor deposition equipment (Kurt Lesker). The electrical characteristics of TFTs were measured using a semiconductor parameter analyzer (Agilent 4155C) in ambient condition at room temperature. TEM with an energy dispersive X-ray spectrometer (EDS) was used to analyze the distribution of elements. The optical characteristics

of fabricated devices were investigated by an Ultraviolet spectrophotometer (SHIMADZU UV2600, SHIMADZU, Tokyo, Japan).

3. Results and Discussion

Figure 2 exhibits the characteristics of corresponding TFTs after post-annealed at 400 °C. Figure 2a shows the I_D-V_D output curves of the coplanar top-gate TFTs, it exhibited good gate-control properties. But there is no gate control for the devices with no post-annealing or post-annealed at 200 °C and 300 °C as shown in Figure 3. This may be due to serious ion damage on the active layer when depositing the insulator layer and the damage could not yet be recovered at a lower annealing temperature. The transfer characteristics (I_D-V_G) of fabricated devices are given in Figure 2b. The transfer curves were measured with V_G swept from negative to positive with negligible gate leakage (<10^{-10}A as shown in the inset of Figure 2b). This enables a mobility of 4.25 cm^2 V^{-1} s^{-1}, on/off current ratio exceeds 10^6, V_{th} of −0.97 V and subthreshold swing (SS) about 0.34 V/decade. No obvious hysteresis was observed, which indicates less electron traps at the interfaces between active layer and dielectric [14], and the remarkably improved storage stability of the device.

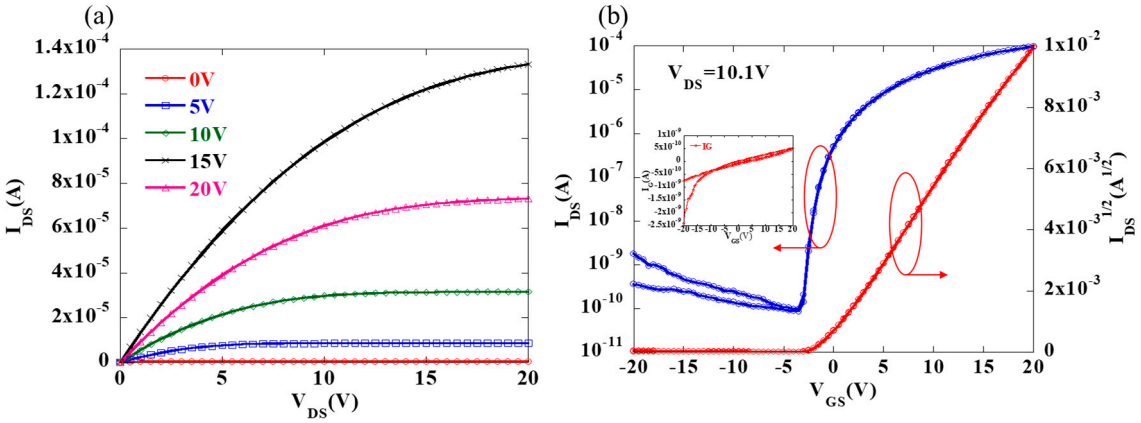

Figure 2. (**a**) Output characteristic curves (I_{DS}-V_{DS}) and (**b**) transfer characteristic curve (I_{DS}-V_{GS}) of manufactured coplanar top-gate Nd-IZO TFTs. V_{GS} is varied from −20 to 20 V with V_{DS} = 10.1 V, and the inset was the gate leakage current.

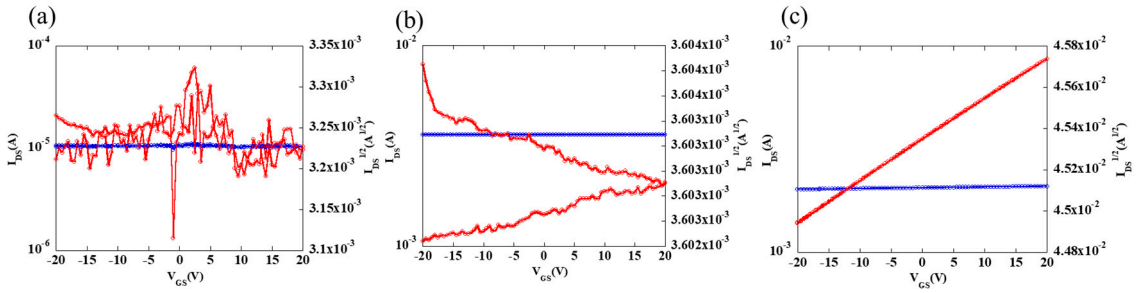

Figure 3. Transfer characteristic curve (I_{DS}-V_{GS}) of manufactured coplanar top gate Nd-IZO TFTs under different post-annealing temperatures (**a**) without annealing, (**b**) 200 °C (**c**) 300 °C. V_{GS} is varied from −20 to 20 V with V_{DS} = 10.1 V.

Figure 4 shows BF STEM image together with the elemental distribution detected by EDS in the channel region of the coplanar top-gate Nd-IZO TFTs. The STEM result shows that the Nd-IZO film was continuous and compact sandwiched between the buffer layer and insulating layer, suggesting good thickness uniformity and no obvious intermixing between adjacent layers. It is known that clear interface and uniform thin films help devices to achieve high performance [15]. The small amount of Nd acted as a superior oxygen binder required to suppress the formation of oxygen vacancies

and control the carrier concentration can be ascribed to its low electronegativity (~1.1) and stronger bonding strength of Nd-O (703 kJ/mol) [16,17].

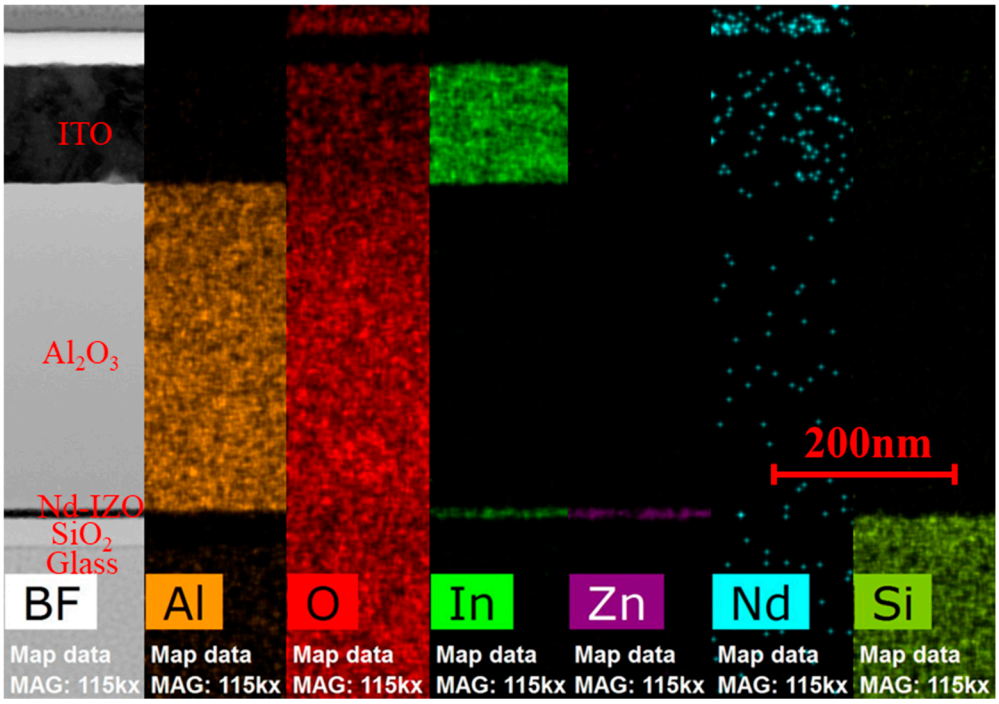

Figure 4. BF STEM image together with the elemental distribution (from left to right: Al, O, In, Zn, Nd, Si) detected by EDS.

The electrical stability of the coplanar top-gate TFTs was investigated by stressing a prolonged combined gate/drain bias on the device. The devices were stressed under the following conditions: V_{GS} = ±20 V, V_{DS} = 10 V and applied V_{GS} = ±10 V, which was applied for 3600 s. Figure 5 shows electrical stability under NBS, PBS, NBIS and PBIS, respectively. The corresponding V_{th} is shown in Table 2, where the all sputtered coplanar top-gate TFTs exhibited a slight negative NBS shift and positive PBS shift. The V_{th} shift after 1 h under NBS and PBS was only −0.04 V and 0.05 V, respectively. This is remarkable for a TFT device. It is also noted that there was no significant degradation in saturation mobility and SS, indicating that no new defects were created when applying gate bias and self-passivated property could effectively prevent the semiconductor from ambience interaction, which is very critical for the stability of devices. The declined I_{off} in NBS indicated that the devices tend to be more stable after negative bias was applied for one hour. However, once illumination was introduced, the transfer curves exhibited a −0.78 V shift after 1 h under positive V_G stress with illumination. Moreover, larger negative shifts in V_{th} were observed under negative V_G stress with illumination. The most plausible degradation mechanism of the Nd-IZO TFTs under NBIS conditions was suspected to be photogenerated holes being trapped at the gate insulator and/or insulator/channel interface, and there was no hole recombination with the redundant photogenerated electrons once the gate bias was withdrawn, finally resulting in a negative shift of V_{th} [18]. As reported by other groups, the NBIS could be improved by a high-pressure annealing process [19], long-time annealing process [20], ozone treatment [21] or by adding a buffer layer [22].

Figure 6a shows the time dependence of ΔV_{th} for Nd-IZO TFTs under NBS, PBS, NBIS and PBIS at room temperature. It can be clearly seen that the NBS and PBS curves are approximately two straight lines. The NBIS and PBIS decline a lot from the original values. Figure 6b shows the transmittances of all sputtered coplanar top-gate TFTs of SiO_2/Nd-IZO/ITO/Al_2O_3/ITO on glass substrate with different post-annealing temperatures. The transmittance increased with the increasing of the post-annealing temperature, which may due to the high annealing temperature prompting more

transparency of ITO [23]. Moreover, the maximum transparency exceeded 96% under a wide visible light region, which indicates a great potential for transparent displays.

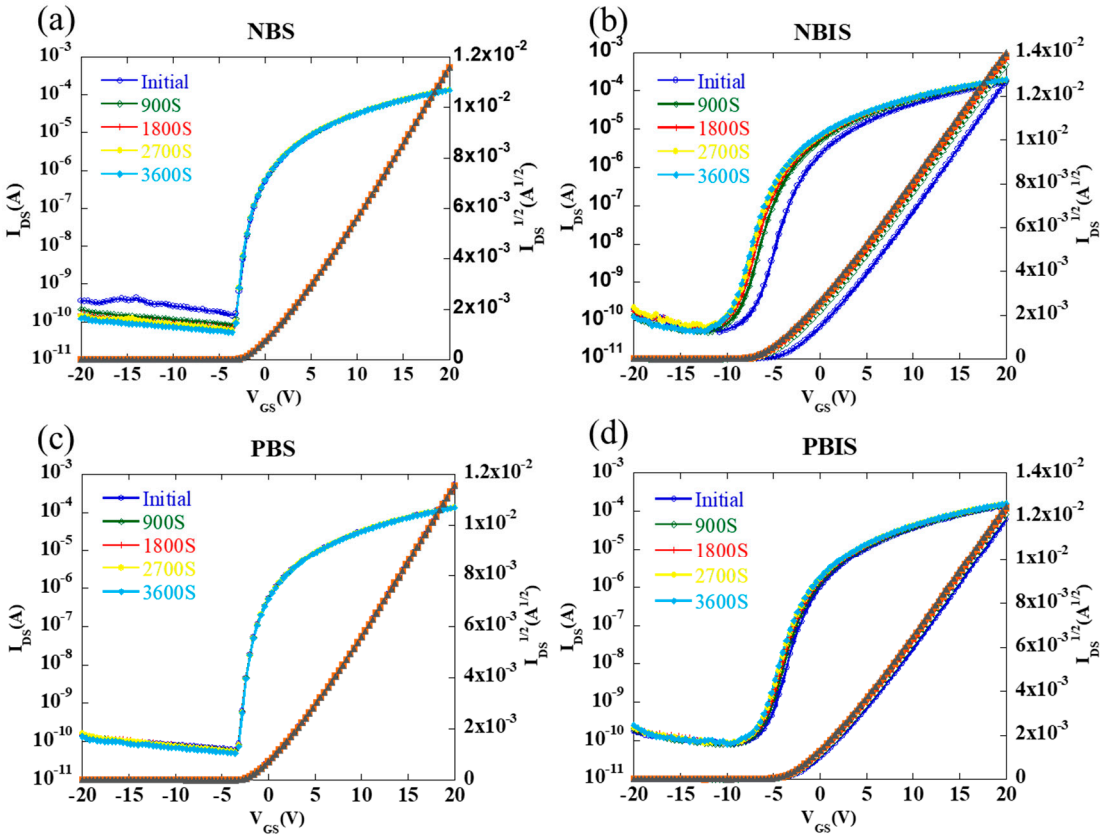

Figure 5. Variations of the transfer curves under (**a**) negative bias stress, (**b**) negative bias stress under illumination, (**c**) positive bias stress, (**d**) positive bias stress under illumination. During the test, a positive gate bias (V_G = 10 V, V_{DS} = 10 V) and a negative gate bias (V_G = −10 V, V_{DS} = 10 V) was applied as an electrical stress for 1 h, respectively. Transfer curves were recorded every 15 min.

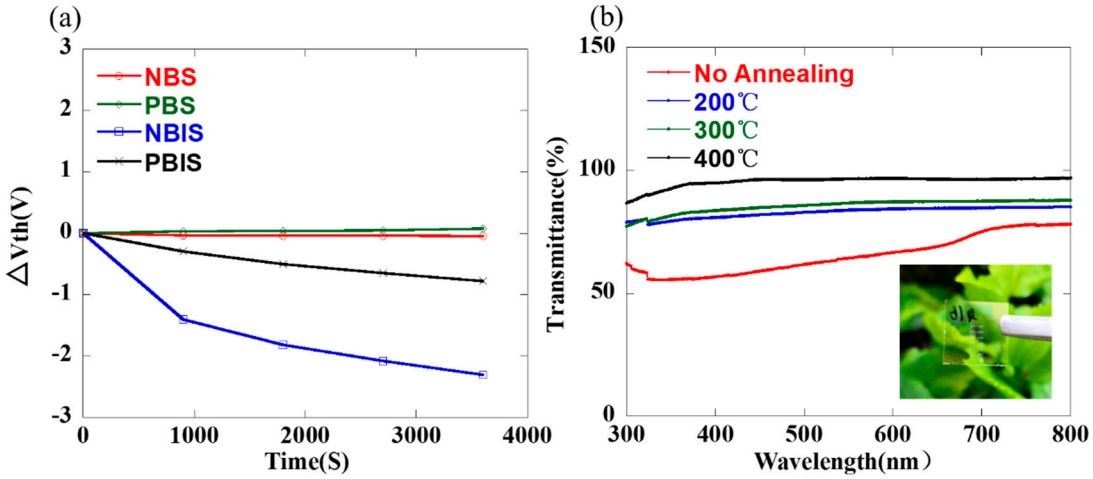

Figure 6. (**a**) Variations of V_{th} at the applied NBS time, NBIS time, PBS time and PBIS time, respectively. (**b**) Optical transmittance spectra of fabricated devices at different post-annealing temperature, no annealing, 200 °C, 300 °C, and 400 °C, respectively. The inset is the devices post annealed at 400 °C.

Table 2. Summary of the V_{th} of the coplanar top-gate TFTs under various bias stress.

Time (s)	V_{th} (V) NBS	V_{th} (V) NBIS	V_{th}(V) PBS	V_{th} (V) PBIS
Initial	−0.03	−1.81	−0.06	−0.52
900	−0.06	−3.21	−0.03	−0.81
1800	−0.06	−3.62	−0.03	−1.02
2700	−0.07	−3.88	−0.02	−1.17
3600	−0.07	−4.11	−0.01	−1.30

4. Conclusions

In summary, we have fabricated coplanar top-gate Nd-IZO TFTs using all sputtering processes. After 400 °C post-annealing for 1 h, the devices exhibited good electrical performance with a saturation mobility of 4.25 $cm^2 \cdot V^{-1} \cdot S^{-1}$, I_{on}/I_{off} ratio about 10^6, V_{th} of −0.97 V and SS about 0.34 V/decade. In addition, the devices showed excellent PBS and NBS stability that are likely due to its self-encapsulation. But PBIS and NBIS instability is still a problem due to the photogenerated holes trapped in the gate insulator and/or at the insulator/channel interface. In addition, the devices showed high transparency of about 96% over the visible-light region of 400–700 nm, which perfectly fits the needs of transparent display.

Author Contributions: J.C., H.N., Q.L. and Z.F. designed the research; H.L. and J.C. performed the experiments; J.C. and Y.Z. analyzed the data; X.H., R.Y., J.P. and H.N. provided valuable discussions and suggestions; H.N., J.C. and R.T. wrote the paper.

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Conflicts of Interest: The authors declare no conflict of interest.

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