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Improving the Gate-Induced Drain Leakage and On-State Current of Fin-Like Thin Film Transistors with a Wide Drain

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Abstract: Polycrystalline silicon (poly-Si) thin film transistors (TFT) with a tri-gate fin-like structure and wide drain were designed and simulated to improve gate-induced drain leakage (GIDL), ON-state current, and breakdown voltage. The GIDL of fin-like TFTs (FinTFTs) examined in this study was dominated by longitudinal band-to-band tunneling (L-BTBT). Extending the wide drain can effectively suppress the longitudinal electric field near the drain and improve L-BTBT GIDL and breakdown. In addition, a wider drain can lead to a large cross section in the current path and improve the ON-state current. FinTFTs with wide drain exhibit a low GIDL, a high ON-state current, and high breakdown voltage, while maintaining favorable gate controllability.

Keywords: thin-film transistor transistors; gate induced drain leakage (GIDL); Band-to-band tunneling (BTBT)

1. Introduction

Polycrystalline silicon (poly-Si) thin film transistors (TFTs) [1–4] and oxide semiconductor TFTs [5–8] are suitable for use in system-on-panels (SoP) or system-on-glass (SoG) displays because of their higher electron mobility compared with that of amorphous silicon (a-Si). The attraction of using poly-Si TFTs in displays lies in their ability to integrate peripheral functional components such as a controller, a high-voltage driver, and memory into the display panel. Improving the breakdown characteristics of poly-Si TFTs has become an important issue for realizing SoP. To improve these breakdown characteristics, methods such as lightly doped drain [9,10], offset drain [11,12], and semi-insulating field plate [13,14] were proposed. However, these methods increase the series resistances, and the ON-state current is sacrificed. A field-plate (FP) structure can increase the breakdown voltage, as well as the ON-state characteristics [15]. In this study, an FP was adopted to improve the breakdown characteristics without sacrificing the ON-state current.

The carrier mobility of poly-Si TFTs can be improved by scaling the channel length, which results in a decrease in the number of grain boundaries, i.e., an increase in the grain size in the active region [16]. However, the short channel effect is exacerbated as the channel length decreases. Three-dimensional (3-D) multi-gate structures, such as double-gate, tri-gate, and gate-all-around (GAA) structures, have been proposed to improve gate controllability and protect against the short-channel effects of nanoscale transistors [17–24]. Therefore, a tri-gate fin-like structure with a channel length (L) of 0.2 μm was employed in this study.

For a two-dimensional conventional planer structure, transverse band-to-band tunneling (T-BTBT) in the gate/drain overlap region is the dominant mechanism for gate-induced drain leakage (GIDL)

in the OFF-state [25–27]. However, for a 3-D structure such as a fin-like TFT (FinTFT) with a narrow channel wire width, band overlap between the valence band of the body and the conduction band of the drain region enables substantial lateral band-to-band tunneling (L-BTBT) of electrons from the body to the drain in the OFF-state [28,29]. This indicates that the mechanism of GIDL is L-BTBT for a 3-D structure. Recently, some studies have focused on minimizing L-BTBT in 3-D structures [30–34].

A dual-metal gate-stack architecture for nanowire field-effect transistors (FETs) [30] or nanowire junctionless FETs [31] can lead to a reduction in the electric field at the channel–drain extension interface width, which reduces L-BTBT-induced GIDL. In addition, a nanowire junctionless-mode FET with a long extension (the length between the source/drain electrode and the gate edge) has a lower GIDL current than does a nanowire inversion mode FET owing to a low doping concentration at the drain and thus a broad tunneling width [32].

The effect of a gate sidewall spacer on GIDL was investigated by Sahay and Kumar [33]. A nanowire metal–oxide—semiconductor FET with high-κ spacer-like HfO_2 has a low OFF-state current because of the low-peak electric field at the channel–drain extension interface; the OFF-state current increases as the dielectric constant of the spacer is reduced [33].

Because the GIDL current largely depends on drain extension doping, the influence of the lightly doped drain on L-BTBT is crucial. A nanowire FETs with a lightly doped drain (LDD) has a low OFF-state current because of its increased tunneling width; the OFF-state current decreases as the LDD length increases [34].

In our previous studies, a lateral double-diffused metal oxide semiconductor (LDMOS) and an FP high-voltage TFT with multi-gate and a wide drain have been proposed. Both devices show a high breakdown voltage; low specific on-resistance; and superior electrical characteristics [35,36]. LDMOS without a wide drain structure has a high electric field peak at the Ndrift/N^+ junction and a low breakdown voltage. As the wide drain region extends under the right edge of the field oxide, the breakdown voltage increases because of the suppressed electric field peak at the Ndrift/N^+ junction, resulting in a gradual field distribution and a high breakdown voltage. However, further extending this drain region causes a high electric field peak near the right edge of the gate field plate and a low breakdown voltage. Although breakdown characteristics have been investigated in our previous studies, the high OFF-state current of FinFET with a narrow wire due to overlapping of the conduction band in the drain region with the valence band of the drift region has not. Therefore, the effect of the wide drain structure of a FinTFT on the GIDL induced by L-BTBT and ON-state current is discussed in this paper.

In this study, an FP was formed to improve the breakdown characteristics of a FinTET without sacrificing the ON-state current. A tri-gate fin-like structure was adopted to suppress the short channel effects, and a wide drain design was used to reduce the electric field, thereby reducing GIDL and increasing the breakdown characteristics. The first part of this study focused on the effect of a wide drain on breakdown voltage. The electric field distribution is shown for comparison. For tri-gate FinTFTs with a wide drain, increasing the wide drain length is expected to suppress the electric field peak and increase the breakdown voltage. The second part of this study examined the effect of a wide drain length on the OFF-state GIDL current. GIDL induced by the L-BTBT of tri-gate FinTFTs with different wide drain lengths was investigated. A band diagram and the band-to-band generation rate distribution of devices with different wide drain lengths are shown. In addition, the ON-state current change with wide drain length is also important. The final part of this study analyzed the influence of wide drain length on the ON-state current of tri-gate FinTFTs with a gate field plate (GFP) or FP that has been subjected to extra-high voltage.

2. Materials and Methods

First, a 1 μm thick oxide layer was deposited as buried oxide. Subsequently, undoped poly-Si (100 nm thick) was deposited on a substrate to form the active region. Then, 5×10^{15} cm^{-2} of phosphorus was implanted to form the source and drain region. After the active region had been

created, a 50-nm thick HfO_2 with a high dielectric constant (~25) was deposited as the gate dielectric, and a 100-nm thick titanium nitride (TiN) was deposited as the gate electrode, with a work function of 4.9 eV. The equivalent oxide thickness (EOT) value of HfO_2 was 7.8 nm. Using high-k metal gate (HKMG) stacks can reduce the gate leakage and eliminate the poly-gate depletion [37–39]. A 250-nm thick tetra-ethyl-ortho-silicate (TEOS) oxide was deposited followed by chemical-mechanical polishing to planarize the top surface. Finally, an aluminum layer was deposited; this layer was defined as a FP by the mask.

Figure 1 shows the 3-D structure of the FinTFTs with various extended wide drain lengths (L_{EX}). The channel length (L) and height (h) are 0.2 µm and 100 nm, respectively. FinTFTs with different structures are simulated by varying each channel wire width (W_0) and fin number N_f (i.e., W40: W_0 = 40 nm, N_f = 5 and W200: W_0 = 200 nm, N_f = 3). The effective channel width W_{eff} is fixed at 1.2 µm (=$(2h + W_0) \times N_f$) for comparison. The L_{EX} is from the drain region to the channel region and varies from 0 to 0.6 µm. The length of the overlap between the FP and N^+ region (L_{ov1}) is 0.5 µm, as shown in Figure 1e.

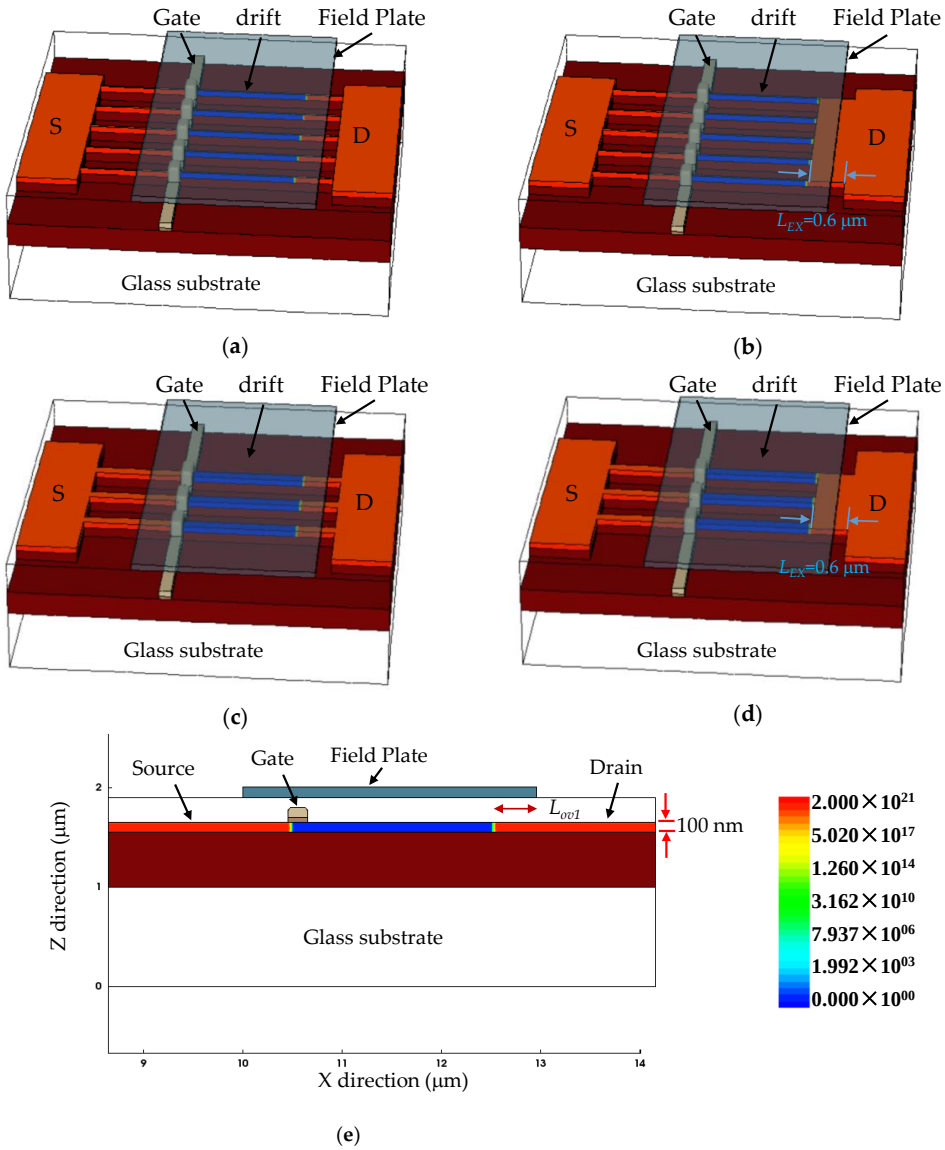


Figure 1. 3-D structure of FinTFTs: (**a**) W40 with L_{EX} = 0 µm; (**b**) W40 with L_{EX} = 0.6 µm; (**c**) W200 with L_{EX} = 0 µm; and (**d**) W200 with L_{EX} = 0.6 µm; (**e**) Cross-section view of FinTFT.

In this study, a Sentaurus technology computer aided design (TCAD) 3-D simulator was used. In the physic section of the device simulator, the mobility model, generation, and recombination models are included. For the mobility model, the "Doping Dependence", "Enormal", and "High Field Saturation" flags are used to consider mobility degradation due to impurity scattering, mobility degradation at the interfaces, and high electric field saturation, respectively. For generation and recombination models, "SRH", "Auger", "Avalanche", and "Band 2 Band" flags are used to model the Shockley–Read–Hall recombination, Auger recombination, avalanche generation (impact ionization), and band-to-band tunneling, respectively.

3. Results and Discussion

3.1. Breakdown Characteristics

Figure 2a shows the breakdown voltage of W40 and W200 with various L_{EXs}. When the drain current is 3×10^{-8} A, the breakdown voltage is taken as the drain voltage value at V_{GS} = 0 V. For W40, the breakdown voltage increases when L_{EX} increases from 0 to 0.6 µm. However, for W200, the influence of L_{EX} on the breakdown voltage is quite small until L_{EX} exceeds 0.6 µm. According to reports in the literature [40,41], a device with a narrower channel has a higher breakdown voltage due to a lower peak electric field, which is located near the drain; in addition, a device with a wider drift width has a lower electric field and impact ionization in the drift region, which results in a high breakdown voltage [42]. Here, a narrower channel in conjunction with a wider drain—for example, W40 with L_{EX} = 0.6 µm—exhibits a high breakdown voltage (approximately 57 V).

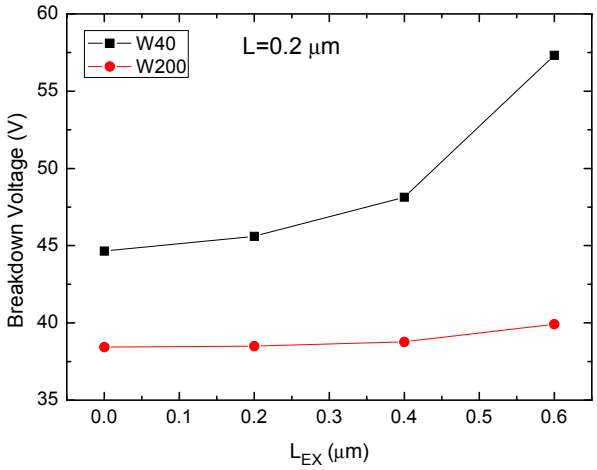


Figure 2. Breakdown voltage of FinTFTs with various L_{EX}.

Figure 3 shows the electric field distribution of W40 and W200 with L_{EX} = 0 and 0.6 µm at V_{GS} = 0 V and V_{DS} = 20 V (before breakdown). The highest electric field peaks of W40 and W200 are located at the intrinsic drift/N^+ junction and cause breakdown. Suppressing the electric field peak at the intrinsic drift/N^+ junction is an effective method for preventing breakdowns. In Figure 3a, it can be observed that extending the wide drain length of W40 to L_{EX} = 0.6 µm led to a marked decrease in the electric field peak at the intrinsic/N^+ junction and a consequent increase in the breakdown voltage. However, as each channel wire width increased, such as in W200, the difference in the electric field peak between L_{EX} = 0 and 0.6 µm was not pronounced, as shown in Figure 3b. Additionally, the peak electric field values for W200 with L_{EX} = 0 and 0.6 µm were 1.48 and 1.43 MV/m, respectively, compared with 1.34 and 1.11 MV/m, respectively, for W40 with L_{EX} = 0 and 0.6 µm. The narrower each channel wire, the lower was the peak electric field. Therefore, the breakdown voltage of W40 was higher than that of W200. Consequently, extending the wide drain under the FP contributed to a more uniform electric field distribution within the drift region. Therefore, the breakdown voltage improved with an increase in L_{EX}.

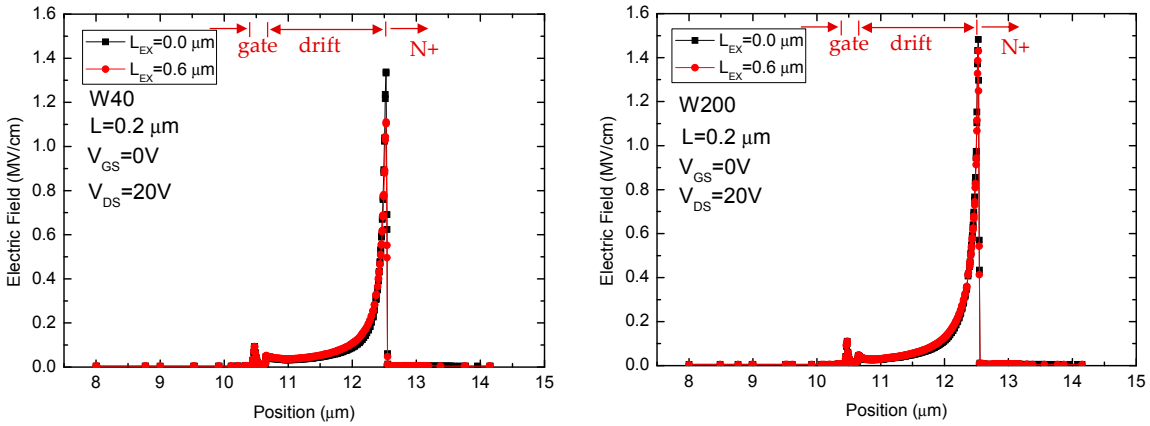


Figure 3. Electric field distribution of (**a**) W40 and (**b**) W200 with L_{EX} = 0 and L_{EX} = 0.6 μm at V_{DS} = 20 V (before breakdown).

3.2. GIDL and I_{ON}/I_{OFF} Ratio

Figure 4a presents the typical subthreshold characteristics of FinTFTs with a narrow W_0 (W40). The leakage current increased with a larger negative gate bias, which was due to GIDL. Increasing L_{EX} can not only improve the breakdown voltage but also suppress GIDL. For multi-gate devices such as a FinFET with a narrow channel width, L-BTBT instead of conventional T-BTBT is dominant [31]. L-BTBT occurs when a high drain bias (V_{DS}) and low gate bias (V_{GS}) are applied and the valence band in the body becomes higher than the conduction band in the drain region; these factors increase the GIDL current. The typical subthreshold characteristics of a device with a wide W_0 (W200) are shown in Figure 4b for comparison. The leakage current is almost constant below $V_{GS} = -1$ V because of the slight change in the longitudinal energy band, which bends when V_{GS} is varied. The longitudinal energy band diagrams of W40 and W200 with V_{GS} = 0 and −3 V are presented in Figure 5. Weak gate controllability in W200, which is similar to that in the conventional planar structure, results in a minor influence of gate bias on the longitudinal energy band (Figure 5b). However, the bending of the longitudinal energy band becomes evident for W40 and is caused by a large longitudinal electrical field at the intrinsic drift $/N^+$ junction (Figure 5a).

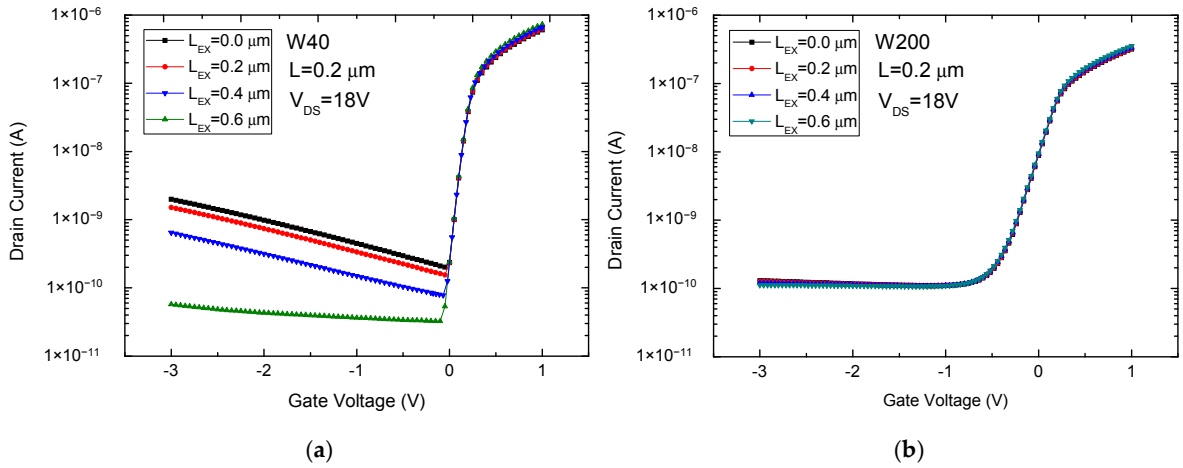


Figure 4. Subthreshold characteristics of (**a**) W40 and (**b**) W200 with various L_{EX} at V_{DS} = 18 V.

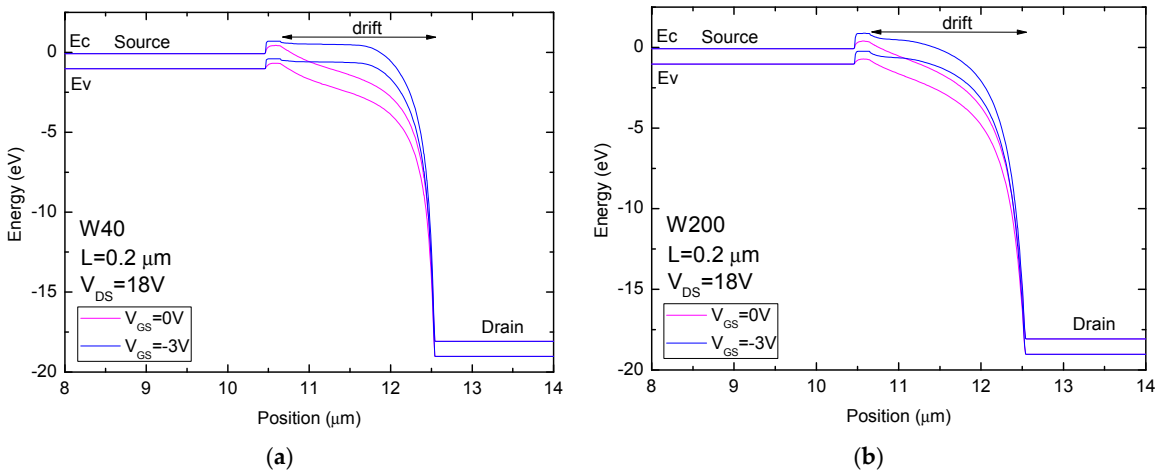


Figure 5. Longitudinal energy band diagrams of (**a**) W40 and (**b**) W200 with V_{GS} = 0 and −3 V.

To understand the dependence of GIDL on L_{EX}, the longitudinal energy band diagrams were analyzed. Figure 6 shows the longitudinal energy band diagrams of W40 with L_{EX} = 0 and 0.6 μm at V_{GS} = −3 V and V_{DS} =18 V. For FinTFTs with L_{EX} = 0.6 μm, an increase in the depletion width and a decrease in the electric field resulted in less pronounced band bending, and thus a wider tunneling width compared with FinTFTs with L_{EX} = 0 μm.

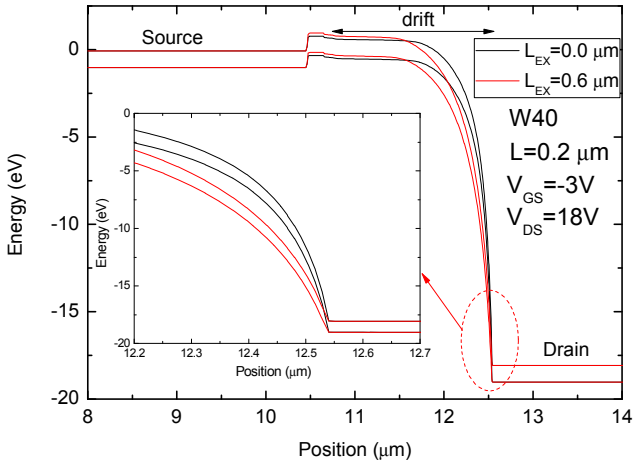


Figure 6. Longitudinal energy band diagrams of W40 with L_{EX} = 0 and L_{EX} = 0.6 μm at V_{GS} = −3 V and V_{DS} = 18 V.

Figure 7a shows variation in the GIDL current with a wide drain length for W40 and W200 at V_{GS} = −3 V and V_{DS} = 18 V. The values in Figure 7a were obtained from the simulation results. The GIDL current of W40 and W200 without the BTBT model are also shown in Figure 7a. The GIDL current was almost constant when the BTBT model was not considered. The values for W40 and W200 are indicated by the black line with a hollow symbol and red line with a hollow symbol, respectively. W40 with L_{EX} = 0 μm has a large GIDL current because of the enhanced L-BTBT. As a result, the GIDL current decreased as L_{EX} increased. The GIDL current of W40 with L_{EX} = 0.6 μm had a value close to that observed at the black line with a hollow symbol. However, the device with a wide W_0 (W200) exhibited a small change in GIDL current with an increase in L_{EX}, and all values of the GIDL current were close to the red line with a hollow symbol. Notably, the GIDL current of W40 with L_{EX} = 0.6 μm was lower than that of W200; this indicates that a device with a wide drain can effectively reduce the GIDL current. Figure 7b shows the electric field distribution of W40 and W200 with L_{EX} = 0 and 0.6 μm

at $V_{GS} = -3$ V and $V_{DS} = 18$ V. The electric field peaks of W40 and W200 are located at the intrinsic drift/N^+ junction. The peak value of the electrical field near the drain side can be expressed in the following relationship: W40/L_{EX} = 0 μm > W200/L_{EX} = 0 μm > W200/L_{EX} = 0.6 μm > W40/L_{EX} = 0.6 μm. The higher the electric field peaks, the higher is the GIDL current.

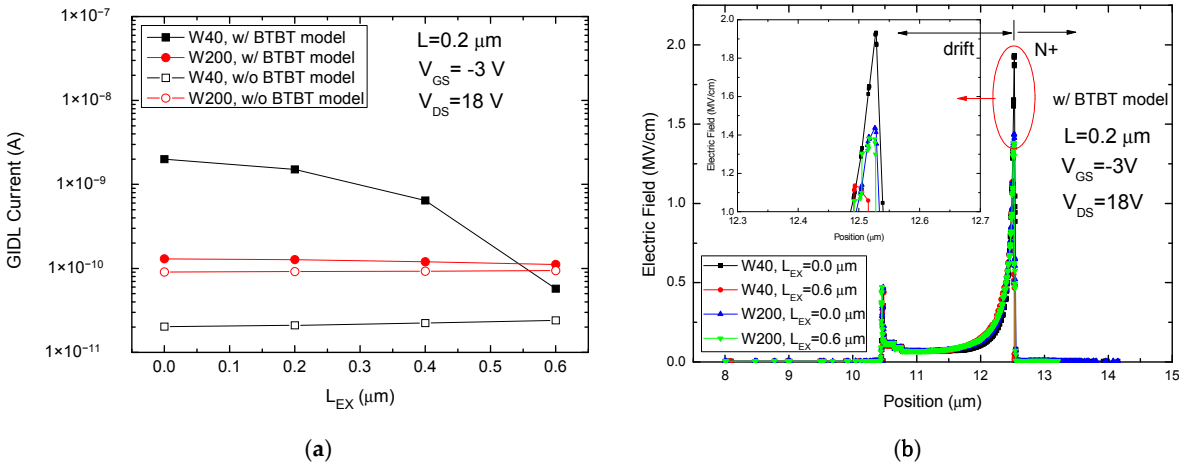


Figure 7. (**a**) Variation in the GIDL current with a wide drain length for W40 and W200 at $V_{GS} = -3$ V and $V_{DS} = 18$ V. (**b**) Electric field distribution of W40 and W200 with L_{EX} = 0 and 0.6 μm at $V_{GS} = -3$ V and $V_{DS} = 18$ V.

To clarify the improvement in the dependence of GIDL on L_{EX}, the band-to-band generation rate (BTBT-GR) of W40 and W200 with L_{EX} = 0 and 0.6 μm at $V_{GS} = -3$ V and $V_{DS} = 18$ V were analyzed to explain the correlation between GIDL and L_{EX}, as shown in Figures 8 and 9. The highest BTBT-GR for both W40 and W200 are located at the intrinsic drift/N^+ junction, and its peaks are close to the surface at the drift/FP overlap region. The devices with L_{EX} = 0.6 μm had a lower BTBT-GR compared with those with L_{EX} = 0 μm, for which the GIDL was improved. Figure 8c and d show the BTBT-GR of W40 along with electric field contours near the intrinsic drift/N^+ junction. The red area under the FP is the dominant tunneling region of the FinTFT. Owing to the lower longitudinal electric field in the FinTFT with L_{EX} = 0.6 μm, devices with extended wide drain were observed to have a lower GIDL. The BTBT-GR and electric field near the corner of W200 were higher than those towards the center, as shown in Figure 9c,d. In addition, the BTBT-GR, as well as the electric field in the corner of W40, were higher than those in the corner of W200. Therefore, W40 had a higher GIDL current than W200 owing to a higher BTBT-GR and the electric field near the corner.

Figure 10 shows the I_{ON}/I_{OFF} ratio and I_{ON} of W40 with various L_{EX} values at V_{DS} = 18 V. The ON-state current (I_{ON}) is obtained at V_{GS} = 3 V, and the off-state current (I_{OFF}) is obtained at V_{GS} = 0 V. As the L_{EX} increases, so does the I_{ON} of W40 with GFP and the I_{ON}/I_{OFF} ratio (shown in Figure 10a). Extending the wide drain region length leads to a large cross section in the current path and increases the I_{ON}. However, when the FP is applied to extra-high voltage (V_{FP} = 30 V) instead of the gate voltage, the I_{ON} slightly decreases as the L_{EX} increases, as shown in Figure 5b. According to a previous study [26], when V_{FP} = 30 V, FinTFTs with wide drift have a high electron density concentrated at the corner of the drift and a low electron density at the non-corner region. Nevertheless, as the drift region of FinTFTs changed to multiple nanowire and each wire width was downscaled to nanometers, the corner and non-corner regions exhibited high electron density. Lower electron density in the FinTFTs with a wide drift (L_{EX} = 0.6 μm) leads to a low I_{ON}. Therefore, the I_{ON} of FinTFTs with L_{EX} = 0 μm is higher than that of that with L_{EX} = 0.6 μm. The FinTFTs with GFP not only achieved a high I_{ON} and I_{ON}/I_{OFF} ratio but also required no external bias.

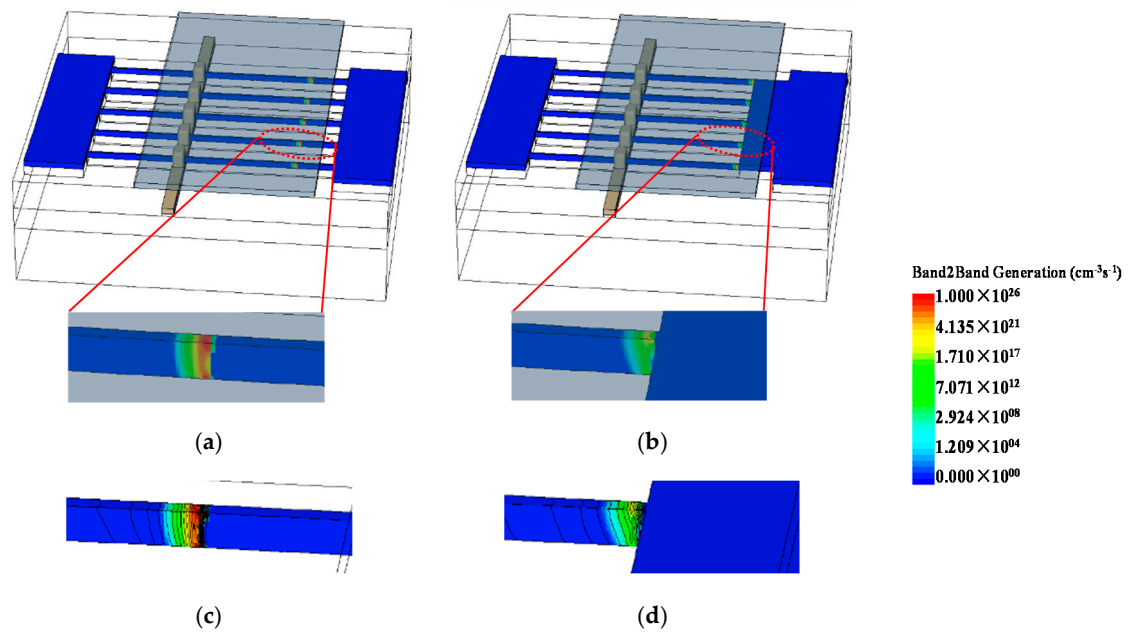


Figure 8. BTBT-GR of W40 with (**a**) L_{EX} = 0 µm and (**b**) L_{EX} = 0.6 µm and 3-D profile with electric field contours for (**c**) L_{EX} = 0 µm and (**d**) L_{EX} = 0.6 µm.

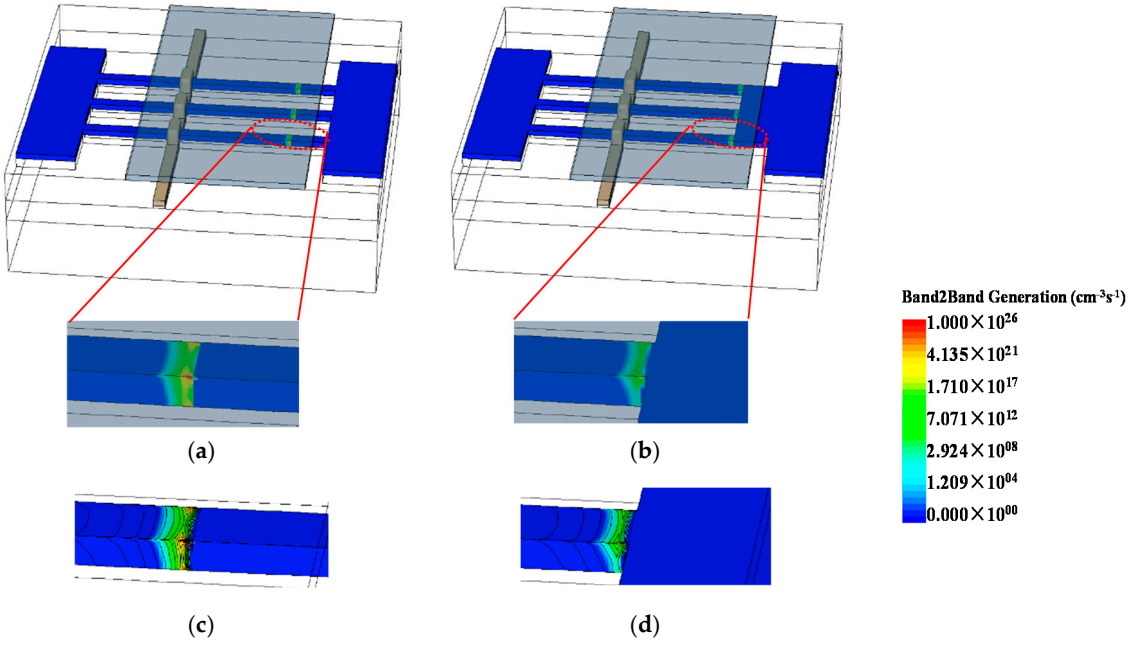
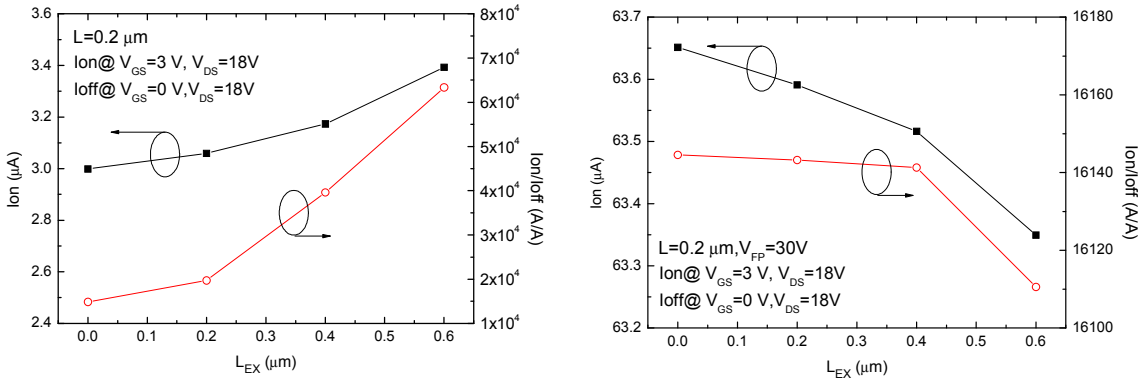


Figure 9. BTBT-GR of W200 with (**a**) L_{EX} = 0 µm and (**b**) L_{EX} = 0.6 µm and 3-D profile with electric field contours for (**c**) L_{EX} = 0 µm and (**d**) L_{EX} = 0.6 µm.



(**a**) (**b**)

Figure 10. On-state current and I_{ON}/I_{OFF} ratio of W40 with various L_{EX} at V_{DS} = 18 V. (**a**) Gate field plate (GFP) and (**b**) V_{FP} = 30 V.

4. Conclusions

An investigation of breakdown voltage, GIDL, and ON-state current in tri-gate FinTFTs with various L_{EX} was conducted using 3-D simulations. This short channel (L = 0.2 μm) is composed of a FinTFT contains multi-gate, which enables the suppression of short channel effects, and a wide drain, which reduces the longitudinal electric field at the intrinsic drift $/N^+$ junction and improves GIDL and the breakdown characteristics. By extending the wide drain region length, the electric field peak was effectively suppressed, as was L-BTBT-induced GIDL. Furthermore, the wide drain FinTFTs with GFP exhibited higher ON-state currents and required no external bias. As the technology node is further scaled down, FinTFTs with wide drains demonstrate their potential for use as TFTs in SoP applications.

Author Contributions: H.-H.H. conceived and designed the experiments; H.-H.H. and Y.-W.Z. ran the simulation; H.-H.H. and Y.-W.Z. performed the electrical characterization; H.-H.H. and Y.-W.Z. analyzed the data; H.-H.H. and K.-M.C. supervised the project; H.-H.H. and Y.-W.Z. wrote the manuscript; and all authors contributed discussions and feedback to the manuscript and the project.

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