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Charge Carrier Distribution in Low-Voltage Dual-Gate Organic Thin-Film Transistors

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Featured Application: Organic Integrated Circuits.

Abstract: Dual-gate organic thin-film transistors (DGOTFTs), which exhibit better electrical properties, in terms of on-current and subthreshold slope than those of single-gate organic thin-film transistors (OTFTs) are promising devices for high-performance and robust organic electronics. Electrical behaviors of high-voltage (>10 V) DGOTFTs have been studied: however, the performance analysis in low-voltage DGOTFTs has not been reported because fabrication of low-voltage DGOTFTs is generally challenging. In this study, we successfully fabricated low-voltage (<5 V) DGOTFTs by employing thin parylene film as gate dielectrics and visualized the charge carrier distributions in low-voltage DGOTFTs by a simulation that is based on finite element method (FEM). The simulation results indicated that the dual-gate system produces a dual-channel and has excellent control of charge carrier density in the organic semiconducting layer, which leads to the better switching characteristics than the single-gate devices.

Keywords: organic transistor; dual-gate; carrier distribution; simulation

1. Introduction

Organic thin-film transistors (OTFTs) have been attracting attention in the field of flexible and printed electronics. OTFTs have intrinsic mechanical flexibility due to the loose van der Waals force between organic molecules, and can be fabricated on flexible plastic films by a low temperature printing method. Ink-jet printing provides for drop-on-demand fabrication from digital data and can directly pattern customizable elements on a substrate. These features are ideal for large-are electronic applications, including a flexible sensor sheet [1] and radio frequency identification (RFID) tags [2].

Towards improving the OTFT device performances, in terms of on-current (I_{ON}) and subthreshold slope (SS), the transistor channel length (L) and gate dielectric thickness have been scaled down [3,4]. Dual-gate (DG) architecture which has both bottom-gate (BG) and top-gate (TG) electrode is also known as a way to get a higher current and a steeper subthreshold slope than those from single-gate architecture commonly employed [5,6]. This DG architecture also enables control of threshold voltage (V_{TH}) of the OTFTs [7]. These features are significant for realizing high-performance and robust organic electronics [8–15].

Operation analysis of low-voltage dual-gate organic thin-film transistors can be significant, since low-voltage OTFTs have specific issues that is less significant in high-voltage, for example,

contact resistance which is associated with gate-voltage [16]. The electrical behaviors of dual-gate organic transistors (DGOTFTs) have been studied, including its analytical model [17,18], contact resistance [19], charge transport and back-gate-bias effects [20]. However, these studies are based on OTFTs that were operated at high-voltage (>10 V): the operation analysis in low-voltage (<5 V) DGOTFTs is never reported. This possible reason is that fabrication of low-voltage DGOTFTs is generally challenging because vertical multi-layer-stacking of thin gate dielectric layers would be required.

In this study, charge carrier distribution in low-voltage OTFTs with BG, TG, and DG architecture was reported. Low-voltage DGOTFTs were successfully fabricated by employing 140-nm-thick parylene film as gate dielectrics formed by chemical vapor deposition (CVD). Numerical simulation of the carrier distribution was carried out based on a finite element method (FEM). The charge carrier distributions were successfully imaged. The simulation results indicated that DG system produces a dual-channel and has excellent control of charge carrier density in the organic semiconducting layer, which leads to the better switching characteristics of the OTFTs than the single-gate devices.

2. Materials and Methods

2.1. Device Fabrication

Schematic structure and photograph of the fabricated OTFT devices are shown in Figure 1. Single- and dual-gate OTFTs were integrated on a glass substrate, as shown in Figure 1a,b. Note that for the DG devices, the bottom- and top-gate electrode was connected each other. All layers except the gate dielectrics were formed by printing processes at process temperatures below 150 °C [21,22]. 140-nm-thick parylene films that were formed by chemical vapor deposition (CVD) were used as the gate dielectric and encapsulation layer. Parylene is good for low-voltage operation due to its low trap density [23] and fine thin-film formation [24]. The electrodes were fabricated by inkjet printing of a silver nanoparticle ink. Formation of the short-channels was enabled by separate printing of the source/drain electrodes as reported [25]. In this work, the standard deviation in channel length was ±2 μm. A printed fluoropolymer layer was used as a confining bank layer, whereby the semiconducting layer was printed in the area defined by the bank layer using dispenser equipment. These device fabrication processes used drop-on-demand printing techniques such as ink-jet printing and dispenser printing for ease of the layout customization.

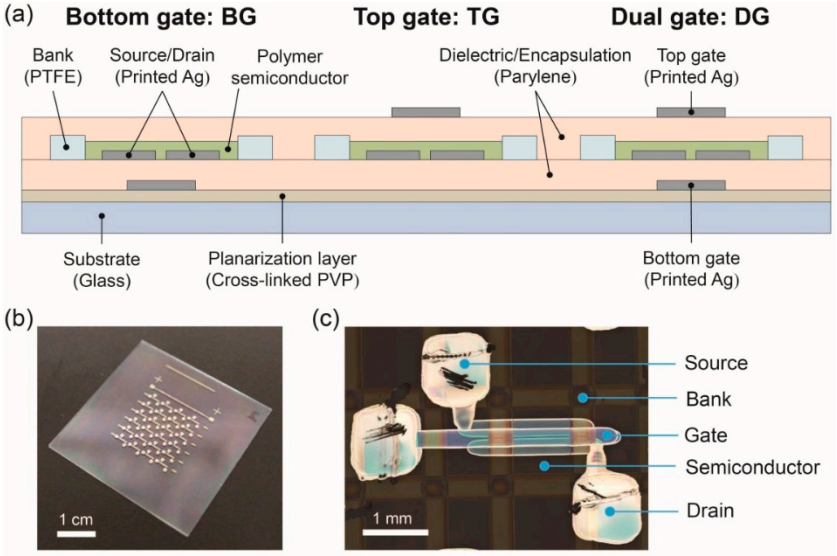

Figure 1. (**a**) Schematic structures, (**b**) photograph and (**c**) layout of fabricated organic thin-film transistor (OTFT) devices.

Cross-linked poly(4-vinyl-phenol) (PVP) was formed on 0.5-mm-thick glass substrates to modify the surface wettability. PVP ($M_W \approx$ 25,000, Sigma-Aldrich, St. Louis, MI, USA) and poly(melamine-co-formaldehyde) ($M_N \approx$ 432.84 wt %, Sigma-Aldrich, St. Louis, MI, USA) were dissolved in propylene glycol monomethyl ether acetate (PGMEA), and spin-coated onto the substrates, followed by annealing process at 150 °C for 30 min. in ambient air to produce thermal-crosslinking. Next, a silver nanoparticle ink in hydrocarbon-based solution (NPS-JL, Harima Chemicals, Chuo-ku, Tokyo, Japan) was printed as bottom-gate electrodes using an inkjet printer (DMP2831, Fujifilm Dimatix, Santa Clara, CA, USA) with 10 pl nozzles. During the inkjet printing process, the substrates and cartridge were kept at 50 and 40 °C, respectively. The substrates were then heated at 150 °C for 15 min. in ambient air to sinter the silver nanoparticles. A 140-nm-thick parylene (diX-SR, KISCO, Tokyo, Japan) gate dielectric layer was then formed by chemical vapor deposition. Source and drain electrodes were subsequently printed in the same manner as the gate electrodes. The conditions of S/D printing and sintering process were same as those for the gate electrodes. Fluoropolymer (DuPont, Teflon AF1600) bank layers (70 nm thick) were then printed using a dispenser system (MUSASHI Engineering, Image Master 350 PC) at a pattering speed of 20 mm·s^{-1} and with a discharge pressure of 6 kPa. During the dispensing process, the plates and nozzle temperatures were kept at 60 and 30 °C, respectively. A p-type donor-acceptor polymer semiconductor ink (0.03 wt %, mesitylene solvent, Mitsubishi Chemical, MOP-01) was then printed onto the area defined by the bank layer by the dispenser system at a patterning speed of 20 mm·s^{-1} and discharge pressure of 2 kPa, while keeping the stage and nozzle temperatures at 60 and 30 °C, respectively, followed by an anneal at 150 °C in nitrogen globe box for 1 h to remove the solvent. 10-nm-thick semiconducting layer was obtained. Then, a 140-nm-thick parylene (diX-SR, KISCO, Tokyo, Japan) gate dielectric layer was then formed by chemical vapor deposition. Finally, top-gate electrodes were printed and sintered in the same manner as the bottom-gate electrodes.

2.2. Device Characterization

The capacitance of the dielectric was measured using an LCR meter (ZM2376, NF Corporation, Yokohama, Japan). The electrical characteristics of the OTFTs and inverter circuits were measured using a semiconductor parameter analyzer (model 4200A-SCS, Keithley, Cleveland, OH, USA). All electrical measurements were carried out in the air. Optical microscope images of the devices were obtained using a digital microscope (LEXT OLS4000, Olympus, Shinjuku, Tokyo, Japan).

2.3. Method of the Device Simulation

Device simulation in finite element method (FEM) was carried out to investigate the carrier distribution in single- and dual-gate p-type transistors by using the mathematics module of COMSOL Multiphysics (KESCO Ltd., Tokyo, Japan) [14]. The simulation was based on the Poisson equation and the continuity equation.

$$\vec{\nabla} \cdot \left[\vec{\nabla}(x,y) \right] = \frac{e}{\varepsilon} [n_f(x,y)n + n_t(x,y) - n_0] \quad (1)$$

$$\vec{\nabla} \cdot \left[en_f(x,y)\mu \overrightarrow{\nabla E_F}(x,y) \right] = 0 \quad (2)$$

Here V is the electrostatic potential, e is the elementary charge, ε is the dielectric constant, n_f is the free hole carrier density, n_t is the trapped hole carrier density, n_0 is the carrier density in the neutral state, μ is the mobility tensor, and E_F is the Fermi energy. These equations contain two independent variables: $V(x, y)$ and $E_F(x, y)$. Carrier densities n_f and n_t were approximated as

$$en_f(x,y) = D_v exp(-\frac{E_F(x,y) - E_v}{k_B T}) \quad (3)$$

$$n_t(x,y) = \int_{-\infty}^{+\infty} \frac{\frac{D_t}{E_t} exp[\frac{E_v - E}{E_t}]}{1 + exp[-\frac{E_F(x,y) - E}{k_B T}]} dE \approx D_t exp[-\frac{E_F(x,y) - E_v}{k_B T}] \quad (4)$$

Here D_v is the effective density of states in the valence band, E_v is the top energy of the valence band, k_B is the Boltzmann constant, T is the temperature, D_t is the total density of trap states, and E_t is the average energy of traps with exponential density of states.

The parameters used in the simulation were summarized in Table 1. Channel width, channel length, channel thickness, dielectric constant of insulator (ε_i), and dielectric thickness were measured directly by experiments. The dielectric constant of semiconductor (ε_s) and temperature were set at typical values. The effective density of states in the valence band (D_v) was estimated from a typical effective mass of organic semiconductor, $3m_0$, and has little effect on the simulation results. Here m_0 is the mass of a free electron. The other parameters, mobility, work function, ionization energy, density of trap states (D_t), average energy of trap states (E_t), and carrier density in the neutral state (n_0), were arbitrarily set to fit the experimental data. In the simulation, either work function or ionization energy does not matter as long as the difference between the two does not change. We assumed anisotropic mobility because it is a common nature of polymeric semiconductors as reported [26].

Table 1. Parameters Used in the finite element method (FEM) Simulation.

Parameter	Value	Parameter	Value
Channel width	732 μm	Temperature	300 K
Channel length	6.73 μm	Work function of source, drain and gate electrodes	4.6 eV
Channel thickness	10 nm	Ionization energy of semiconductor	5.0 eV
Dielectric constant of insulator, ε_i	$3.38\varepsilon_0$	The effective density of states in the valence band, D_v	1.6×10^{20} cm^{-3}
Dielectric constant of semiconductor, ε_s	$4\varepsilon_0$		
Dielectric thickness	140 nm	Density of trap states, D_t	3×10^{18} cm^{-3}
Mobility along the channel, μ_x	0.24 cm^2/Vs	Average energy of trap states, E_t	0.15 eV
Mobility perpendicular to the channel, μ_y	0.048 cm^2/Vs	Carrier density in the neutral state, n_0	3×10^{23} cm^{-3}

3. Results and Discussion

Transfer characteristics in the saturation regime and output characteristics of the OTFTs were shown in Figure 2. Transfer characteristics in the linear regime obtained from experimental and numerical simulation were shown in Figure 3. The simulated characteristics were similar to the experimental. Channel width (W) and length (L) was 740 μm and 7 μm, respectively. Capacitance per unit area was 21 nF/cm^2. The electrical properties such as mobility in saturation (μ_{sat}) and linear regime (μ_{lin}), threshold voltage (V_{TH}), on-current (I_{ON}) and subthreshold slope (SS) were summarized at Table 2. At $V_{DS} = -5$ V, I_{ON} for the BG, TG, and DG devices was 0.23 ± 0.04 μA, 1.5 ± 0.2 μA, and 1.9 ± 0.2 μA, respectively. SS for the BG, TG, and DG devices was 0.5 ± 0.3 V/dec, 1.5 ± 1.0 V/dec, and 0.3 ± 0.1 V/dec, respectively. The higher I_{ON} and steeper SS were obtained: the result is consistent with that from previously reported [5,6]. Furthermore, for the DG devices, saturation ($V_{DS} = -5$ V) and linear ($V_{DS} = -0.1$ V) mobility was 0.05 ± 0.013 cm^2/Vs and 0.047 ± 0.013 cm^2/Vs, respectively. The mobility for the DG devices was also better than those of the single-gate devices. On the whole, the DG devices exhibited better electrical properties.

To elucidate the origin of better switching characteristics of the DG device, charge carrier distribution in the organic semiconducting layer was displayed in Figure 4. Spatial x-axis and y-axis were defined as Figure 4a, where the origin was set to be the crossing point of middle of the channel and the line along the bottom-dielectric/semiconductor interface. Free hole densities as a function of y-axis at $V_{GS} = 1$ V (off state) and $V_{GS} = -2$ V (on state) were shown in Figure 4b,c. $V_{DS} = -0.1$ V in all

three device simulations. For the single-gate devices, the carrier density at the side of the gate electrode could be controlled in the range of 6.2×10^{20}–2.5×10^{23} m^{-3}. Nevertheless, the carrier density at the opposite side of the gate electrode was hardly controlled (2.1×10^{21}–5.5×10^{22} m^{-3}). On the other hand, for the DG system, the carrier density over the entire region in the channel could be controlled in the wider range of 4.8×10^{18}–3.8×10^{23} m^{-3}. This excellent control of carrier density in the DG system should contribute to obtaining the steeper *SS* than those from the single-gate system.

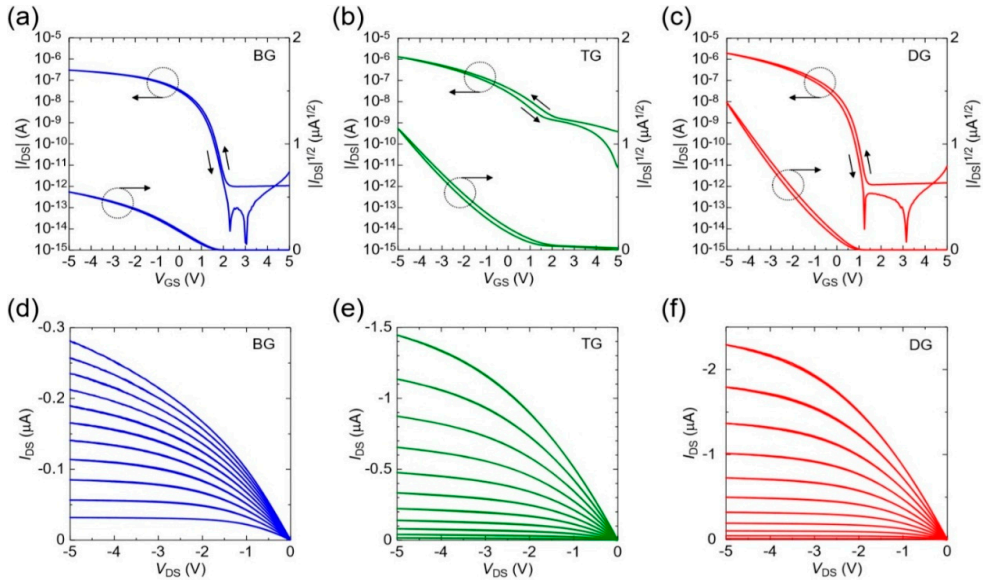

Figure 2. Transfer characteristics of fabricated (**a**) bottom-gate (BG), (**b**) top-gate (TG), and (**c**) dual-gate (DG) OTFTs at V_{DS} = −5 V. Output characteristics of fabricated (**d**) bottom-gate, (**e**) top-gate, and (**f**) dual-gate OTFTs. Gate-source voltages were from 0 to −5 V in −0.5 V step. The channel dimensions were W/L = 740 μm/ 7 μm.

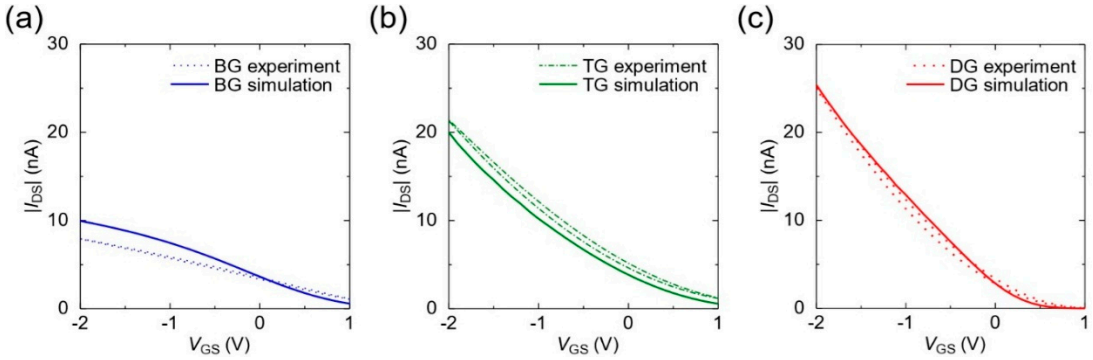

Figure 3. Transfer characteristics of (**a**) bottom-gate, (**b**) top-gate, and (**c**) dual-gate OTFTs obtained from the experimental and numerical simulation at V_{DS} = −0.1 V. The channel dimensions were W/L = 740 μm/7 μm.

Table 2. Electrical Properties of the Fabricated OTFTs.

Device Structure	μ_{sat} (cm^2/Vs)	V_{TH} (V)	I_{ON} (μA)	*SS* (V/dec)	μ_{lin} (cm^2/Vs)	I_{ON} (nA)	*SS* (V/dec)
	V_{DS} = −5 V, V_{GS} > −5 V				V_{DS} = −0.1 V, V_{GS} > −2 V		
BG	0.012 ± 0.002	1.5 ± 0.1	0.23 ± 0.04	0.5 ± 0.3	0.012 ± 0.002	6.4 ± 0.8	1.6 ± 0.3
TG	0.038 ± 0.005	0.68 ± 0.06	1.5 ± 0.2	1.4 ± 1.0	0.032 ± 0.003	19 ± 1	1.4 ± 0.2
DG	0.050 ± 0.013	0.42 ± 0.04	1.9 ± 0.2	0.3 ± 0.1	0.047 ± 0.011	24 ± 2	0.4 ± 0.1

We note that the difference in threshold voltage between three device structures needs to be taken into account: however, it is well known that the determination of threshold voltage from experimental transfer characteristics is not always accurate in organic field-effect transistors [27]. On the other hand, in this simulation, the flat band gate voltages, which has a similar implication of threshold voltage, were −0.2 V for all three device structures: the comparison of carrier density at a same gate voltage is reasonable in this simulation.

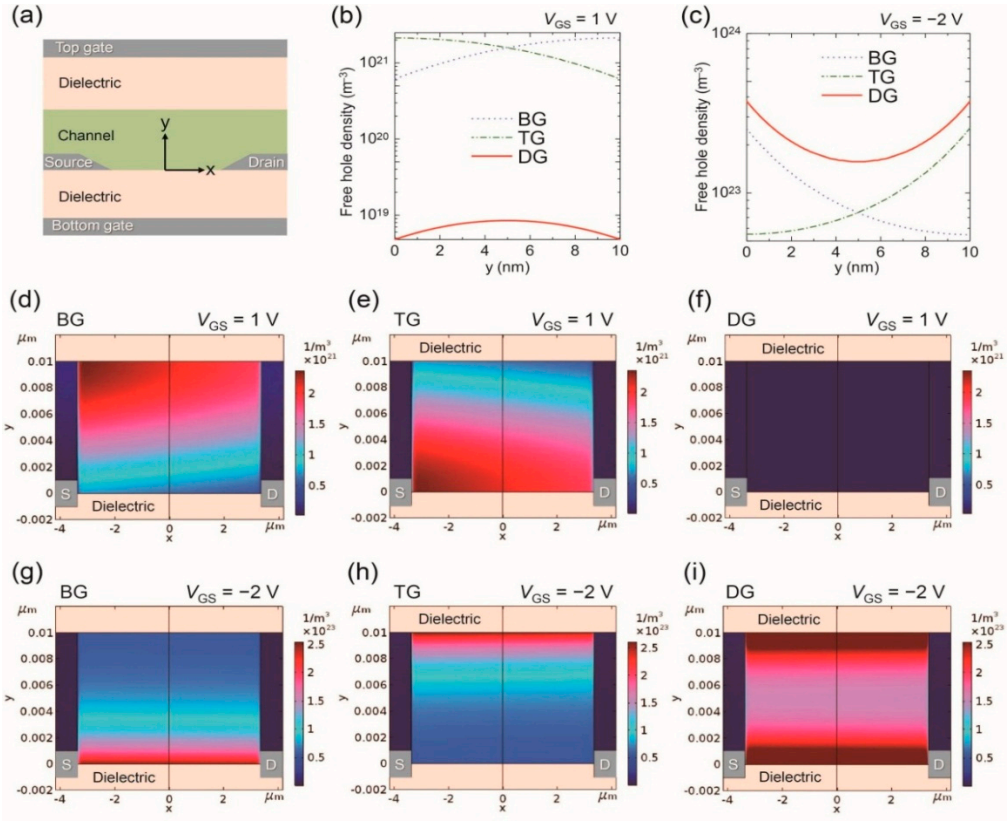

Figure 4. (**a**) Device geometry in the simulation; free hole density as a function of *y*-axis at (**b**) V_{GS} = 1 V and (**c**) V_{GS} = −2 V. Charge carrier distribution in (**d**) BG, (**e**) TG, (**f**) DG device at V_{GS} = 1 V (off-state), and (**g**) BG, (**h**) TG, (**i**) DG devices at V_{GS} = −2 V (on-state). V_{DS} = −0.1 V.

Moreover, the charge carrier distributions at on/off state were visualized in Figure 4d–i. It is clear that DG device could control the carrier density well, as opposite to single-gate devices. For all the gate structure devices, the accumulation channel whose thickness was estimated to be about 2-nm-thick [28] was formed at on-state. In particular, for the DG device, the channel was formed at both bottom- and top-gate side, and carrier density of this dual-channel was estimated to be <3.8 × 10^{23} m^{-3}, which was higher density than that of single-gate devices (<2.5 × 10^{23} m^{-3}). This dual-channel obviously flow current more than the single-channel, while I_{ON} for the DG devices ($I_{ON}{}^{DG}$) was approximately equivalent to the sum of I_{ON} for the BG devices ($I_{ON}{}^{BG}$) and I_{ON} for the TG devices ($I_{ON}{}^{TG}$), $I_{ON}{}^{DG} \approx I_{ON}{}^{BG} + I_{ON}{}^{TG}$, according to Table 2.

For a discussion about the reason why mobility for the DG devices was higher than that of the single-gate devices, potential in the channel were simulated, as shown in Figure 5a,b. Potential in the source and drain region was pinned at 0 V and −0.1 V, respectively. Gate voltage affected the slope of the channel potential and voltage drop at source/channel interface and channel/drain interface.

Channel-width-normalized channel resistance ($R_{ch}W$), contact resistance at source/channel (R_sW) and channel/drain (R_dW) were extracted from Figure 5a,b and plotted as a function of gate voltage in Figure 5c–e. At V_{GS} = −2 V, $R_{ch}W$ for the BG, TG, DG device was estimated to be 1.8 × 10^3 Ωm,

1.8×10^3 Ωm, 0.8×10^3 Ωm, respectively. There was negligible difference between $R_{ch}W$ for the BG device ($R_{ch}W^{BG}$) and $R_{ch}W$ for the TG device ($R_{ch}W^{TG}$), on the other hand, $R_{ch}W$ for the DG device ($R_{ch}W^{DG}$) was about 55% less than that of the single-gate devices at $V_{GS} = -2$ V ($R_{ch}W^{BG} \approx R_{ch}W^{TG} > R_{ch}W^{DG}$), because the DG device produces the dual-channel as shown in Figure 4i.

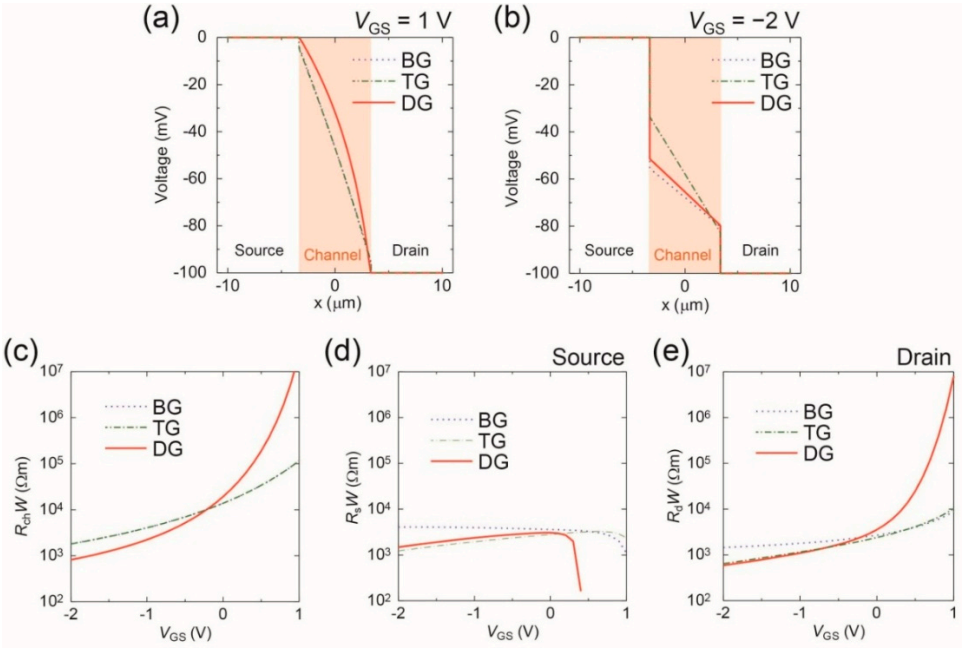

Figure 5. Simulation of the potential in source, channel, drain region as a function of *x*-axis at (**a**) $V_{GS} = 1$ V and (**b**) $V_{GS} = -2$ V. Channel-width-normalized (**c**) channel resistance ($R_{ch}W$), (**d**) source/channel contact resistance (R_sW) and (**e**) channel/drain contact resistance (R_dW) as a function of V_{GS}.

Contact resistances at $V_{GS} = -2$ V for the DG device (R_sW^{DG}: 1.5×10^3 Ωm, R_dW^{DG}: 0.6×10^3 Ωm) were approximately equivalent values to those for the TG device (R_sW^{TG}: 1.2×10^3 Ωm, R_dW^{TG}: 0.6×10^3 Ωm). R_sW and R_dW (at $V_{GS} = -2$ V) for the TG/DG device were 60−70% less than those for the BG device (R_sW^{BG}: 4.1×10^3 Ωm, R_dW^{BG}: 1.5×10^3 Ωm). In brief, R_sW, R_dW for the TG, DG device were less than the BG device (R_sW or R_dW: BG > TG ≈ DG) [29]. This is the reason why mobility for the TG, DG devices was higher than the BG devices.

Meanwhile, mobility for the DG devices was also higher than that for the TG devices. For a discussion about the reason for this, we focus on carrier density of the channels. Maximum carrier density of the dual-channel (3.8×10^{23} m^{-3}) was 1.5 times more than that of single-channel (2.5×10^{23} m^{-3}), as shown in Figure 4c. To achieve carrier density equivalent of the dual-channel, at least $V_{GS} < -2$ V would be required in the TG devices. Since the mobility was associated with gate-voltage [30], we suggest that higher carrier density of the DG devices would contribute to obtaining the higher mobility than the TG devices.

4. Conclusions

In conclusion, we successfully fabricated low-voltage BG, TG, DG organic transistors by employing thin parylene dielectrics. The DG devices exhibited better switching characteristics than the single-gate devices. To elucidate this reason, charge carrier distribution and channel potential in BG, TG, DG devices were successfully simulated based on a FEM simulation. It was clear that the DG system produces a dual-channel, and that it has excellent control of charge carrier density in an organic semiconducting layer, which leads to higher I_{ON} and steeper *SS* than the single-gate devices. The conclusions also would apply to OTFTs that employ other organic semiconductor materials.

These results can be significant information for the better understanding of a low-voltage DG device operation, as well as for the realization of the high-performance and robust organic electronics.

Author Contributions: R.S., H.M. and S.T. designed the research and experiments. T.M. prepared and supplied the polymer semiconductor material. R.S., M.T., Y.T. and T.M. performed fabrication and characterization of the organic transistors. M.T. and H.M. carried out the device simulation. Each of the authors prepared figures and helped write the manuscript.

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Conflicts of Interest: The authors declare no conflict of interest.

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