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Influence of Substrate Modification with Dipole Monolayers on the Electrical Characteristics of Short-Channel Polymer Field-Effect Transistors

Takashi Nagase ^{1,2,*} , Takeshi Hirose ¹, Takashi Kobayashi ^{1,2}, Rieko Ueda ³, Akira Otomo ³ and Hiroyoshi Naito ^{1,2,*} 

¹ Department of Physics and Electronics, Osaka Prefecture University, Sakai 599-8531, Japan; takeo.yb@gmail.com (T.H.); tkobaya@pe.osakafu-u.ac.jp (T.K.)

² The Research Institute for Molecular Electronic Devices, Osaka Prefecture University, Sakai 599-8531, Japan

³ Advanced ICT Research Institute, National Institute of Information and Communications Technology, Kobe 651-2492, Japan; urieko@nict.go.jp (R.U.); akira_o@nict.go.jp (A.O.)

* Correspondence: nagase@pe.osakafu-u.ac.jp (T.N.); naito@pe.osakafu-u.ac.jp (H.N.); Tel.: +81-72-254-9266 (H.N.)

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Abstract: This study investigates the influence of self-assembled monolayer treatment of gate insulators on the electrical characteristics of bottom-gate/bottom-contact organic field-effect transistors (OFETs) with short channel lengths of 5 μm to 30 nm. The treatment of 3-chloropropyltrichlorosilane (CPTS) with large dipoles produces a high built-in electric field perpendicular to the SiO_2 gate insulator surface, which results in a threshold voltage shift and enhanced hole injection compared to the treatment of phenethyltrichlorosilane (PETS) with small dipoles. Pronounced parabolic drain current-voltage (I_D - V_D) characteristics due to a space-charge limited current are observed in short-channel OFETs based on poly(3-hexylthiophene) with CPTS-treated gate insulators. CPTS treatment on short-channel OFETs based on poly(9,9-dioctylfluorene-co-bithiophene) (F8T2) suppresses the nonlinear I_D increase in the low V_D region caused by the voltage drop at the Au/F8T2 contact. The influence of the increase in the net source-drain electric field associated with the reduced voltage drops on the channel-length dependence of the field-effect mobility of short-channel F8T2 FETs is also discussed.

Keywords: organic field-effect transistor; short-channel effect; self-assembled monolayer; dipole electric field

1. Introduction

There has been considerable interest in the development of organic field-effect transistors (OFETs) with high electrical performance because of their potential use in various organic devices, such as flexible displays, low-cost radio frequency identification tags, and large-area sensors [1–3]. Shrinking the channel length (L) of OFETs, which is typically several tens of micrometers, is a crucial issue for enhancing the performances of electronic circuits based on OFET devices because the operational speed and output current of FET devices are, respectively, proportional to μ/L^2 and μ/L , where μ is the field-effect mobility. However, reducing L to the sub-micrometer regime generally suffers from the high space-charge limited current (SCLC) associated with the application of a high source-drain electric field to the organic semiconductor; this results in parabolic drain current-drain voltage (I_D - V_D) characteristics without current saturation and an increase in the off current [4–8]. Such short-channel effects in OFETs have been reported to be suppressed by using ultrathin gate insulators (several

nanometers in thickness) [9] to ensure a gradual-channel approximation (the gate electric field in the channel is much larger than the source-drain electric field) [4,10].

We have previously studied the influence of the source electrode/organic semiconductor contact on the current–voltage characteristics of short-channel OFETs based on *p*-type organic semiconductors and reported that the parabolic I_D – V_D characteristics and high off current are suppressed by using organic semiconductors with high ionization potentials [11]. This behavior originates in the formation of Schottky barriers for hole injection at the source electrode/organic semiconductor contact, which reduces the SCLC and increases the effectiveness of the gate electric field in the channel because of the decrease in the net source-drain electric field. However, the formation of charge injection barriers also causes an increase in the threshold voltage of the short-channel OFETs and nonlinear I_D increase in the low V_D region. It has been reported that the threshold voltage of OFETs can be reduced by increasing the capacitance of gate insulators [12,13] and modifying the surfaces of gate insulators (next to the organic semiconductor channels) with self-assembled monolayers (SAMs) having polar end groups [14–20]. In particular, the latter approach uses a built-in electric field produced by the permanent dipoles of SAMs, which can provide an effective route to reduce the threshold voltage of short-channel OFETs without thinning the gate insulator to several nanometers.

In this study, we investigate the influence of the surface treatment of gate insulators with dipole SAMs on the electrical characteristics of short-channel OFETs with L of 5 μm to 30 nm fabricated using *p*-type polymer semiconductors with different ionization potentials.

2. Experimental

Figure 1a shows a schematic cross-section of the short-channel OFETs fabricated in this study. We used a heavily doped *n*-type Si wafer with a thermally-grown SiO_2 insulating layer (200 or 50 nm thick), which served as the gate electrode and gate insulator, respectively. Ti/Au (1–2 nm/30 nm) source-drain electrodes with different values of L (5 μm to 30 nm) were fabricated on the Si/ SiO_2 substrates by using electron-beam lithography and a lift-off process. The bottom Ti layer was employed to promote the adhesion of the Au electrodes to the SiO_2 surface. To ensure that carriers can be injected from the Au source electrode into the organic semiconductor layer [21], the thin Ti adhesion layer was used in our devices. The channel width (W) was scaled to maintain $W/L = 10$ to adjust the dimension of the output current in devices with different L .

Figure 1b shows the chemical structures of organosilanes used to form dipole SAMs on the SiO_2 surfaces. We used phenethyltrichlorosilane (PETS) and 3-chloropropyltrichlorosilane (CPTS), which have different polarities of dipole moments and form SAMs with similar levels of hydrophobicity [15,16]. CPTS has a large dipole moment pointing from chlorine toward trichlorosilane; this forms strong electron-withdrawing surfaces and leads to the accumulation of holes [15,16,18,22]. PETS has a relatively small dipole moment pointing toward the phenyl end group [16,23,24], which can form weak electron-donating surfaces. After the Si/ SiO_2 substrates with Ti/Au source-drain electrodes were cleaned with acetone and isopropanol in an ultrasonic bath and with an UV/ O_3 cleaner, the substrates were immersed in ~10 mM toluene solutions of the organosilanes in capped bottles for ~14 h to form SAMs on the SiO_2 surfaces. After SAMs were formed, the substrates were washed ultrasonically with fresh toluene, acetone, and isopropanol to remove any excessive layers and then baked at 150 $^\circ\text{C}$ for 1 h in a vacuum to enhance the cross-linking of the organosilane molecules. The water contact angles of the Si/ SiO_2 substrates treated with PETS and CPTS SAMs were 92 $^\circ$ and 84 $^\circ$, respectively.

For the organic semiconductors, we used *p*-type polymer semiconductors with different ionization potentials (IPs), as shown in Figure 1c: regioregular poly(3-hexylthiophene) (P3HT) (IP = 4.9 eV) and poly(9,9-dioctylfluorene-co-bithiophene) (F8T2) (IP = 5.5 eV) [25]. The organic semiconductor films were deposited on the SAM-treated Si/ SiO_2 substrates by spin-coating from 0.5–1 wt % toluene solutions. The obtained films were followed by thermal annealing in a vacuum to remove residual solvent and dopants such as oxygen and water from the semiconductor films [26]. The annealing

temperature of 100 °C was used to avoid the degradation of field-effect mobility in P3HT FETs caused by high-temperature annealing [27].

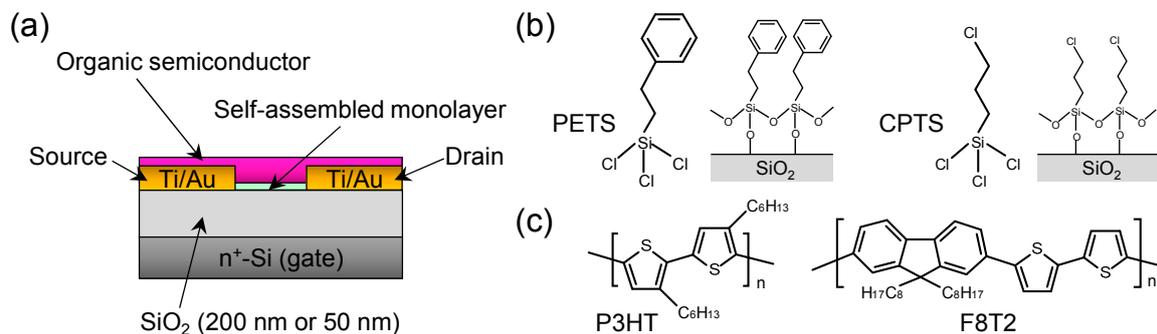


Figure 1. (a) Schematic cross-section of short-channel organic field-effect transistors (OFETs) fabricated in this study. Chemical structures of (b) organosilanes and (c) polymer semiconductors; PETS: phenethyltrichlorosilane; CPTS: 3-chloropropyltrichlorosilane; P3HT: poly(3-hexylthiophene); F8T2: poly(9,9-dioctylfluorene-co-bithiophene).

The electrical measurements of the fabricated OFET devices were performed in a vacuum at a probe station (Lake Shore Cryotronics TTP4 (Westerville, OH, USA)) by using source meters (Keithley 2611 and 2400 (Cleveland, OH, USA)) at room temperature. The field-effect mobility (μ) was calculated from the transfer characteristics in the saturation region by using the following standard FET equation:

$$I_D = \frac{\mu C_i W}{2L} (V_G - V_{th})^2 \quad (1)$$

where C_i is the capacitance per unit area for the gate insulator, V_G is the gate voltage, and V_{th} is the threshold voltage.

3. Results and Discussion

Figure 2a,b show the typical I_D - V_D (output) characteristics of short-channel P3HT-based FETs with L of 5 μm , 500 nm, and 30 nm fabricated on 200-nm-thick SiO_2 insulators treated with PETS and CPTS SAMs, respectively. The P3HT FETs with $L = 5 \mu\text{m}$ show typical output characteristics with clear current saturation. This can be attributed to the high gate electric field relative to the source-drain electric field, which ensures that the gate electric field determines the charge distribution within the channel (i.e., the gradual-channel approximation) [4,10]. As the channel length is reduced to the sub-micrometer regime, the output characteristics become parabolic, and the drain current at $V_G = 0 \text{ V}$ increases. Such behavior has been explained by the increase in the current flow to the bulk region of the organic semiconductor due to the SCLC [28]. The P3HT semiconductor allows forming ohmic contacts with the Au source-drain electrodes because of the small potential difference between the work function of Au (4.8 eV) and the ionization potential of P3HT (4.9 eV) [29]. Applying the source-drain voltage to the sub-micrometer channel leads to an extremely high source-drain electric field, which results in the SCLC significantly contributing to the drain current.

Figure 2c shows the I_D - V_G (transfer) characteristics of the short-channel P3HT FETs with PETS- and CPTS-treated SiO_2 gate insulators. The transfer characteristics of the devices with CPTS-treated gate insulators shift toward the positive V_G direction compared to that with PETS-treated gate insulators. Such behavior is consistent with the results reported for pentacene-based OFETs with $L = 30$ – $150 \mu\text{m}$ on SAM-treated SiO_2 insulators [15,16] and has been explained by the change in surface potential of the gate insulator by the permanent dipole of SAMs [14–20]. As shown in Figure 3, the electric field pointing toward the surface of the gate insulator produced by the dipole moment of CPTS causes the bending of molecular orbital levels of organic semiconductors toward high energy.

The upward bending of energy levels accumulates additional holes in the channel, which leads to the positive shift of transfer characteristics [15,16].

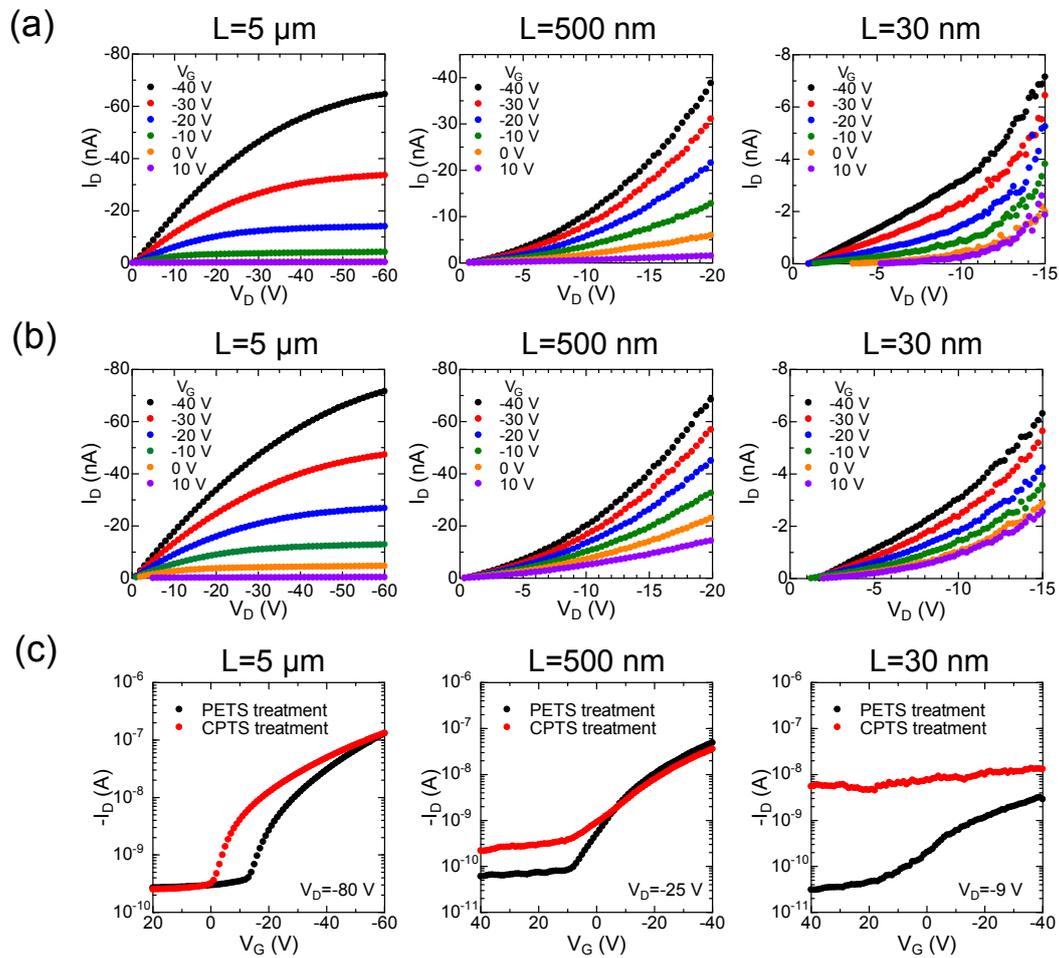


Figure 2. Output characteristics of P3HT FETs with L of 5 μm , 500 nm, and 30 nm on 200-nm-thick SiO_2 insulators treated with (a) PETS and (b) CPTS; and (c) their transfer characteristics.

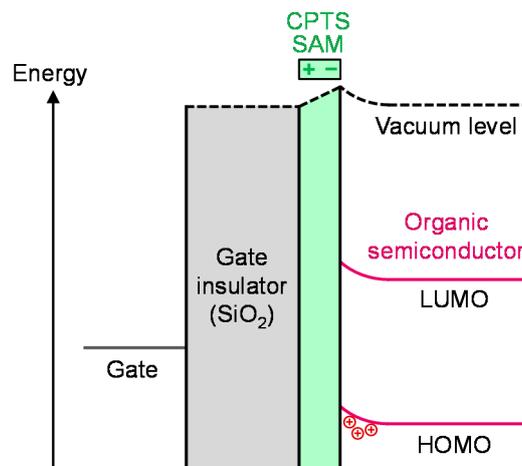


Figure 3. Schematic energy band diagram for bottom-gate OFETs with SiO_2 gate insulators treated with the CPTS SAM; LUMO: lowest unoccupied molecular orbital; HOMO: highest occupied molecular orbital; SAM: self-assembled monolayer.

The field-effect mobility of the P3HT FET devices with $L = 5 \mu\text{m}$ on the CPTS-treated gate insulators was $6.8 \pm 0.81 \times 10^{-4} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, which was slightly lower than that of the devices on the PETS-treated gate insulators ($1.4 \pm 0.13 \times 10^{-3} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$). Such a decrease in the mobility of P3HT FETs might be attributed to the smaller water contact angle of CPTS-treated gate insulators, since the ordering of organic semiconducting molecules in bottom-gate OFETs depends largely on the surface energy of gate insulators and a more hydrophobic surface gives a higher mobility [30,31]. It can be seen in the figures that the off current of the devices with CPTS-treated gate insulators remarkably increases as the channel length is reduced to 30 nm. Additionally, the devices with CPTS-treated gate insulators show a smaller increase in the drain current for the variation of the gate voltage, compared to the devices with PETS-treated gate insulators. These results clearly indicate that short-channel effects are more pronounced in the short-channel P3HT FETs fabricated on CPTS-treated gate insulators. This can be attributed to the improved injection of holes associated with the enhanced hole accumulation by CPTS SAMs, which increases the SCLC and reduces the modulation of the drain current by the gate voltage [8,9].

Figure 4 shows the output and transfer characteristics of short-channel F8T2-based FETs with $L = 5 \mu\text{m}$, 500 nm, and 30 nm that were fabricated on 200-nm-thick SiO_2 gate insulators treated with PETS and CPTS SAMs. In contrast to the P3HT FETs, the short-channel F8T2 FETs exhibit no parabolic output characteristics when the channel length is reduced, and the saturation of drain current is clearly observed in F8T2 FETs with $L = 30 \text{ nm}$ despite the use of thick SiO_2 gate insulators (200 nm). These results are attributed to the formation of Schottky barriers for hole injection because of the large potential difference between the work function of the source Au electrodes (4.8 eV) and ionization potential of the F8T2 semiconductors (5.5 eV) [29], which leads to contact-limited charge transport and, hence, suppresses the SCLC. The formation of Schottky barriers also causes the voltage drop at the source electrode/organic semiconductor contact, which reduces the net source-drain electric field at the channel region. The resulting increased effectiveness of the gate electric field at the channel region has been shown to enhance the current modulation in OFETs with nanometer channels [8,9,11].

It can be seen in Figure 4a,b that the large voltage drop at the Au/F8T2 contact causes a nonlinear increase in I_D in the low V_D region in the F8T2 FETs with PETS-treated gate insulators, whereas the nonlinearity of the I_D - V_D characteristics is decreased for short-channel F8T2 FETs with CPTS-treated gate insulators. These results are consistent with those observed for the short-channel P3HT FETs of Figure 2, which clearly indicates that a shift in the threshold voltage of transfer characteristics by CPTS SAMs involves the hole injection barriers at the source electrode/organic semiconductor interface being lowered. Such effects can manifest as the smaller modulation of the drain current by the gate voltage in F8T2 FETs with CPTS-treated gate insulators. This is because a lower hole injection barrier leads to a higher source-drain electric field and prevents the effective application of the gate electric field to the channel.

To clarify the difference in effects of the built-in electric field produced by the dipole SAM and increased gate electric field with thinner gate insulators, we investigated the electrical characteristics of short-channel P3HT and F8T2 FETs fabricated on thinner SiO_2 insulators (50 nm thick) treated with the PETS SAMs (Figure 5). As shown in Figure 5a, P3HT FETs with $L = 5 \mu\text{m}$ fabricated on 50-nm-thick gate insulators exhibit clearer current saturation behavior compared to devices on 200-nm-thick gate insulators (Figure 2a). Further, linear I_D - V_D characteristics in the low V_D region are obtained even for the device with $L = 500 \text{ nm}$ because of the increased gate electric field. Since OFETs require thin gate insulators (the thickness of a gate insulator is typically $<L/10$) to suppress the short-channel effects [4], P3HT FETs with $L = 30 \text{ nm}$ exhibit parabolic I_D - V_D characteristics even when 50-nm-thick SiO_2 insulators are used. For the F8T2 FETs shown in Figure 5b, good transistor characteristics with saturation of the drain current are observed in devices with $L = 30 \text{ nm}$. This results from the formation of voltage drops at electrode contacts, as mentioned above. In contrast to the F8T2 FETs on 200-nm-thick gate insulators treated with CPTS SAMs (Figure 4b), the short-channel F8T2 FETs on 50-nm-thick gate insulators treated with PETS SAMs still exhibit a nonlinear increase in the drain current in the

low- V_D region. The strength of the built-in electric field produced by the dipole SAMs has been reported to be on the order of $1\text{--}10\text{ MV cm}^{-1}$ [14–17,32,33], which is comparable to the gate electric field induced by applying gate voltages of $20\text{--}200\text{ V}$ for the 200-nm -thick SiO_2 gate insulator and $5\text{--}50\text{ V}$ for the 50-nm -thick SiO_2 gate insulators. Therefore, a similar degree of improvement in charge injection is expected in devices with thinner gate insulators. These results clearly show that using gate insulators modified with dipole SAMs is effective not only for increasing the threshold voltage, but also for reducing the charge injection barriers at the source electrode/organic semiconductor contacts of short-channel OFETs.

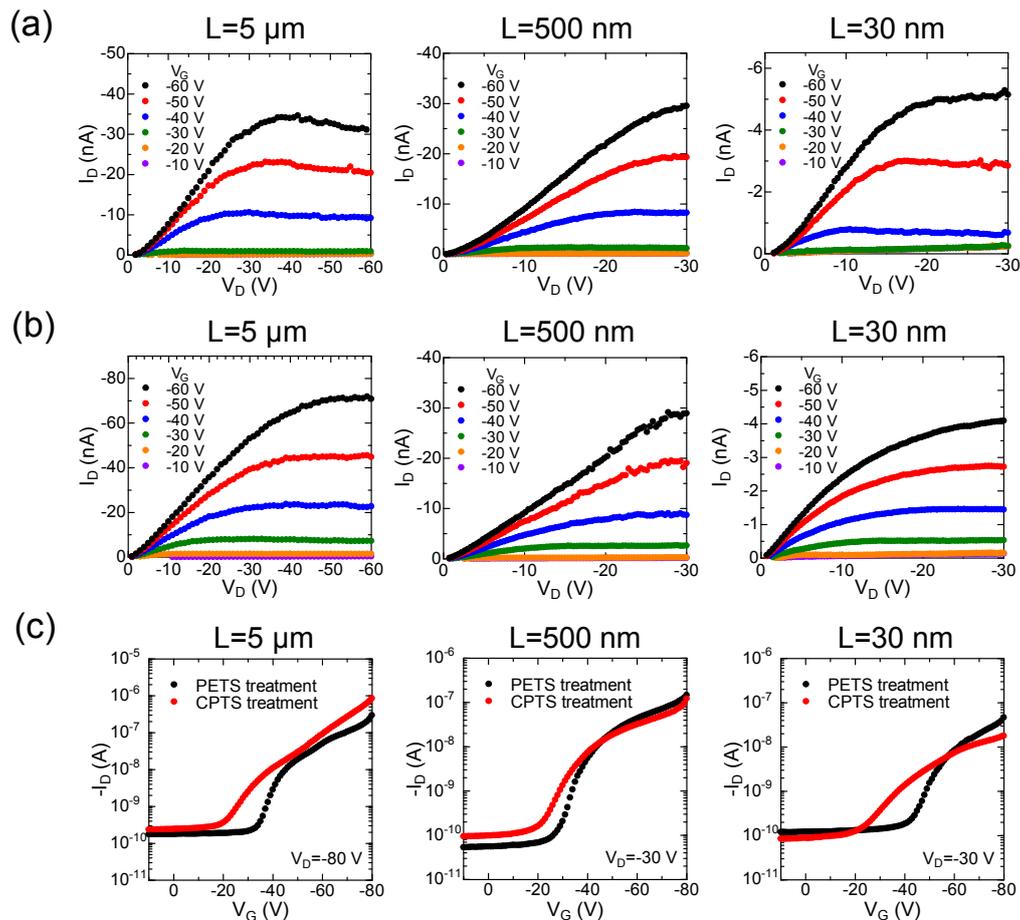


Figure 4. Output characteristics of F8T2 FETs with L of $5\ \mu\text{m}$, $500\ \text{nm}$, and $30\ \text{nm}$ on 200-nm -thick SiO_2 insulators treated with (a) PETS and (b) CPTS; and (c) their transfer characteristics.

Figure 6 shows the channel-length dependence of the field-effect mobilities of F8T2 FETs fabricated on PETS- and CPTS-treated SiO_2 gate insulators with different thicknesses (d_{ox}). In all devices, the field-effect mobility decreases with the channel length. Similar dependences have typically been observed in OFETs and explained by the increased influence of the contact resistance on the channel resistance [34]. This apparently reduces the field-effect mobility calculated with Equation (1). Therefore, the improved charge injection of F8T2 FETs by the CPTS treatment of gate insulators is expected to increase the field-effect mobility of short-channel F8T2 FETs. In fact, the devices with $L = 5\ \mu\text{m}$ formed on CPTS-treated gate insulators exhibited higher mobility ($3.9 \pm 0.77 \times 10^{-3}\ \text{cm}^2\ \text{V}^{-1}\ \text{s}^{-1}$) than those formed on PETS-treated gate insulators ($1.5 \pm 0.30 \times 10^{-3}\ \text{cm}^2\ \text{V}^{-1}\ \text{s}^{-1}$), as observed in Figure 6. The influence of the CPTS treatment on the mobility of F8T2 FETs is different from that of P3HT FETs shown in Figure 2, which can result from the larger influence of contact resistances on the field-effect mobility of F8T2 FETs [29]. However, the field-effect mobility of the devices with CPTS-treated gate

insulators shows a larger decrease as the channel length is reduced to the nanometer scale, as compared to those with PETS-treated gate insulators. Such behavior can be related to the smaller modulation of the drain current by the gate voltage observed in the F8T2 FETs with $L = 30$ nm by the CPTS treatment (Figure 4b). The results strongly suggest that the increased net source-drain electric field caused by the decreased voltage drop at the Au/F8T2 contact by the CPTS treatment reduces the effectiveness of the gate electric field in the channel, and it also leads to the apparent decrease in the field-effect mobility of OFETs with nanometer channels. Optimizing the dipole moments of SAM materials and using high-k gate dielectrics can further improve the field-effect mobility of nanochannel OFETs.

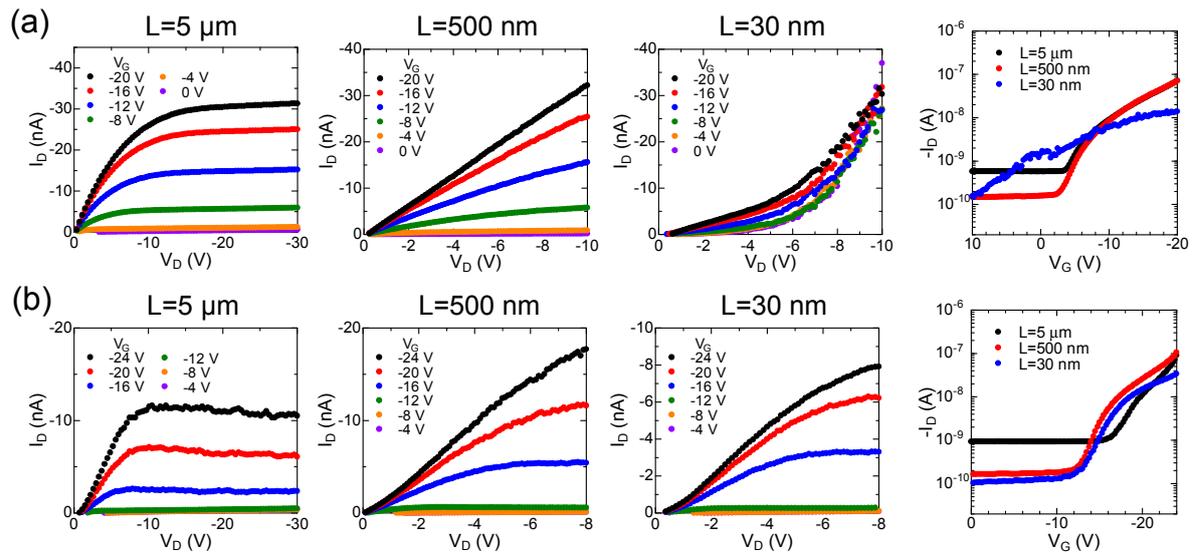


Figure 5. Output and transfer characteristics of (a) P3HT FETs and (b) F8T2 FETs with L of 5 μm , 500 nm, and 30 nm on 50-nm-thick SiO_2 insulators treated with PETS.

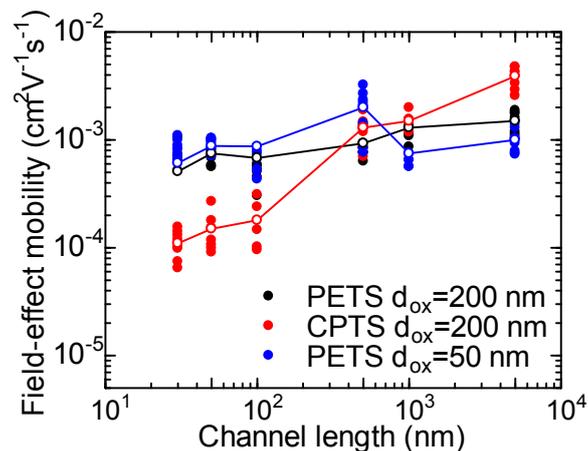


Figure 6. Channel length dependence of field-effect mobilities of F8T2 FETs on PETS- and CPTS-treated SiO_2 insulators with different SiO_2 thicknesses (d_{ox}). The open circles indicate average field-effect mobilities for each channel length.

4. Conclusions

We have investigated the electrical characteristics of short-channel OFETs based on polymer semiconductors with different ionization potentials formed on SiO_2 gate insulators treated with dipole SAMs. The built-in electric field produced by CPTS SAMs shifts the threshold voltage and reduces hole injection barriers at the source electrode/organic semiconductor contacts, which gives

the SCLC a larger influence on the current–voltage characteristics of P3HT FETs with nanometer channels compared with that of devices treated with PETS SAMs. The nonlinear increase in drain current in the low-voltage region of short-channel F8T2 FETs is improved by the CPTS treatment, which reduces the voltage drops at the Au/F8T2 contacts. The field-effect mobility of F8T2 FETs with CPTS-treated insulators exhibits a large apparent decrease as the channel length is reduced to the nanometer scale. Such behavior can be understood by the increase in the net source-drain electric field caused by the decrease in voltage drop at the Au/F8T2 contact by the CPTS treatment, which prevents the large modulation of drain current by the gate electric field and, hence, decreases the effective field-effect mobility.

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Conflicts of Interest: The authors declare no conflict of interest.

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