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An AC/DC LED Driver with Unity Power Factor and Soft Switching

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Abstract: Traditional light-emitting diode (LED) drivers with pulse-width modulation (PWM)-type converters suffer the problem of hard switching, leading to low circuit efficiency and low reliability. LED drivers supplied by alternating current (AC) line source generally require using an additional power-factor correction (PFC) stage to satisfy the regulations on power factor (PF) and total current harmonic distortion (THDi). It results in more circuit losses, especially when the active switch of the PFC stage operates at hard switching. This paper presents an alternating current-to-direct current (AC/DC) converter for driving high-brightness LEDs with the features of soft switching and high PF. The proposed single-stage circuit is formed by integrating a buck–boost converter and a buck converter. By elaborately rearranging the wirings between the circuit components of both converters, the power MOSFETs can be switched on at zero voltage. The operating modes at steady-state are analyzed and the mathematical equations for deriving circuit parameters are conducted. Finally, a prototype circuit for driving 60-W LEDs was built and measured. Based on the experimental results, the feasibility and satisfactory performance of the proposed LED driver are proved.

Keywords: hard switching; light-emitting diode (LED); power-factor correction; single stage; soft switching

1. Introduction

Nowadays, high-brightness light-emitting diodes (LEDs) are popularly used to replace incandescent and fluorescent lamps in many applications owing to their advantages of small size, high luminous efficiency, long lifespan, high reliability, and environmental friendliness [1–3]. On the purpose of increasing the utilization factor of the power electric equipment and reduce the electromagnetic interference (EMI), some regulations such as IEC 61000-3-2 and IEEE 519, are enacted to restrict the power factor (PF) and total current harmonic distortion (THDi) of the alternating current-to-direct current (AC/DC) LED drivers to a reasonable range. In order to meet these regulations, an additional converter serving as a power-factor correction (PFC) stage is added to a DC/DC converter of which the output voltage is adjusted to drive LEDs. It results in a LED driver with two power-process stages. Although the two-stage approaches have satisfactory performance, they are not cost-effective products since two converters and two corresponding control circuits are required. In addition, the two-stage approaches take two energy-conversion processes, and hence produce more losses including switching loss and conduction loss. Aiming to solve the shortcomings

of the two-stage approaches, many single-stage LED drivers have been proposed by integrating the PFC stage and the DC/DC stage [4–10].

Among the single-stage approaches, one power switch is commonly shared by the PFC stage and the DC/DC stage. Hence, they only use one control circuit and own the benefits of less component count and simply circuit topology. Nevertheless, the shared power switch should handle the current in both power-conversion stages, leading to more conducting losses. Moreover, the power switches of the single-stage approaches usually operate at hard switching and suffer the problem of high switching losses and high voltage and current stresses.

To further improve the circuit efficiency, literature proposed single-stage converters of which the power switches can fulfill soft switching to effectively reduce the switching losses [11–13]. Also, high PF and low THDi can be achieved. Unfortunately, there are still some defects required to be improved. In Reference [11], a coupled inductor is used in the buck–boost converter and its leakage inductance would incur high spike voltage across the power switch. In Reference [12], a boost converter serves as the PFC converter. Figure 1 shows the circuit topology that was proposed in Reference [12]. It integrates a boost converter and a buck converter. The boost converter serves as a PFC stage while the buck converter outputs a stable voltage to drive the load. High PF can be achieved, provided that the boost converter is operated at discontinuous current mode (DCM). However, a boost-typed PFC converter needs a high DC-link voltage to ensure DCM operation. It causes the circuit to require the use of high voltage rated components. For pursuing a better solution, this paper proposes a novel AC/DC converter to drive high power LEDs. The proposed circuit mainly consists of a buck–boost converter and a buck converter. Different from the circuit of Reference [12], when the boost-buck converter operates at DCM, it can obtain high power factor without needing a high DC-link voltage. A prototype circuit of 60-W was built and tested to verify the analytical predictions. Satisfactory performance is obtained from the experimental results.

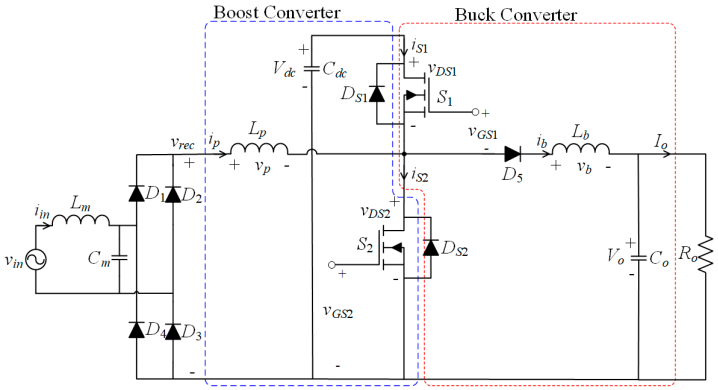

Figure 1. An integrated circuit with a boost converter and buck converter [12].

2. Proposed Circuit Topology and Operation Analysis

2.1. Circuit Topology

The proposed AC/DC LED driver is derived by integrating a buck–boost converter and a buck converter, as shown in Figure 2. Two MOSFETs serve as the active switches, S_1 and S_2. The diodes D_{S1} and D_{S2} are the intrinsic diodes of S_1 and S_2, respectively. The buck–boost converter is formed by L_p, S_2, D_{S1}, D_5, and C_{dc}. The buck converter is formed by L_b, S_1, D_{S2}, D_6, D_7, and C_o. The low-pass filter is composed of L_m and C_m. The control circuit is mainly a half-bridge controller that is widely adopted to control the active switches of a Class-D inverter. The power switches S_1 and S_2 are driven by two gated voltage, v_{GS1} and v_{GS2}. They are nonoverlapping and complementary rectangular-wave

waveform. There is a short duration called deadtime. During the deadtime, both v_{GS1} and v_{GS2} are zero volts. Neglecting the deadtime, both v_{GS1} and v_{GS2} have a duty ratio of 0.5.

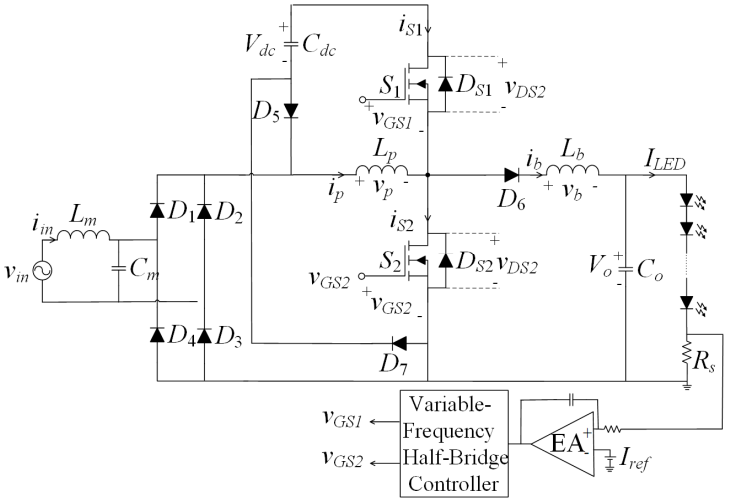

Figure 2. Proposed AC/DC LED driver.

As compared to the circuit topology proposed in Reference [12], the proposed one uses a buck–boost converter to serve the PFC stage while that of Reference [12] uses a boost converter. It is known that both converters operating at DCM can achieve nearly unity power factor. Nevertheless, when using a boost-typed PFC converter, it requires very high DC-link voltage to ensure unity power factor [14]. Although the proposed circuit needs to use two additional diodes, the voltage ratings of the circuit components could be lower than that of Reference [12].

2.2. Operation Analysis

For simplifying the circuit analysis, the following assumptions are made:

1. All the semiconductor devices are ideal except that the parasitic capacitances and the intrinsic diodes of the MOSFETs are considered.
2. The DC-link capacitor C_{dc} and the output capacitor C_o are both large enough; thus, the DC-link voltage V_{dc} and the output voltage V_o can be regarded as constant.
3. The switching frequency of the active switches, f_s, is much higher than that of the input-line voltage, f_s. Hence, the input-line voltage is considered as constant during each high-frequency cycle.

At steady-state operation, the circuit operation can be divided into six modes in one high-frequency cycle. In order to make both power switches achieve zero-voltage switching (ZVS), both converters should be operated at DCM. These six operation modes are shown in Figure 3, where v_{rec} represents the rectified input voltage. The illustrative current and voltage waveforms of some key components are shown in Figure 4.

2.2.1. Mode I ($t_0 < t < t_1$; in Figure 3a)

Prior to this mode, S_1 is on and the DC link voltage V_{dc} supplies the buck-inductor current i_b. Mode I begins at the instant of turning off S_1. Thereby, i_b would discharge the parasitic capacitance (C_{DS2}) between the drain and source of S_2. As soon as the voltage across C_{DS2} decreases to -0.7 V, D_{S2} is forward-biased to conduct i_b. The gated voltage v_{GS2} becomes high level after the short deadtime and the current flowing through D_{S2} diverts to flow from the source to drain of the MOSFET S_2. By this

way, the voltage across S_2 is clamped at near zero voltage. The voltage across the buck inductor L_b is minus of the output voltage V_o and hence, i_b decreases linearly.

$$v_b(t) = -V_o \tag{1}$$

$$i_b(t) = i_b(t_0) - \frac{V_o}{L_b}(t - t_0) \tag{2}$$

Since S_2 is on, the voltage across the buck–boost inductor L_p is equal to v_{rec}.

$$v_p(t) = v_{rec}(t) = V_m|sin(2\pi f_L t)|, \tag{3}$$

where f_L and V_m respectively represent the frequency and the amplitude of the input-line voltage.

Since the buck–boost converter is operated at DCM, the buck–boost current i_p linearly increases from zero.

$$i_p(t) = \frac{v_{rec}(t)}{L_p}(t - t_0) = \frac{V_m|sin(2\pi f_L t)|}{L_p}(t - t_0) \tag{4}$$

In this mode, i_b is higher than i_p. There are two current loops for i_b. Parts of i_b flow through S_2, while the rest of i_b is equal to i_p, which flows through L_p and the line-voltage source. This mode ends when i_p becomes higher than i_b.

2.2.2. Mode II ($t_1 < t < t_2$; in Figure 3b)

At the beginning of Mode II, i_p becomes higher than i_b and the current flowing through S_2 changes direction. Parts of i_p flow through S_2 from its drain to source, while the rest flows to the buck converter. The voltage and current equations for v_b, v_p, i_b and i_p are the same as (1)–(4) in Mode I. The current i_b keeps decreasing and i_p keeps increasing. When i_b decreases to zero, Mode II ends.

2.2.3. Mode III ($t_2 < t < t_3$; in Figure 3c)

The current i_b is zero. S_2 is kept on and i_p continues to increase. Mode III ends when the gated voltage v_{GS2} becomes low level to turn off S_2, and the circuit operation enters Mode IV.

2.2.4. Mode IV ($t_3 < t < t_4$; in Figure 3d)

The current i_p reach a peak value of each high-frequency cycle at the instant of turning off S_2. The current i_p will be diverted from S_2 to discharge the parasitic capacitance (C_{DS1}) between the drain and source of S_1. As soon as the voltage across C_{DS1} decreases to -0.7 V, D_{S1} is forward biased to conduct i_p. The gated voltage v_{GS1} becomes high level after the short deadtime and i_p diverts from D_{S1} to flow through S_1 from its source to drain. By this way, the voltage across S_1 is clamped at near zero voltage. Now, the current loop of i_p is L_p–S_1–C_{dc}–D_5 and the DC-link capacitance C_{dc} is charged. The voltage across L_p is equal to $-V_{dc}$ and hence, i_p decrease linearly.

$$v_p(t) = -V_{dc} \tag{5}$$

$$i_p(t) = i_p(t_3) - \frac{V_{dc}}{L_p}(t - t_3) \tag{6}$$

On the other hand, the current i_b starts to increase from zero with the current loop: L_p–D_6–L_b–C_o–v_{rec}. The voltage and current equations for the buck inductor can be expressed as:

$$v_b = v_{rec}(t) + V_{dc} - V_o, \tag{7}$$

$$i_b(t) = \frac{V_m|sin(2\pi f_L t)| + V_{dc} - V_o}{L_b}(t - t_3). \tag{8}$$

In this mode, i_p is higher than i_b. There are two current loops for i_p. Parts of i_p flow through S_1 to charge C_{dc}, while its residual is equal to i_b and flows into the buck converter. This mode ends when i_b becomes higher than i_p.

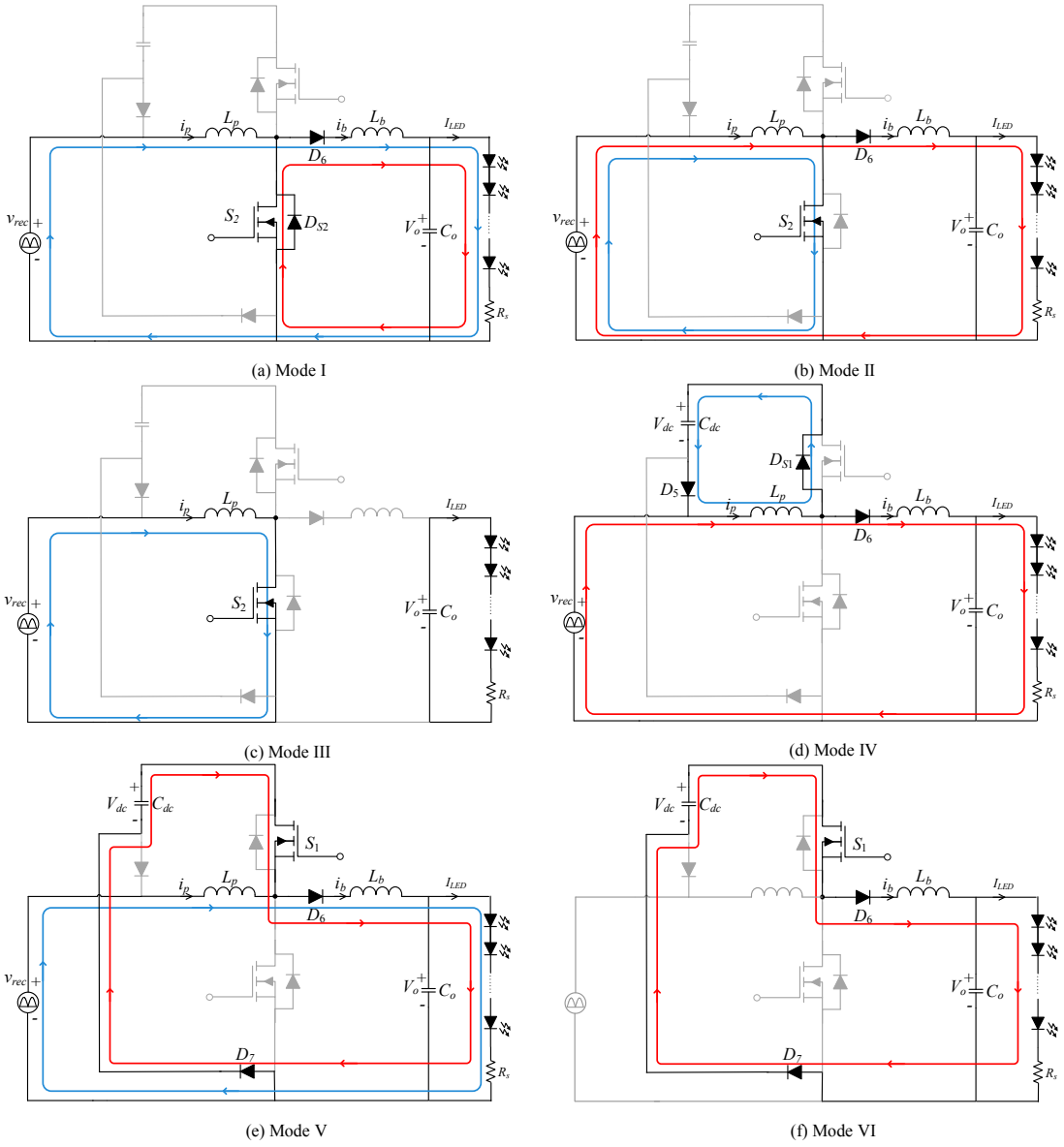

Figure 3. Equivalent circuit of operation modes: (**a**) Modes I–(**f**) Modes VI.

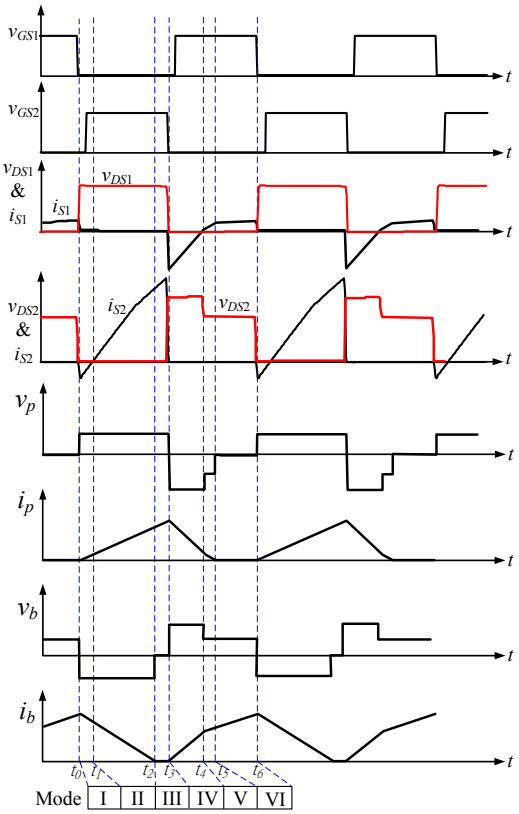

Figure 4. Theoretical waveforms.

2.2.5. Mode V ($t_4 < t < t_5$; in Figure 3e)

At the beginning of Mode V, i_b becomes higher than i_p and the current flowing through S_1 changes direction. There are two current loops for i_b. Parts of i_b are supplied from the DC-link voltage and flows through S_1, D_6, L_b, C_o, and D_7 while the rest is equal to i_p and flow through D_6, L_b, C_o, the line voltage source and L_p. The voltages across L_b and L_p can be respectively expressed as:

$$v_b(t) = V_{dc} - V_o, \tag{9}$$

$$v_p(t) = v_{rec}(t) - V_{dc}. \tag{10}$$

The current equations of i_p and i_p can be expressed as

$$i_b(t) = i_b(t_4) + \frac{V_{dc} - V_o}{L_b}(t - t_4), \tag{11}$$

$$i_p(t) = i_p(t_4) - \frac{V_{dc} - V_m|sin(2\pi f_L t)|}{L_p}(t - t_4). \tag{12}$$

The current i_b increases linearly. From Equation (12), i_p would decrease when V_{dc} is designed higher than the amplitude of the input-line voltage. This mode ends when i_p decreases to zero.

2.2.6. Mode VI ($t_5 < t < t_6$; in Figure 3f)

In this mode, S_1 is remained on. Only the current i_b keeps increasing linearly with the current path V_{dc}–S_1–D_6–L_b–C_o–D_7. This mode ends at the time when v_{GS1} becomes low level to turn off S_1 and the circuit operation returns to Mode I of the next high-frequency cycle.

Base on the discussion in Mode I and Mode IV, as soon as the active switch of one converter is turned off, its inductor current diverts from the active switch. The diverting current flows through the parasitic capacitance of the active switch of the other converter. The parasitic capacitance is discharged and the voltage across it decreases. When the voltage across the parasitic capacitance decreases to −0.7 V, the intrinsic diode of the active switch turns on to conduct current and the voltage across the active switch is clamped at almost zero volts (−0.7 V). The gated voltage of the active switch should become high level before the current change polarity. Now, the active switch is ready for conducting current and its voltage is almost zero. When the switch current increases to pass zero and becomes positive, the positive current will flow from the source to drain of the active switch. By this way, the active switch is turned on at ZVS. For ensuring the ZVS operation, the deadtime of the two gated voltage (v_{GS1} and v_{GS2}) should be longer than the duration for discharging the parasitic capacitance to −0.7 V. The parasitic capacitance of the MOSFET is very small. The parasitic capacitance would be fully discharged very quickly. Therefore, the deadtime could be short. The half-bridge controller commonly used in markets generally has the deadtime long enough to meet this requirement.

3. Design Equation

3.1. Buck–Boost Converter Equations

It is known that the maximum value of the buck–boost inductor current happens at the time when the input-line voltage is at the peak point of the sinusoidal waveform. For ensuring DCM operation at the peak, the following inequality should be satisfied.

$$V_{dc} > \frac{DV_m}{1-D}, \tag{13}$$

where D is the duty ratio of the active switch. If Equation (13) is satisfied, the buck–boost converter can operate at DCM within the whole cycle of the input-line voltage.

For an AC/DC buck–boost converter operating at DCM, the input-line current and the input power can be expressed as Equations (14) and (15), respectively [15].

$$i_{in}(t) = \frac{V_m D^2}{2L_p f_s} sin(2\pi f_L t), \tag{14}$$

$$P_{in} = \frac{{V_m}^2 D^2}{4L_p f_s}, \tag{15}$$

As shown in Equation (14), the input-line current is purely sinusoidal and in phase with the input-line voltage. It means that low THDi and high PF can be achieved by operating the buck–boost converter at DCM. From Equation (15), the output power can be expressed as

$$P_0 = \eta P_{in} = \frac{\eta {V_m}^2 D^2}{4L_p f_s}, \tag{16}$$

where η represents the energy-conversion efficiency of the proposed circuit.

3.2. Buck Converter Equations

The buck converter is also designed to operate at DCM. For ensuring DCM operation, the output voltage should be high enough to satisfy the following inequality [12].

$$V_{dc} < \left(1 + \frac{1}{2D}\right) V_o \tag{17}$$

Besides this, the average of the buck inductor current is equal to the output current and can be expressed as [12]:

$$\overline{i_b} = \frac{D^2(V_{dc} - V_o)V_{dc}}{2L_b V_o f_s} = I_o. \quad (18)$$

From Equation (17), the output power can be expressed as:

$$P_o = V_o I_o = \frac{D^2(V_{dc} - V_o)V_{dc}}{2L_b f_s}. \quad (19)$$

4. Parameters Design and Experimental Results

4.1. Parameters Design

A prototype circuit of 60-W was designed and built to drive sixty 1-W high brightness LEDs connected in series. The rated voltage and current of each LED is 3.25 V and 0.308 A, respectively. The specification of the proposed LED driver is shown in Table 1.

By substituting the values of v_{in}, V_o, and D into Equations (13) and (17), the constraint of V_{dc} can be obtained. In this illustrative example, V_{dc} is designed to be 350 V. Assuming 93% circuit efficiency, the buck–boost inductor can be calculated from Equation (16).

$$L_p = \frac{\eta {V_m}^2 D^2}{4P_o f_s} = \frac{0.93 \times \left(110\sqrt{2}\right)^2 \times 0.5^2}{4 \times 60 \times 50 \times 10^3} = 0.47 \text{ mH}$$

The buck inductor can be calculated from Equation (19).

$$L_b = \frac{D^2(V_{dc} - V_o)V_{dc}}{2P_o f_s} = \frac{0.5^2 \times (350 - 195) \times 350}{2 \times 60 \times 50 \times 10^3} = 2.26 \text{ mH}$$

In order to achieve a sinusoidal input current, a low-pass filter is required to cascade in front of the rectifier bridge to filter out the high-frequency current induced from the buck–boost converter. L_m and C_m are designed to perform the ow-pass filter. By rule of thumb, the corner frequency of a low-pass filter should be lower than one eighth of the switching frequency. Here, the corner frequency is designed to be about 5 kHz, and L_m and C_m are determined to be L_m = 2.0 mH, C_m = 0.47 μF.

The circuit parameters of this prototype circuit are listed in Table 2.

Table 1. Specification of the proposed light-emitting diode (LED) driver.

Input voltage v_{in}	110 V ± 10% (rms), 60 Hz
Output power P_o	60 W
Output voltage V_o	3.25 V × 60 = 195 V
Output Current I_o	0.308 A
Equivalent LED Resistance R_{LED}	633 Ω
Switching frequency f_s	50 kHz
Duty ratio D	0.5

Table 2. Circuit parameters.

The low-pass inductance L_m	2.0 mH
The low-pass capacitance C_m	0.47 μF
Dc-link capacitance C_{dc}	100 μF
Output capacitance C_o	100 μF
Buck–boost inductor L_p	0.47 mH
Buck inductor L_b	2.26 mH
Active switches S_1, S_2	IRF840
Diodes D_1–D_7	MUR460

4.2. Experimental Results

From Equation (16), it is noted that the switching frequency is used to control the output power. As seen in Figure 2, the LED current is sensed by a series resistor R_s. The voltage across R_s which is proportional to the LED current is compared to a reference value I_{ref}, and their difference is amplified by an operational amplifier in the error amplifier (EA). The output of the operation amplifier is sent to the half-bridge controller which mainly consists of a double-ended controller (L6599). The outputs of the half-bridge controller are two complementary waveforms (v_{GS1}, v_{GS2}) of which the frequency is regulated [12]. By this way, the switching frequency of the active switch is controlled to regulate the LED current. Figure 5 shows the measured waveforms of the input voltage and input current. The rms values of the input voltage and current are 112.4 V and 0.57 A, respectively. It can be observed that the input current is sinusoidal and in phase with the input voltage. The power quality in the input line is measured with a power analyzer (PowerLogic PM1000, Schneider Electric, Rueil-Malmaison, France). The measured PF is greater than 0.99, and the THDi is 3.5%. The inductor currents of both converters are shown in Figure 6 to indicate the DCM operation. There are spike currents in both the buck–boost inductor and the buck inductor. Theoretically, it is impossible to have a current spike in an inductor; otherwise, the voltage across the inductor would be tremendous high. The measured spike current in the buck–boost inductor and the buck inductor is believed to result from the interference voltage when one active switch is turned off. Figure 7 shows the waveforms of the output voltage and output current, which are well consistent with the design values. The DC values of the output voltage and current are 198.5 V and 0.304 A, respectively. In addition, the input power and output power are both measured with an oscilloscope. The measured values are 64 W and 60.3 W, respectively. The circuit efficiency is calculated to be 94.2%. Figure 8 shows waveforms of the voltage and current of the active switches. As shown, the switch current always increases from negative to positive. Its intrinsic diode conducts the negative current and clamps the switch voltage at almost zero volts. The active switch would naturally turn on as the switch current becomes positive, leading to ZVS operation. In the prototype circuit, MOSFET IRF840 serves the active switch. The current rating of the source-drain current (i.e., the current rating of the intrinsic diode) is 8 A maximum. It is seen in Figure 8, the maximum value of the diode current is about 3.5 A. Besides, the current in the intrinsic diode decreases linearly to zero. It means that the intrinsic diodes would turn off at zero current. Therefore, there is no faster diode in parallel with the active switch to replace the intrinsic diode. Figure 9 shows the prototype LED driver.

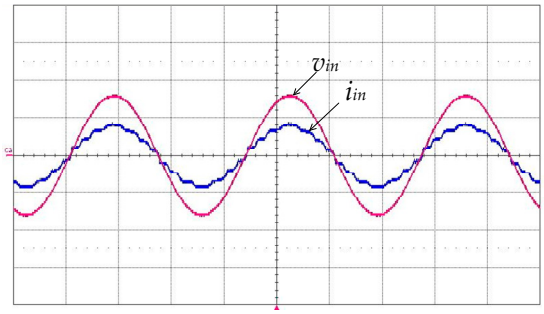

Figure 5. Waveforms of the input voltage and current. (v_{in}: 100 V/div, i_{in}: 1 A/div, time: 5 ms/div).

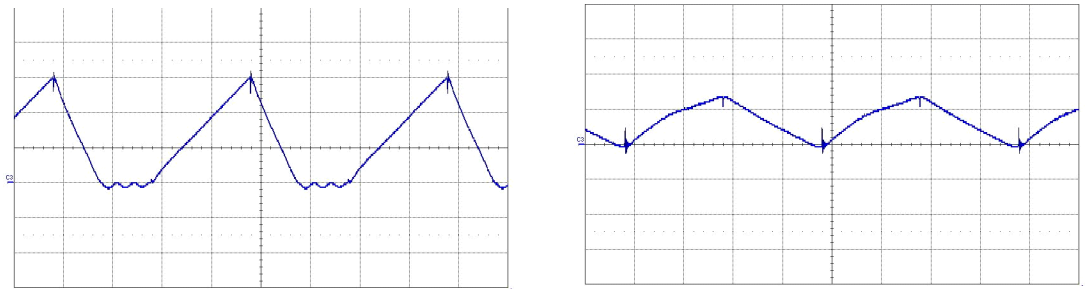

Figure 6. Waveforms of inductor currents (**a**) Buck–boost inductor current i_p (i_p: 1 A/div, time: 5μs/div) and (**b**) Buck inductor current i_b (i_b: 0.5 A/div, time: 5 μs/div).

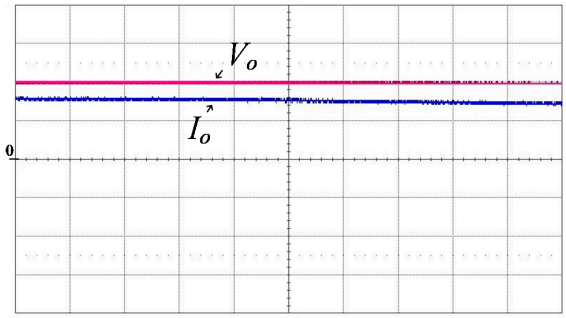

Figure 7. Waveforms of V_o and I_o. (V_o: 100 V/div, I_o: 0.2 A/div, time: 5 ms/div).

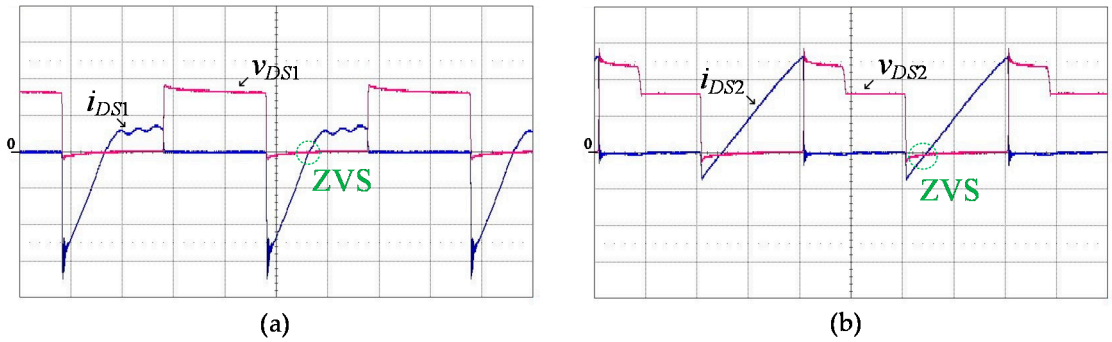

Figure 8. Waveforms of the voltages and currents of the active switches. (**a**) v_{DS1} and i_{S1} (v_{DS1}: 200 V/div, i_{S1}: 1 A/div, time: 5 μs/div) and (**b**) v_{DS2} and i_{S2} (v_{DS1}: 200 V/div, i_{S1}: 1 A/div, time: 5 μs/div).

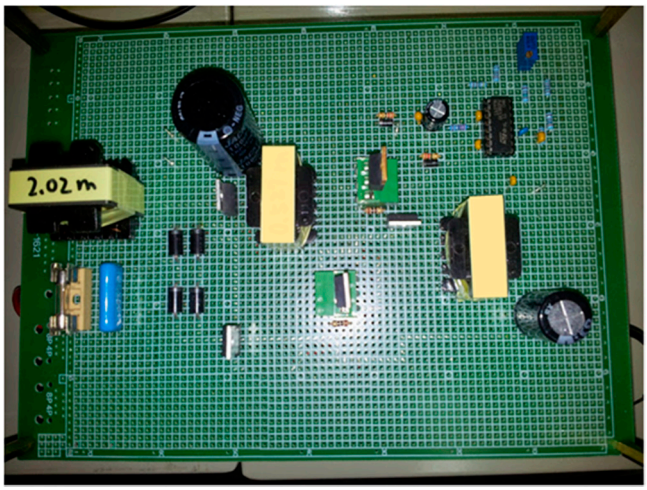

Figure 9. The prototype LED driver.

5. Conclusions

A novel AC/DC LED driver derived by integrating a buck–boost converter and a buck converter is proposed. The buck–boost converter serves as PFC converter to achieve high PF and low THDi while the buck converter steps down the DC-link voltage to drive high power white LEDs. A 60-W prototype circuit is built and tested to verify the theoretical analyses. Both the active switches can achieve ZVS. Experimental results show that the proposed circuit performs satisfactorily. A nearly unity PF (>0.99) and low THDi (3.5%) are achieved. With ZVS operation on both active power switches, the proposed circuit efficiency is as high as 94.2%.

Author Contributions: Y.-N.C. and H.-L.C. conceived and designed the circuit; C.-H.C. and H.-C.Y. performed circuit simulations and designed parameters of the circuit components; R.-Z.L. carried out the prototype LED driver, and measured as well as analyzed experimental results with the guidance from H.-L.C.; H.-L.C. wrote the paper and Y.-N.C. revised it for submission.

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Conflicts of Interest: The authors declare no conflict of interest.

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