applied sciences

MDPI

Article

Reduction of Bias and Light Instability of Mixed Oxide Thin-Film Transistors

Mallory Mativenga *, Jae Gwang Um and Jin Jang

Department of Information Display, Kung Hee University, Seoul 02447, Korea; jkum@tft.khu.ac.kr (J.G.U.); jjang@khu.ac.kr (J.J.)

* Correspondence: mallory@khu.ac.kr; Tel.: +82-2-961-9504

Received: 31 July 2017; Accepted: 25 August 2017; Published: 29 August 2017

Featured Application: Active-matrix displays and sensors.

Abstract: Despite their potential use as pixel-switching elements in displays, the bias and light instability of mixed oxide semiconductor thin-film transistors (TFTs) still limit their application to commercial products. Lack of reproducible results due to the sensitivity of the mixed oxides to air exposure and chemical contamination during or after fabrication hinders any progress towards the achievement of stable performance. Consequently, one finds in literature several theories and mechanisms, all justified, but most of them conflict despite being on the same subject matter. In this study, we show that under an optimized fabrication process, which involves the in situ passivation of a mixed oxide semiconductor, we can reduce the bias and light instability of the mixed-oxide semiconductor TFTs by decreasing the semiconductor thickness. We achieve a negligible threshold voltage shift under negative bias combined with light illumination stress when the mixed oxide semiconductor thickness is around three nanometers. The improvement of stability in the thin mixed-oxide semiconductor TFTs is due to a reduced number of oxygen-vacancy defects in the bulk of the semiconductor, as their total number decreases with decreasing thickness. Under the optimized fabrication process, bulk, rather than interfacial defects, thus seem to be the main source of the bias and light instability in mixed oxide TFTs.

Keywords: oxide; stability; thin film transistor

1. Introduction

The interest in mixed oxide semiconductor-based thin-film transistors (TFTs) for applications in active-matrix displays (AMDs) has generated a large body of experimental and theoretical studies devoted to mixed oxide semiconductors, particularly amorphous indium-gallium zinc-oxide (a-IGZO) [1,2]. For applications in AMDs, reliability and stability of the TFTs used as pixel-switching elements are of primary concern [3]. Stability against negative-gate bias stress combined with visible light illumination (NBIS) is of particular importance, given that TFTs in a display pixel operate in an illuminated environment. Although many investigations have focused on the effects of NBIS, which include persistent negative threshold-voltage (V_{TH}) shift [4–7], they have not yet found ways to suppress them completely. Since the TFTs' V_{TH} stability has a strong bearing on display uniformity, lifetime, and pixel architecture [3], some groups have proposed subjecting mixed oxide TFTs to post-deposition annealing at high temperatures under wet [8], oxygenated [9], ozonated [10], or nitrogenated environments as a way of minimizing the effects of NBIS. Other groups have proposed the use of light shields, nitrogen cap layers [11], high-quality dielectrics (both as gate insulators [12], and passivation [13] layers), but such methods suppress the NBIS-induced instability only to limited extents.

Recently, bulk accumulation, which is achieved by the use of a dual-gate structure in which the top gate and bottom gate are electrically shorted together, has been shown to reduce the NBIS instability of

mixed oxide TFTs with thin semiconductor layers (<25 nm) [14,15]. However, similar to other stability improvement methods, bulk accumulation also suppresses the NBIS instability only to a limited extent. In addition, several reports have indicated the importance of the semiconductor thickness in the stability of the mixed oxide TFTs but different groups reached different conclusions [8,16–18]. For instance, for some groups, the bias stability of the TFTs became better as semiconductor thickness increased [16,17], whereas, for other groups, it worsened [18]. Nomura et al. also showed opposite trends for wet-annealed and non-annealed TFTs [8]. For wet-annealed TFTs, the V_{TH} shift (ΔV_{TH}) decreased with increasing semiconductor thickness, and for non-annealed TFTs, ΔV_{TH} increased with increasing semiconductor thickness. Nomura et al., therefore, concluded that the density of trap states increased with increasing semiconductor thickness in the non-annealed TFTs, whereas in the wet-annealed TFTs, there was almost no bulk effect.

In this study, we investigate the effect of semiconductor thickness on the stability of mixed oxide semiconductor TFTs against NBIS. In contrast to previous reports [8,16–20], we fabricate the TFTs using an optimized fabrication process, which involves the in situ passivation of the mixed oxide semiconductor, and we investigate very thin (3–10 nm) and thick (20–100 nm) semiconductor layers. For the mixed oxide, we use the a-IGZO semiconductor, given that a-IGZO TFTs can be built with the simple and cost-effective inverted staggered structure, and exhibit high field-effect mobility (μ_{FE}) and low V_{TH} [1,2].

2. Materials and Methods

Figure 1 illustrates the fabrication process of the a-IGZO TFTs investigated in this study. The process begins with the deposition of a 60-nm thick Mo layer on glass by sputtering and its patterning by standard lithography to form the gate electrode (Figure 1a). This is followed by the consecutive deposition of a 250 nm-thick SiO_2 layer by plasma-enhanced chemical vapor deposition (PECVD) as the gate insulator at 380 °C, deposition of an a-IGZO layer by sputtering at 200 °C, and deposition of a 100 nm-thick SiO_2 back passivation layer by PECVD at 200 °C in a cluster deposition tool, without breaking vacuum (Figure 1b). This step ensures the in situ passivation of the a-IGZO, immediately after deposition, to realize an uncontaminated and very stable a-IGZO layer that is necessary for the detection of intrinsic characteristics, rather than fabrication process-related variations. Samples with a-IGZO thickness (t_{IGZO}) of ~3, 5, 10, 20, 50, and 100 nm are fabricated. The sputtering of the a-IGZO is performed using a polycrystalline IGZO target (In_2O_3:Ga_2O_3:ZnO = 1:1:1 mol %) at 200 °C. The Ar:O_2 gas ratio is set at 4:8 for sputtering.

The top SiO_2 layer, which is a protective layer, commonly referred to as the "etch stopper", is patterned to expose the source and drain regions for the metal contacts (Figure 1c). During the fabrication process, the etch stopper protects the a-IGZO from exposure to air and also shields it from being etched away or contaminated by the etchant used to define the source/drain electrodes. The patterning of the a-IGZO layer to form active islands (Figure 1d) follows the etch-stopper process. Deposition of another Mo layer and its patterning to form the source/drain electrode contacts and a 200 nm-thick SiO_2 layer as the final TFT passivation layer (Figure 1e) follows the a-GZO process. The final step is the annealing of the TFTs at 250 °C in vacuum to ensure a reproducible unstressed state.

We confirmed TFT layer thicknesses by means of transmission electron microscopy (TEM) imaging as shown in Figure 2 and determined the crystallinity and chemical composition of the IGZO layers by X-ray diffraction (XRD) patterns and X-ray photon electron spectroscopy (XPS), respectively. In XRD (Figure 3a), the IGZO films do not exhibit sharp diffraction peaks assignable to a crystalline phase but have two halo peaks at 32° and 56°, indicating that they are amorphous. The a-IGZO film is transparent in the visible range (Figure 3b), owing to its large band gap = ~3.2 eV (Figure 3c). XPS results show that the a-IGZO chemical composition is In:Ga:Zn = 3:2:1 in an atomic ratio (Figure 3d).

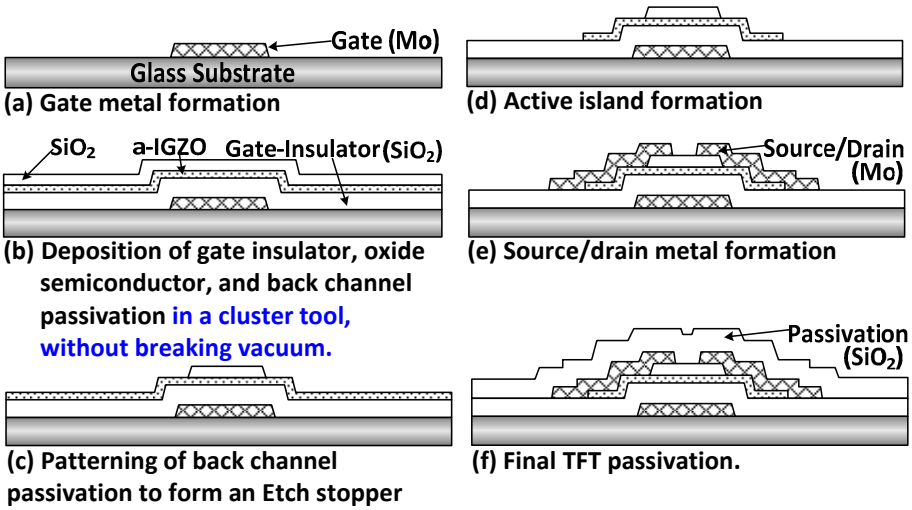

Figure 1. Optimized mixed oxide thin-film transistor passivation. In (**b**), the consecutive deposition of a SiO_2 layer by plasma-enhanced chemical vapor deposition (PECVD) as the gate-insulator, deposition of an amorphous indium-gallium zinc-oxide (a-IGZO) layer by sputtering, and deposition of a SiO_2 back passivation layer by PECVD in a cluster deposition tool, without breaking vacuum, ensures the in situ passivation of the a-IGZO, immediately after deposition. This, in turn, ensures an uncontaminated and very stable a-IGZO layer, necessary for the detection of intrinsic characteristics, rather than fabrication process-related variations.

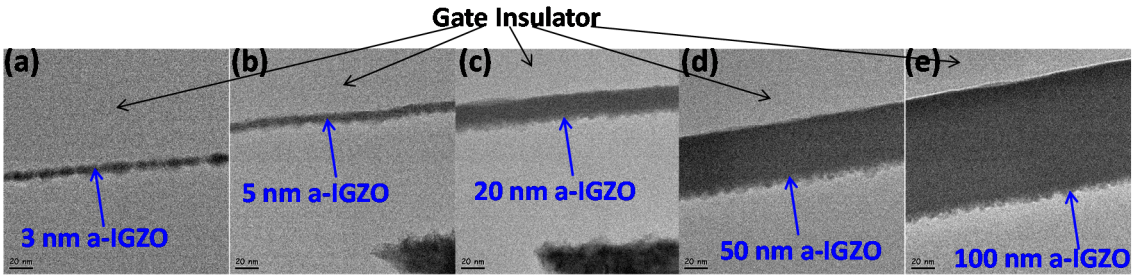

Figure 2. Transmission electron microscope images of parts of thin-film transistors with amorphous indium-gallium zinc-oxide thickness of (**a**) 3 nm, (**b**) 5 nm, (**c**) 20 nm, (**d**) 50 nm, and (**e**) 100 nm.

We measured the current-voltage (*I*-*V*) characteristics using the Agilent 4156C precision semiconductor parameter analyzer, and the capacitance-voltage (*C*-*V*) characteristics using the Agilent E4980A Precision LCR meter by superimposing the gate DC voltage (V_{GS}) on a small AC signal (0.1 V) of frequency (f) at 1 kHz, keeping the source and drain shorted. Note that the f of the AC signal should be low enough to guarantee quasi-static conditions, $1/f \gg$ RC time constant of the system, so that the induced AC variation of surface potential Ψ_S can be considered constant along the channel [21]. Consistent with previous reports, we accomplished the NBIS by holding the TFT V_{GS} at −20 V for 10,000 s, while biasing the source and drain electrodes at zero volts, under white-light illumination (9000 nit) and at room temperature [8,16–18]. TFT parameters were derived from the conventional metal-oxide, semiconductor field-effect transistor (MOSFET) equation. The μ_{FE} was derived from the transconductance (g_M) with V_{DS} = 0.1 V at a gate voltage (V_{GS}) of 10 V. The V_{ON} was taken as the V_{GS} at which the drain current (I_{DS}) started to monotonically increase. The subthreshold voltage swing (SS) was taken as the minimum value of $(d \log(I_{DS})/d\, V_{GS})^{-1}$. We extracted the density of states (DOS) of the a-IGZO as a function of thickness before and after NBIS using a method, which involves a combined analysis of the TFTs' I-V and C-V characteristics [21].

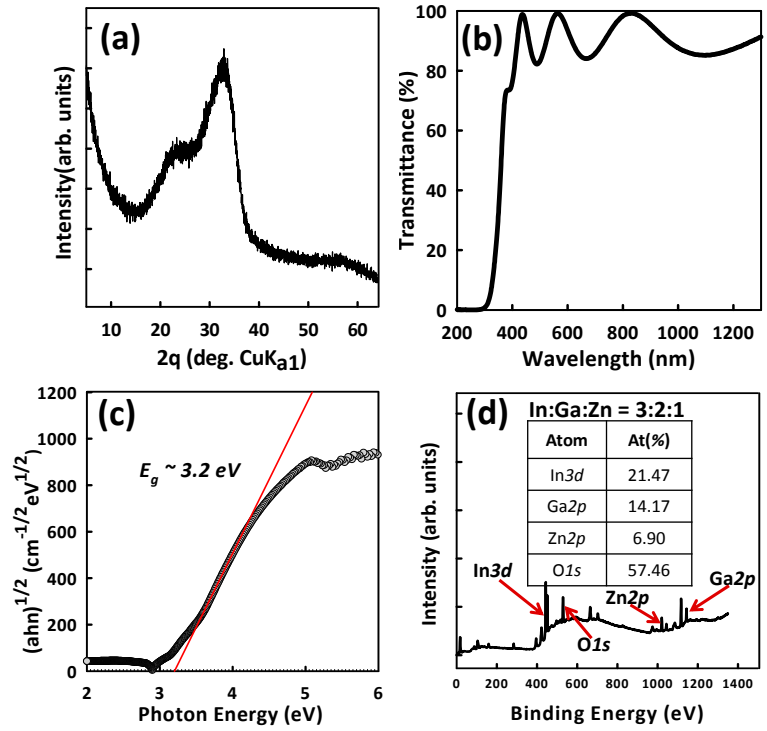

Figure 3. Material properties of amorphous indium-gallium zinc-oxide films. (**a**) X-ray diffraction patterns, (**b**) transmittance, (**c**) Tauc's plot, and (**d**) X-ray photon electron spectroscopy.

3. Results

TFT current-voltage (*I-V*) characteristics exhibit a clear dependency on t_{IGZO} (Figure 4a). Previous reports also show similar effects of t_{IGZO} on TFT parameters [17–20]. The drop in the on-state currents and positive shift of V_{ON} with decreasing t_{IGZO} are consistent with a decrease in carrier concentration [18] or an increase in deep electron traps at the a-IGZO film surface as the t_{IGZO} becomes very small, as previously reported [18,20]. However, it could also be as a result of 20 nm being the thickness in which gate modulation is effective, given that it becomes significant for t_{IGZO} < 20 nm. Similarly, the C-V characteristics shift to the negative V_{GS} direction with increasing t_{IGZO} (Figure 4b). Table 1 lists the TFT parameters as a function of t_{IGZO}.

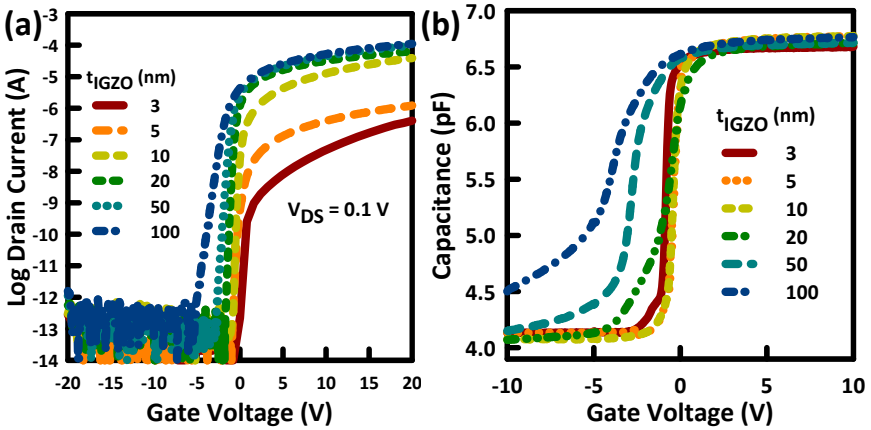

Figure 4. Amorphous indium-gallium zinc-oxide (a-IGZO) thin-film transistor characteristics as a function of a-IGZO thickness (t_{IGZO}), (**a**) current-voltage (*I-V*) and (**b**) capacitance-voltage (*C-V*) characteristics.

For all the t_{IGZO} investigated, the a-IGZO semiconductor should be fully depleted, given that the off-state leakage currents do not significantly change with increasing t_{IGZO} [22]. The negative shift of V_{ON} with increasing t_{IGZO} is interesting, particularly because hydrogenated amorphous silicon (a-Si:H) TFTs do not exhibit such a dependency on semiconductor thickness [22,23]. It is also interesting to note that SS increases with increasing t_{IGZO}, consistent with the stretching out of the C-V characteristics of TFTs with thick a-IGZO layers (Figure 4).

The negative ΔV_{ON} induced by NBIS decreases with decreasing t_{IGZO} (Figure 5a–e). Table 1 also shows TFT parameters extracted after the application of NBIS and Figure 5e shows the time dependency of the ΔV_{ON} for the TFTs. Note that when t_{IGZO} = ~3 nm, the ΔV_{ON} is negligible.

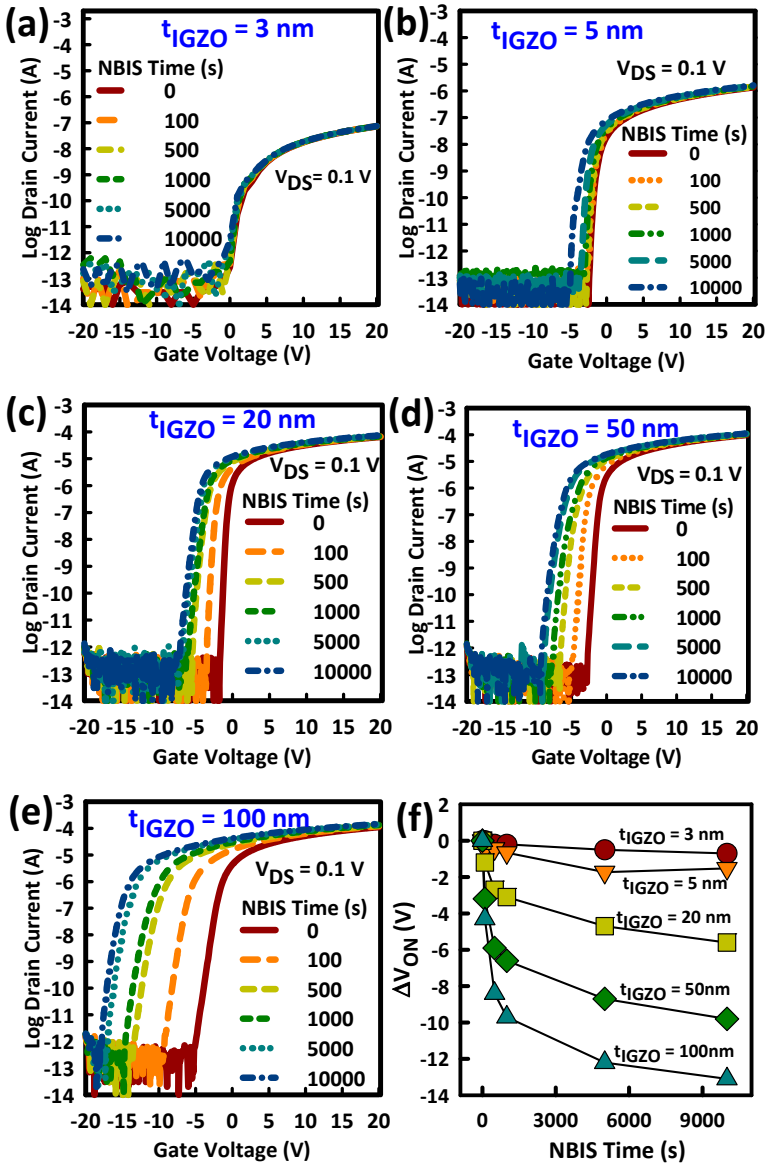

Figure 5. Effect of negative-gate bias stress combined with visible light illumination (NBIS). (**a**–**e**) thin-film transistor (TFT) current-voltage (*I-V*) characteristics before and after NBIS for varying amorphous indium-gallium zinc-oxide thickness (t_{IGZO}). (**f**) Turn-on voltage (V_{ON}) dependence on NBIS Time. Channel width W = 2000 μm and channel length L = 10 μm. The NBIS-induced negative turn-on voltage (V_{ON}) shift increases with increasing t_{IGZO}. NBIS is accomplished by holding the TFT gate voltage at −20 V for 10,000 s, while biasing the source and drain electrodes at zero volts, under white light illumination (9000 nit).

Table 1. Key thin-film transistor parameters.

t_{IGZO} (nm)	V_{ON} (V)		μ_{FE} (cm^2/V·s)		SS (mV/dec)	
	Before NBIS	After NBIS	Before NBIS	After NBIS	Before NBIS	After NBIS
3	0.0	−1.6	1.60	1.68	100	196
5	−1.2	−6.0	17.05	17.43	127	136
20	−2.8	−10.0	18.49	18.88	152	171
50	−4.4	−13.2	19.15	19.47	276	375
100	−4.8	−18.0	20.02	20.19	426	439

NBIS is short for negative-gate bias stress combined with visible light illumination. t_{IGZO}, V_{ON}, μ_{FE}, and SS, are the amorphous indium-gallium zinc-oxide thickness, turn-on voltage, field-effect mobility and subthreshold voltage swing.

4. Discussion

4.1. V_{TH} Dependency on Channel Thickness

Kim et al. noted that the last term in the TFT V_{TH} expression:

$$V_{TH} = (\Phi_M - \Phi_S) \quad + \frac{q \times N_{bulk} \times (E_F - E_i)_{threshold}}{C_{OX}} - \frac{Q_f}{C_{OX}} + \frac{q \times N_{int} \times (E_F - E_i)_{threshold}}{C_{OX}} - \frac{Q_m}{C_{OX}} - \frac{q \times (D_D - D_A)}{C_{OX}} \quad (1)$$

suggests that carrier concentration in the channel layer influences the V_{TH} [24]. In the V_{TH} expression, C_{OX} is the gate-insulator capacitance per unit area, Q_f is the oxide charge density, N_{bulk} and N_{int} are the shallow bulk trap density and the interface trap density, respectively, and Φ_M and Φ_S are, respectively, the metal and semiconductor work functions. D_D and D_A are respectively the donor and acceptor concentrations per unit area. In an n-type oxide semiconductor such as a-IGZO, D_A is negligible and the product of the donor concentration per unit volume (N_D) and the semiconductor thickness obtain D_D. For a-IGZO TFTs with varying t_{IGZO}, V_{TH} thus varies with $q \times N_D \times t_{IGZO}/C_{OX}$, given that all other terms in the V_{TH} expression are independent of the semiconductor thickness. For a 250 nm-thick SiO_2 gate-insulator, Figure 6 shows how V_{TH} varies with t_{IGZO} for N_D ranging from 10^{15}–10^{17} cm^{-3}. As the carrier concertation of the a-IGZO TFTs studied herein lies between 10^{16} and 10^{17} cm^{-3}, simulated results in Figure 6 are consistent with the experimental results in Figure 4a. Kim et al. argued that this phenomenon is generally disregarded in a-Si:H TFTs, given that their carrier concentration is 2–3 orders of magnitude lower than that of the oxide TFTs, making the V_{TH} sensitivity on the channel thickness of a-Si TFTs negligible [24]. This is confirmed in Figure 6, where V_{TH} becomes insensitive to semiconductor thickness when $N_D \leq 10^{15}$ cm^{-3}.

4.2. SS Dependency on Channel Thickness

Total shallow trap densities (N_T) can be estimated from SS values using the relation SS = $\log_e 10 \times k_B T/q \times (1 + q(N_{int} + t_{IGZO} \times N_{bulk})/C_{OX})$, where q is the elementary electric charge, k_B the Boltzmann constant, and T the temperature. N_{int} is the area density of the shallow traps close to the Fermi level (E_F) at the gate-insulator/semiconductor interface and N_{bulk} is the volume density of shallow traps in the bulk of the a-IGZO semiconductor. The sum N_{int} + ($t_{IGZO} \times N_{bulk}$) gives the N_T. By linear regression of $N_T = N_{int} + t_{IGZO} \times N_{bulk}$, N_{int} and N_{bulk} were estimated to be 1.25×10^{11} cm^{-2} eV^{-1} and 1.07×10^{17} cm^{-3}eV^{-1}, respectively (Figure 7).

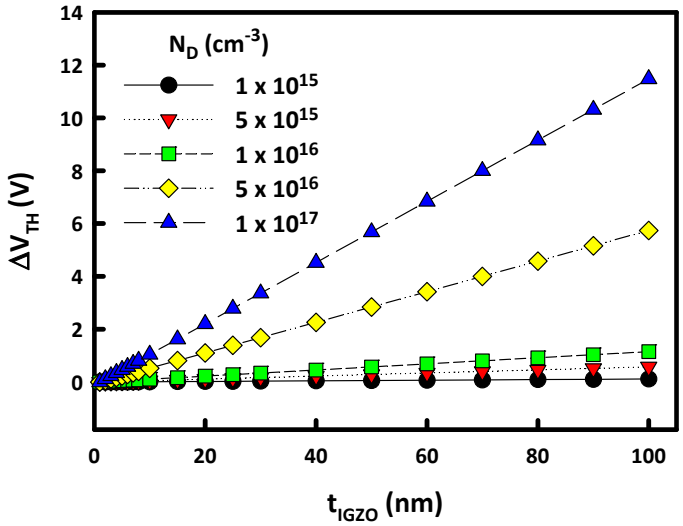

Figure 6. Threshold voltage (V_{TH}) shift (ΔV_{TH}) as a function of amorphous indium-gallium zinc-oxide thickness (t_{IGZO}). V_{TH} = CONST + $q \times N_D \times t_{IGZO}/C_{OX}$, where C_{OX} = 1.38 $\times 10^{-8}$ F/cm^2, $q = 1.6 \times 10^{-19}$ C, and CONST represents the terms independent of t_{IGZO}; $(\Phi_M - \Phi_S) + q \times N_{bulk} \times (E_F - E_i)_{threshold}/C_{OX} - Q_f/C_{OX} + q \times N_{int} \times (E_F - E_i)_{threshold}/C_{OX} - Q_m/C_{OX}$.

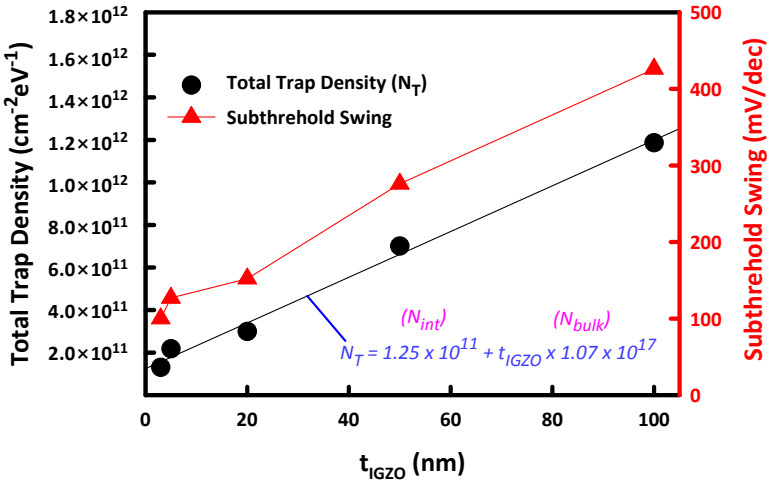

Figure 7. Amorphous indium-gallium zinc-oxide (a-IGZO) semiconductor thickness (t_{IGZO}) dependency of total trap density ($N_T = N_{int} + t_{IGZO} \times N_{bulk}$), where N_{int} is the area density of the shallow traps close to the Fermi level (E_F) at the gate-insulator/semiconductor interface and N_{bulk} is the volume density of shallow traps in the bulk of the a-IGZO semiconductor.

4.3. Effect of Channel Thickness on NBIS Stability

The NBIS instability originates from the presence of gap states near the E_V, which play the role of absorption sites for visible light. Thermal desorption spectra (TDS) obtained by Ide et al. indicated that these defects may include trap states, which originate from the incorporation of the weakly bonded oxygen commonly known as oxygen vacancies [10,22,23]. Upon illumination, a neutral oxygen vacancy (V_O) releases one or two electrons to the conduction band (E_C), forming its ionized states, V_O^+ or V_O^{2+}, which are located in the vicinity of the mobility edge (Figure 8a). The negative V_{GS} applied during NBIS pushes the Fermi level (E_F) toward the E_V, decreasing the ionized vacancies' formation enthalpy, ΔH, which is given by the term $-q(E_F - E_V)$, q being the defect charge state [25]. Creation of additional defects is also possible due to the decrease in ΔH. Note that in an oxygen-deficient material, the shift

of E_F toward E_V may result in a negative ΔH and spontaneous defect formation [25]. The energy distribution of the defects formed after application of NBIS should be very close to E_F because the SS increases after application of NBIS (Figure 5). Existing and created ionized oxygen vacancies can also drift toward the gate insulator interface, contributing to a buildup of a positive charge at the gate-insulator/active-layer interface. Note that trapped/accumulated positive charge may provide a positive bias effect on the n-type a-IGZO channel, consistent with the negative ΔV_{ON} after NBIS.

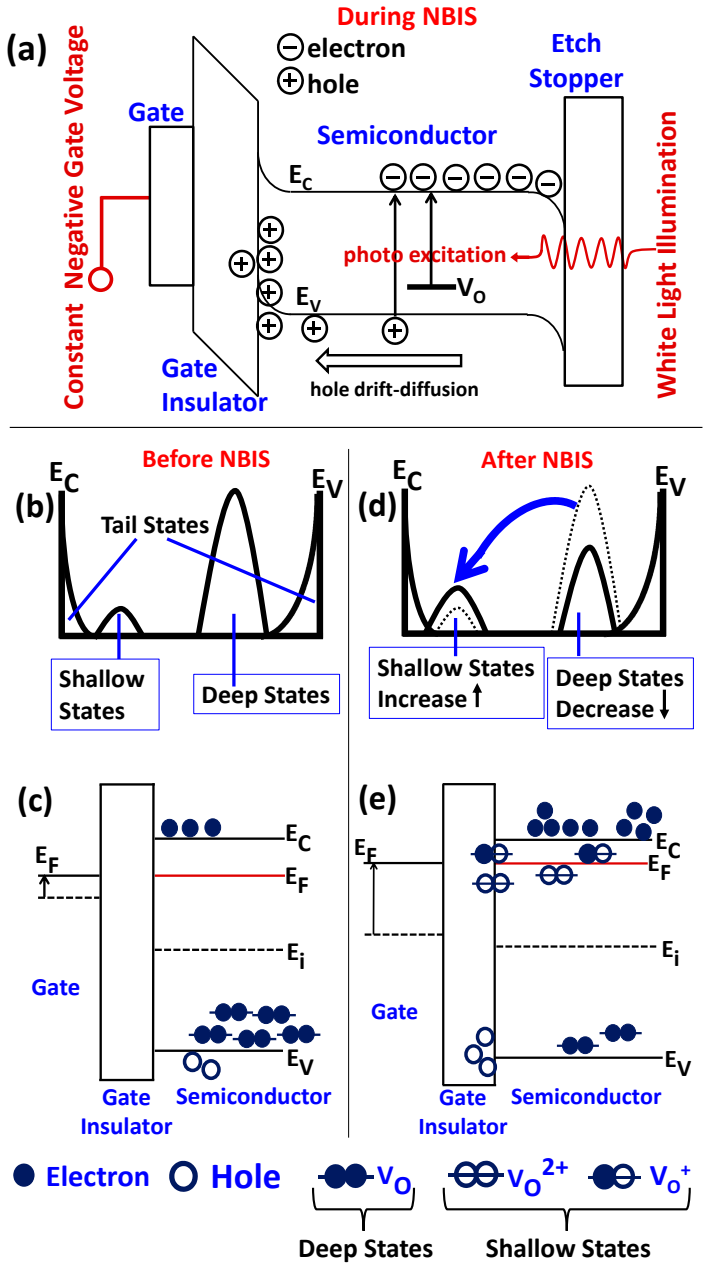

Figure 8. Effect of negative-gate bias stress combined with visible light illumination (NBIS). (**a**–**e**) Thin-film transistor (TFT) current-voltage (*I*-*V*) characteristics before and after NBIS for varying amorphous indium-gallium zinc-oxide thickness (t_{IGZO}). Turn-on voltage (V_{ON}) dependence on NBIS Time. Channel width W = 2000 μm and channel length L = 10 μm. The NBIS-induced negative turn-on voltage (V_{ON}) shift increases with increasing t_{IGZO}. NBIS is accomplished by holding the TFT gate voltage at −20 V for 10,000 s, while biasing the source and drain electrodes at zero volts, under white light illumination (9000 nit).

When the neutral V_O states lose electrons to form the ionized V_O^+ and V_O^{2+}, they undergo outward structural relaxation, suggesting higher energy for V_O^+ and V_O^{2+} compared to the neutral state (V_O). Therefore, shallow states increase, while the deep states decrease, as illustrated in Figure 8b–e. The magnitude of the NBIS-induced negative ΔV_{TH} thus depends on the total number of ionized donors, because events occurring at the semiconductor/gate-insulator interface govern TFT operation. Figure 9 shows the DOS extracted from the combined analysis of *I-V* and *C-V* characteristics before and after application of NBIS. After NBIS, the DOS shows the formation of a broad peak between $E–E_C$ of 0.2 eV and 1.0 eV, which increases in height and width with increasing t_{IGZO}. This peak is consistent with the increase in ionized donors, and as their total number increases with increasing t_{IGZO}, TFTs with the thin a-IGZO layers are, therefore, more stable against NBIS than the TFTs with thicker a-IGZO layers. This dependency of the NBIS stability on t_{IGZO}, thus, indicates that bulk, rather than interfacial defects, are the main source of the NBIS instability in mixed oxide TFTs.

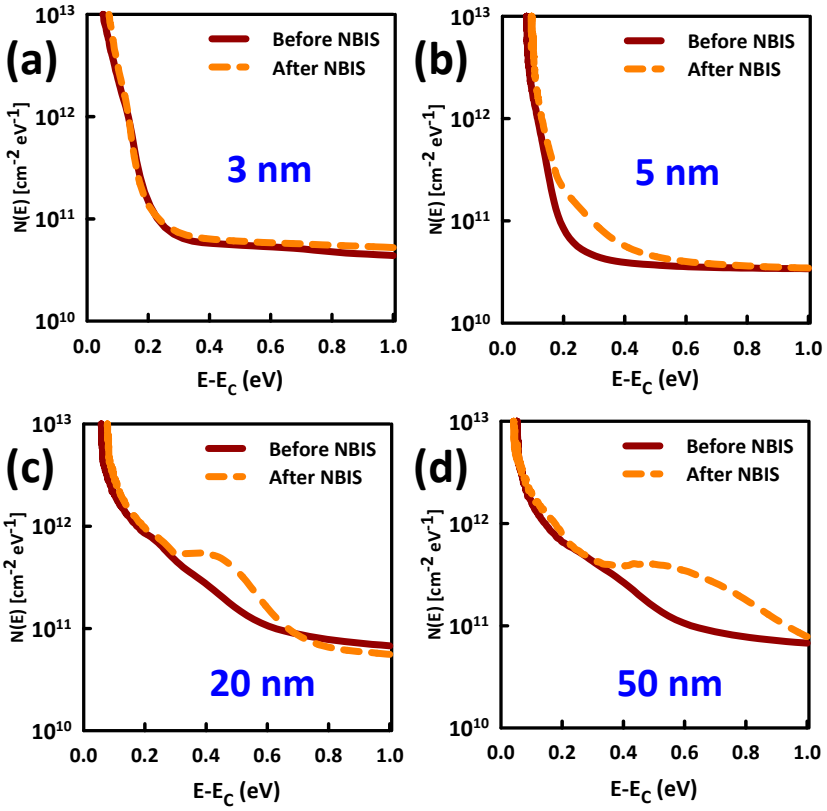

Figure 9. Concentration of donors before and after 10,000 s of negative-gate bias stress combined with visible light illumination (NBIS), (**a**) 3 nm; (**b**) 5 nm; (**c**) 20 nm; (**d**) 50nm.

These results are also consistent with previous reports. For instance, a recent publication by Flewitt et al. revealed a weak localization of carriers in a-IGZO that is over 20 nm [26]. This means that if the number of sites that electrons can migrate to is constrained in the vertical direction, the creation of charged donors should be less likely in TFTs with thinner active layers compared to those with thicker active layers. Li et al. also showed that electron concentration decreases with film thickness in a-IGZO thin films, such that films with t_{IGZO} < ~20 nm exhibited a bandgap expansion with decreasing t_{IGZO} [27]. Li et al. attributed this to a quantum confinement effect in very thin a-IGZO TFTs. Thicker films (t_{IGZO} > ~35 nm) demonstrated the free-electron effect (i.e., the Burstein-Moss shift) and an increase of free-electron absorption with increasing t_{IGZO} (i.e., increasing electron concentration) [27]. For thin layers, the quantum confinement effect is consistent with the large band offsets that the a-IGZO forms with the SiO_2 gate insulator and etch stopper (Figure 10).

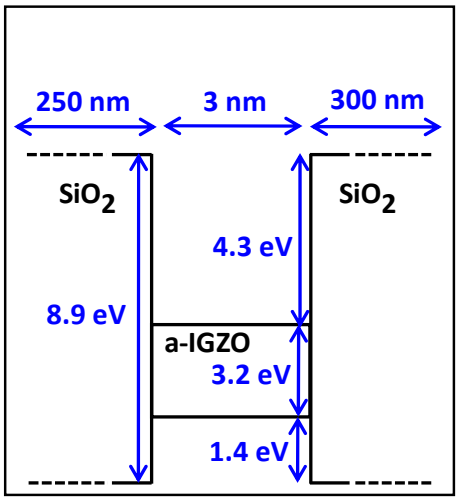

Figure 10. Band offsets between amorphous indium-gallium zinc-oxide (a-IGZO) and SiO_2.

4.4. Verification of the Effect of Oxygen Vacancies on NBIS Stability

To confirm that oxygen vacancies are indeed the cause of the NBIS instability, we investigated the NBIS stability of TFTs with a-IGZO layers that are 20 nm thick but deposited at different oxygen partial pressures (Figure 11). It is interesting to find that NBIS stability increases with an increase the oxygen partial pressure. This confirms that oxygen vacancies are indeed the cause of the NBIS instability in mixed oxide TFTs, given that the concentration of oxygen vacancies and, hence, carrier concentration decreases with the increasing oxygen partial pressure [1,28].

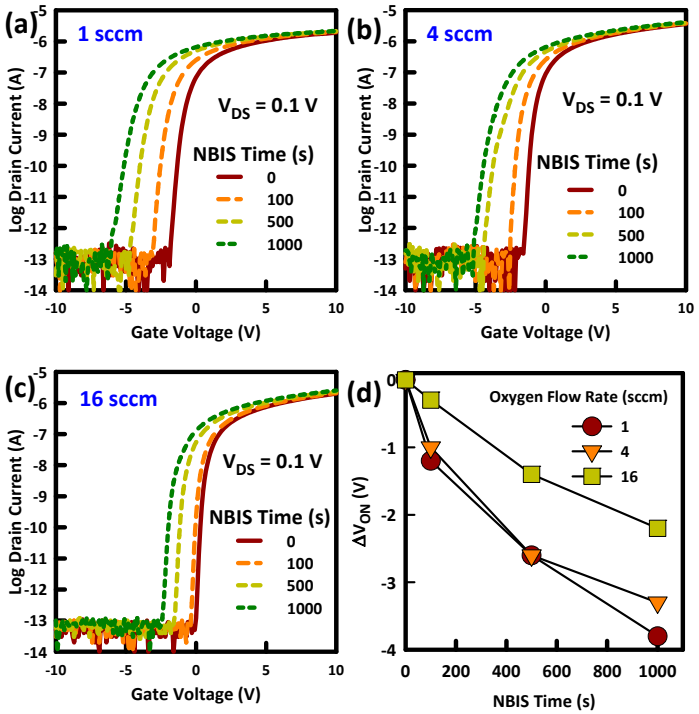

Figure 11. (**a**–**c**) Thin-film transistor (TFT) current-voltage (*I-V*) characteristics before and after negative-gate bias stress combined with visible light illumination (NBIS) for varying oxygen partial pressure during the deposition of the amorphous indium-gallium zinc-oxide layer. (**d**) The corresponding NBIS-induced negative turn-on voltage (V_{ON}) shifts.

Figure 12 presents an additional piece of evidence confirming the role of oxygen vacancies in the NBIS instability of mixed oxide TFTs. Before application of NBIS (Figure 12a), V_{TH} shifted to the negative V_{GS} direction with increasing photon energy, indicating the increase in carrier concentration due to the ionization of V_O to V_O^+ and/or V_O^{2+} [29–31].

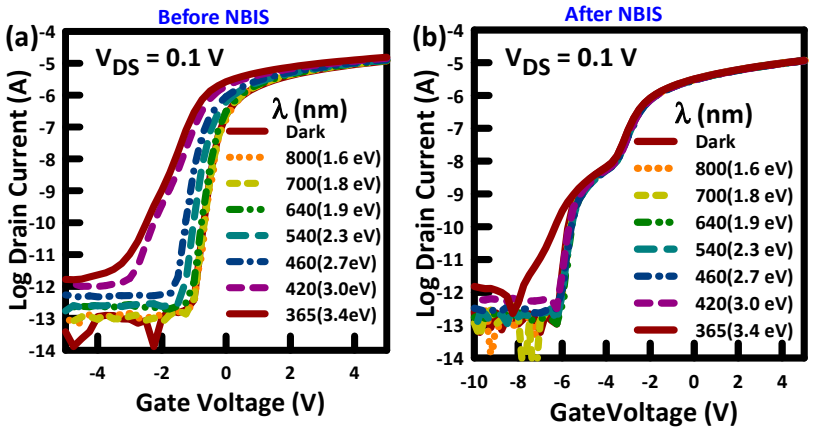

Figure 12. Effect of monochromatic light on the performance of amorphous indium-gallium zinc-oxide (a-IGZO) thin-film transistors (TFTs) (**a**) before and (**b**) after application of negative-gate bias stress combined with visible light illumination (NBIS).

Given that the band gap (E_g) of a-IGZO is ~3.1 eV, these results clearly indicate sub-gap photoexcitation, consistent with the ionization of V_O to V_O^+ and/or V_O^{2+}. However, after application of NBIS, light with a wavelength less than E_g of a-IGZO results in negligible change in the performance of the a-IGZO TFTs (Figure 12b). These results show that NBIS does indeed result in the ionization of V_O to V_O^+ and/or V_O^{2+}, such that further ionization by light illumination results in no significant sub-gap photoexcitation after NBIS. Only light with a wavelength greater than E_g causes a significant change due to band-to-band excitation. The stretching-out of the subthreshold characteristics of the TFT after NBIS is consistent with back channel conduction that randomly occurs after application of NBIS.

4.5. Fabrication Process Optimization

The variations in performance and theories from research group to research group are closely related to the sensitivity of mixed oxide semiconductors to air or chemicals. Exposure to air should be avoided, not only after device fabrication (Figure 1f), but also, more importantly, during the fabrication process itself (Figure 1b). If a device is fabricated with neither an etch stopper nor a passivation layer, the device stability will improve with increasing a-IGZO thickness. Thick a-IGZO layers will have a self-passivation effect by the intrinsic a-IGZO, even though the surface region is affected by moisture or oxygen from ambient air; that is, the thicker the a-IGZO layer, the farther away the front channel accumulation layer (bottom surface of the semiconductor layer) is from the desorption and adsorption properties occurring at the top surface. More importantly, if the vacuum is broken between the deposition of the a-IGZO and the etch stopper, in cases where the two processes have to be performed in two different chambers, significant contamination to the a-IGZO layer will occur during the transfer from the a-IGZO deposition chamber to the etch-stopper deposition chamber. This is very important, but often overlooked. In the case of the devices presented herein, a cluster deposition tool that allows consecutive deposition of the gate insulator, active layer, and etch stopper without breaking vacuum is used, thereby passivating the a-IGZO layer throughout the whole fabrication process. Therefore, we emphasize that due to fabrication process optimization, intrinsic, rather than process-related instability mechanisms, were detectable in this study.

Device structure and the type of dielectrics used can also be a source of the differences in the trends observed with varying semiconductor thickness. For instance, the stability of inverted, staggered devices without a passivation layer is more likely to improve with increasing semiconductor thickness because the thicker the semiconductor, the further away the front channel (bottom surface of the semiconductor layer) is from the absorption/desorption processes occurring at the top surface [8]. In this report, the root cause of these conflicting theories is not only attributed to the possibility of varying the types and/or ratios of the components making up a mixed oxide semiconductor, but it is mainly attributed to fabrication process variations, given the sensitivity of mixed oxide semiconductors to wet etchants, gasses, or air exposure. Therefore, we show here that under an optimized fabrication process, which involves the passivation of the mixed oxide semiconductor in situ, employing very thin mixed oxide semiconductors completely suppresses the NBIS-induced instability. It is, thus, reasonable to conclude that under the optimized fabrication process presented herein, bulk, rather than interfacial defects, are the main source of bias and light instability in mixed oxide TFTs.

It is important to note that the self-passivation effect of thick semiconductor layers is not useful in real applications, such as display panels, where TFTs are passivated/encapsulated by materials with very low water-vapor-transmission-rates. As good NBIS stability is of utmost importance, TFTs with thin semiconductor layers are thus more desirable. However, in TFTs with thin active layers, there is an NBIS stability versus on-state current trade-off. This can be minimized by the employment of large channel widths, if the intended application allows. Although a-IGZO TFTs are used as test devices, the conclusions made herein can also be extended to other varieties of mixed oxides or other forms of instabilities—particularly to explain the non-reproducible nature of the performance of these mixed oxide TFTs, and why, from one group to another, there is so much variation in results and theories.

Acknowledgments: This work was supported in part by the National Research Foundation of Korea (NRF) grant funded by the Korea government (MSIP) (NRF2016R1C1B1015765).

Author Contributions: Jae Gwang Um performed the experiments; Mallory Mativenga analyzed the data and wrote the paper; Jin Jang discussed the results and supervised the work.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Kamiya, T.; Hosono, H. Material characteristics and applications of transparent amorphous oxide semiconductors. *NPG Asia Mater.* **2010**, *2*, 15–22. [CrossRef]
2. Jeong, J.K. The status and perspectives of metal oxide thin-film transistors for active matrix flexible displays. *Semicond. Sci. Technol.* **2011**, *26*, 034008. [CrossRef]
3. Den Boer, W. *Active Matrix Liquid Crystal Displays*; Elsevier: London, UK, 2005.
4. Chang, Y.-G.; Moon, W.; Kim, H.; Lee, S.; Kim, H.; Park, K.; Kim, C.-D.; Im, S. DC versus pulse-type negative bias stress effects on the instability of amorphous InGaZnO transistors under light illumination. *IEEE Electron Device Lett.* **2011**, *32*, 1704–1706. [CrossRef]
5. Chen, W.-T.; Hsueh, H.-W.; Zanz, H.-W.; Tsai, C.-C. Light-enhanced bias stress effect on amorphous In-Ga-Zn-O thin-film transistor with lights of varying colors. *Electrochem. Solid-State Lett.* **2011**, *14*, H297–H299. [CrossRef]
6. Chowdhury, H.; Migliorato, P.; Jang, J. Light induced instabilities in amorphous indium–gallium–zinc–oxide thin-film transistors. *Appl. Phys. Lett.* **2010**, *97*, 173506-1–173506-3. [CrossRef]
7. Oh, H.; Yoon, S.M.; Ryu, M.K.; Hwang, C.S.; Yang, S.; Park, S.H. Photon-accelerated negative bias instability involving subgap states creation in amorphous In–Ga–Zn–O thin film transistor. *Appl. Phys. Lett.* **2010**, *97*, 183502-1–183502-3. [CrossRef]
8. Nomura, K.; Kamiya, T.; Hosono, H. Interface and bulk effects for bias–light-illumination instability in amorphous-In–Ga–Zn–O thin-film transistors. *J. Soc. Inf. Disp.* **2010**, *18*, 789–795. [CrossRef]

9. Ji, K.H.; Kim, J.I.; Jung, H.Y.; Park, S.Y.; Choi, R.; Kim, U.K.; Hwang, C.S.; Lee, D.; Hwang, H.; Jeong, J.K. Effect of high-pressure oxygen annealing on negative bias illumination stress-induced instability of InGaZnO thin film transistors. *Appl. Phys. Lett.* **2011**, *98*, 103509-1–103509-3. [CrossRef]
10. Ide, K.; Kikuchi, Y.; Nomura, K.; Kimura, M.; Kamiya, T.; Hosono, H. Effects of excess oxygen on operation characteristics of amorphous In-Ga-Zn-O thin film transistors. *Appl. Phys. Lett.* **2011**, *99*, 093507-1–093507-3. [CrossRef]
11. Liu, P.-T.; Chou, Y.-T.; Teng, L.-F.; Li, F.-H.; Fuh, C.-S.; Shieh, H.-P. Ambient stability enhancement of thin-film transistor with InGaZnO capped with InGaZnO:N bilayer stack channel Layers. *IEEE Electron Device Lett.* **2011**, *32*, 1397–1399. [CrossRef]
12. Ji, K.H.; Kim, J.I.; Mo, Y.G.; Jeong, J.H.; Yang, S.; Hwang, C.S.; Park, S.-H.K.; Ryu, M.-K.; Lee, S.-Y.; Jeang, J.K. Comparative study on light-induced bias stress instability of IGZO transistors with SiN_x and SiO_2 gate dielectrics. *IEEE Electron Device Lett.* **2011**, *31*, 1404–1406. [CrossRef]
13. Nomura, K.; Kamiya, T.; Hosono, H. Highly stable amorphous In-Ga-Zn-O thin-film transistors produced by eliminating deep subgap defects. *Appl. Phys. Lett.* **2011**, *99*, 053505-1–053505-3. [CrossRef]
14. Lee, S.; Mativenga, M.; Jang, J. Removal of negative-bias-illumination-stress instability in amorphous-InGaZnO thin-film transistors by top-gate offset structure. *IEEE Electron Device Lett.* **2014**, *35*, 930–932. [CrossRef]
15. Jin, S.; Mativenga, M.; Jang, J. Reduction of positive-bias-stress effects in bulk-accumulation amorphous-InGaZnO TFTs. *IEEE Electron Device Lett.* **2014**, *35*, 560–562. [CrossRef]
16. Kong, D.; Jung, H.-K.; Kim, Y.; Bae, M.; Jeon, W.W.; Kim, S.; Kim, D.M.; Kim, D.K. The effect of the active layer thickness on the negative bias stress-induced instability in amorphous InGaZnO thin-film transistors. *IEEE Electron Device Lett.* **2011**, *32*, 1388–1390. [CrossRef]
17. Lee, S.Y.; Kim, D.H.; Chong, E.; Jeon, Y.W.; Kim, D.H. Effect of channel thickness on density of states in amorphous InGaZnO thin film transistors. *Appl. Phys. Lett.* **2011**, *98*, 122105-1–122105-3. [CrossRef]
18. Cho, E.N.; Kang, J.H.; Yun, I. Effects of channel thickness variation on bias stress instability of InGaZnO thin-film transistors. *Microelectron. Reliab.* **2011**, *51*, 1792–1795. [CrossRef]
19. Barquinhaz, P.; Pereira, L.; Gonçalves, G.; Martins, R.; Fortunato, E. Toward high-performance amorphous GIZO TFTs. *J. Electrochem. Soc.* **2008**, *156*, H161–H168. [CrossRef]
20. Shao, L.; Nomura, K.; Kamiya, T.; Hosono, H. Operation characteristics of thin-film transistors using very thin amorphous In-Ga-Zn-O channels. *Electrochem. Solid State Lett.* **2011**, *14*, H197–H200. [CrossRef]
21. Migliorato, P.; Seok, M.J.; Jang, J. Determination of flat band voltage in thin film transistors: The case of amorphous-indium gallium zinc oxide. *Appl. Phys. Lett.* **2012**, *100*, 073506-1–073506-3. [CrossRef]
22. Chiang, H.Q.; McFarlane, B.R.; Hong, D.; Presley, R.E.; Wager, J.F. Processing effects on the stability of amorphous indium gallium zinc oxide thin-film transistors. *J. Non-Cryst. Solids* **2008**, *354*, 2826–2830. [CrossRef]
23. Park, J.-S.; Jeong, J.K.; Mo, Y.-G.; Kim, H.D.; Kim, C.-J. Control of threshold voltage in ZnO-based oxide thin film transistors. *Appl. Phys. Lett.* **2008**, *93*, 033513-1–033513-3. [CrossRef]
24. Barquinha, P.; Pimentel, A.; Marques, A.; Pereira, L.; Martins, R.; Fortunato, E. Influence of the semiconductor thickness on the electrical properties of transparent TFTs based on indium zinc oxide. *J. Non-Cryst. Solids.* **2006**, *352*, 1749–1752. [CrossRef]
25. Kim, S.-J.; Lee, S.-Y.; Lee, Y.-W.; Lee, W.-G.; Yoon, K.-S.; Kwon, J.-Y.; Han, M.-K. Effect of Channel Layer Thickness on Characteristics and Stability of Amorphous Hafnium–Indium–Zinc Oxide Thin Film Transistors. *Jpn. J. Appl. Phys.* **2011**, *50*. [CrossRef]
26. Clark, S.J.; Robertson, J.; Lany, S.; Zunger, A. Intrinsic defects in ZnO calculated by screened exchange and hybrid density functionals. *Phys. Rev. B* **2010**, *81*, 115311-1–115311-5. [CrossRef]
27. Flewitt, A.J.; Powell, M.J. A thermalization energy analysis of the threshold voltage shift in amorphous indium gallium zinc oxide thin film transistors under simultaneous negative gate bias and illumination. *J. Appl. Phys.* **2014**, *115*. [CrossRef]
28. Li, X.D.; Chen, T.P.; Liu, P.; Liu, Y.; Liu, Z.; Leong, K.C. A study on the evolution of dielectric function of ZnO thin films with decreasing film thickness. *J. Appl. Phys.* **2014**, *115*, 103512-1–103512-5. [CrossRef]
29. Lee, K.-H.; Ok, K.-C.; Kim, H.; Park, J.-S. The influence of oxygen partial pressure on the performance and stability of Ge-doped InGaO thin film transistors. *Ceram. Int.* **2014**, *40*, 3215–3220. [CrossRef]

30. Funga, T.-C.; Chuangc, C.-S.; Nomura, K.; Shiehc, H.-P.D.; Hosono, H.; Kanicki, J. Photofield-Effect in Amorphous In-Ga-Zn-O (a-IGZO) Thin-Film Transistors. *J. Inf. Disp.* **2008**, *9*, 21–29. [CrossRef]
31. Lee, K.W.; Shin, H.S.; Hoe, K.Y.; Kim, K.M.; Kim, H.J. Light Effects of the Amorphous Indium Gallium Zinc Oxide Thin-Film Transistor. *J. Inf. Disp.* **2009**, *10*, 171–174. [CrossRef]