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Universal Voltage Conveyor and its Novel Dual-Output Fully-Cascadable VM APF Application

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Abstract: This letter presents a novel realization of a voltage-mode (VM) first-order all-pass filter (APF) with attractive features. The proposed circuit employs a single readily available six-terminal active device called as universal voltage conveyor (UVC) and only grounded passive components, which predict its easy monolithic integration with desired circuit simplicity. The auxiliary voltage input (W) and output (ZP, ZN) terminals of the device fully ensure easy cascadability of VM APF, since the input and output terminal impedances are theoretically infinitely high and zero, respectively. Moreover, thanks to mutually inverse outputs of the UVC, the proposed filter simultaneously provides both inverting and non-inverting outputs from the same configuration. All of these features make the UVC a unique active device currently available in the literature. The behavior of the filter was experimentally measured using the readily available UVC-N1C 0520 chip, which was produced in cooperation with ON Semiconductor Czech Republic, Ltd.

Keywords: active circuit; all-pass filter; dual-output; fully-cascadable filter; universal voltage conveyor; UVC-N1C 0520; voltage-mode

1. Introduction

All-pass filters (APFs) are widely used in signal processing to correct the phase shifts caused by analog filtering operations without changing the amplitude of the applied signal. Moreover, they are with advantage used for the design of high-Q frequency-selective circuits or quadrature/multiphase oscillators [1–4]. In the open literature, a large number of voltage-mode (VM) APFs using various active building blocks (ABBs) exist; however, most of them are single-output realizations (i.e., provide only inverting or non-inverting phase response at voltage-mode output). Note that we do not rule out the importance of such circuits; however, in this study we solely focus on VM APFs that provide both inverting and non-inverting voltage-mode outputs simultaneously [5–14]. In general, the desired features of VM APFs are:

(i) Provide both inverting and non-inverting voltage-mode outputs simultaneously from the same configuration [5–14],
(ii) High-impedance character of voltage input terminal and low output impedance at both voltage-mode outputs, which is needed for easy cascading [12], Figure 2b in [13], [14],
(iii) All passive components are grounded, which is advantageous for monolithic integration [9],
(iv) No complex passive and/or active matching constraints are required [5–11,13,14],
(v) Use of single ABB in order to avoid increasing the circuit complexity [7–10,12–14].

Table 1 summarizes the advantages and disadvantages of previously reported VM APFs which satisfy feature (i), and it provides their fair performance comparison. Among these filtering topologies, the [5,6] are based on a fully-differential operational amplifier (FD-OPA) and second-generation current

conveyor (CCII). Utilization of a positive-type inverting second-generation current conveyor (ICCII+) for VM APF design is demonstrated in [7]. The literature offers various types and generations of CCs, such as fully differential second-generation current conveyor (FDCCII) or differential voltage dual-X second-generation current conveyor (DV-DXCCII) and their dual-output VM APF realizations [8,9]. One of the most recently published VM APFs with attractive performance based on a voltage differencing inverting buffered amplifier (VDIBA) was reported in [10]. The VDIBA is a recently introduced four-terminal active device with an input/output stage that is easily implemented by a differential-input single-output operational transconductance amplifier (OTA) and a unity-gain inverting voltage buffer (IVB), respectively. As it is known, the OTA converts the input voltage to output current while its intrinsic transconductance can easily be tuned via external bias voltage or current. This favorable feature was advantageously used for pole frequency tuning of VM APF in [11]. In the filter topology, except for a single OTA, an additional ABB called a universal voltage conveyor (UVC) is employed. In general, the concept of voltage conveyors (VC) was defined based on the duality principle to current conveyors in 1981 [15]. Since then, different generations (first, second, third) and types (non-inverting, inverting, positive, negative) of voltage conveyors have been introduced in the open literature. Among the special types of VCs is the plus -type differential current voltage conveyor (DCVC+) [16], the concept of which is equivalent to the current differencing buffered amplifier (CDBA) [17,18]. All of the VCs listed above can be realized using a single UVC by suitable interconnection or grounding of its ports [19–22]. Hence, the UVC is a "universal" active element which has one voltage input X, two difference current inputs (YP, YN), two mutually inverse voltage outputs (ZP, ZN), and one auxiliary terminal W, which determine the generation of the voltage conveyor. Moreover, the UVC is a readily available chip which was produced in cooperation with ON Semiconductor Czech Republic, Ltd. under designation UVC-N1C 0520 [22–24]. Since the first UVC-based VM APF was published [11], four more dual-output VM APFs have been introduced into the literature [12–14]. Here it is worth noting that none of these UVC-based APFs simultaneously satisfy the desired features (i)–(v) listed above. Therefore, this letter aims to report a dual-output VM APF with high input and low output impedance characters employing only single UVC and all grounded passive components and with no complex passive matching constraints, which enables a reduction of the circuit complexity. The behavior of the proposed circuit has been experimentally measured using the readily available UVC-N1C 0520.

Table 1. Comparative study of existing dual-output voltage-mode (VM) all-pass filters (APFs).

Reference	ABB Type	Grounded R/C	Floating R/C	Simul./ Meas.	f_p (Hz)	Supply (V)
Figure 4b in [5]	FD-OPA & CCII	0/0	1/1	Meas.	29.6 k	±5
Figure 1 in [6]	FD-OPA	0/0	0/1	Simul.	92 k	±1.5
Figure 2 in [7]	ICCII+	0/0	1/1	Simul.	1.59 M	±1.25
Figure 2 in [8]	FDCCII	0/1	1/0	Simul.	159.2 k	±3
Figure 2 in [9]	DV-DXCCII & 1 NMOS	0/1	0/0	Simul.	27 M	±0.9
Figure 3 in [10]	VDIBA	0/0	0/1	Both	S: 9.44 M; M: 1 M	±0.9; ±5
Figure 1 in [11]	UVC & OTA	0/0	0/1	Simul.	3 M	±2
Figure 3 in [12]	UVC	2/0	1.I	Both	S: 3.5 M; M: 160.4 k	±2.5; ±1.65
Figure 2a in [13]	UVC	2/0	0/1	Simul.	1.17 M	±2.5
Figure 2b in [13]	UVC	2/0	0/1	Both	S: 1.17 M; M: 746.4 k	±2.5; ±1.65
Figure 2 in [14]	UVC	0/1	2/0	Simul.	390 k	±2.5
This work	UVC	2/2	0/0	Meas.	277.8 k	±1.65

Note: S.: simulation result; M.: measurement result. CCII: second-generation current conveyor; DV-DXCCII: differential voltage dual-X second-generation current conveyor; FD-OPA: fully-differential operational amplifier; FDCCII: fully differential second-generation current conveyor; ICCII+: positive-type inverting second-generation current conveyor; OTA: operational transconductance amplifier; UVC: universal voltage conveyor; VDIBA: voltage differencing inverting buffered amplifier; NMOS: n-type metal-oxide-semiconductor.

2. Circuit Description

The circuit symbol of the UVC is shown in Figure 1a. Using standard notation, relations between its individual terminals can be described by the following hybrid matrix:

$$\begin{bmatrix} i_X \\ v_{YP} \\ v_{YN} \\ i_W \\ v_{ZP} \\ v_{ZN} \end{bmatrix} = \begin{bmatrix} Y_X & \alpha_1(s) & -\alpha_2(s) & 0 & 0 & 0 \\ 0 & Z_{YP} & 0 & \delta_1(s) & 0 & 0 \\ 0 & 0 & Z_{YN} & \delta_2(s) & 0 & 0 \\ 0 & 0 & 0 & Y_W & 0 & 0 \\ \gamma_1(s) & 0 & 0 & 0 & Z_{ZP} & 0 \\ -\gamma_2(s) & 0 & 0 & 0 & 0 & Z_{ZN} \end{bmatrix} \cdot \begin{bmatrix} v_X \\ i_{YP} \\ i_{YN} \\ v_W \\ i_{ZP} \\ i_{ZN} \end{bmatrix}, \quad (1)$$

where $Y_X = sC_X + 1/R_X$, $Y_W = sC_W + 1/R_W$ are parasitic admittances and $Z_k = R_k$ (k =YP, YN, ZP, ZN) are the parasitic resistances at relevant terminals of the UVC, respectively, discussed in detail for the readily available UVC-N1C 0520 chip in [22–24]. Parameters $\alpha_j(s)$, $\delta_j(s)$, and $\gamma_j(s)$ are, respectively, frequency-dependent non-ideal current and voltage gains for $j = \{1,2\}$. Ideally, these parameters are equal to unity. Using a single-pole model, they can be defined as:

$$\alpha_j(s) = \frac{\alpha_{oj}}{1+\tau_{\alpha_j}s}, \quad \delta_j(s) = \frac{\delta_{oj}}{1+\tau_{\delta_j}s}, \quad \gamma_j(s) = \frac{\gamma_{oj}}{1+\tau_{\gamma_j}s}. \quad (2)$$

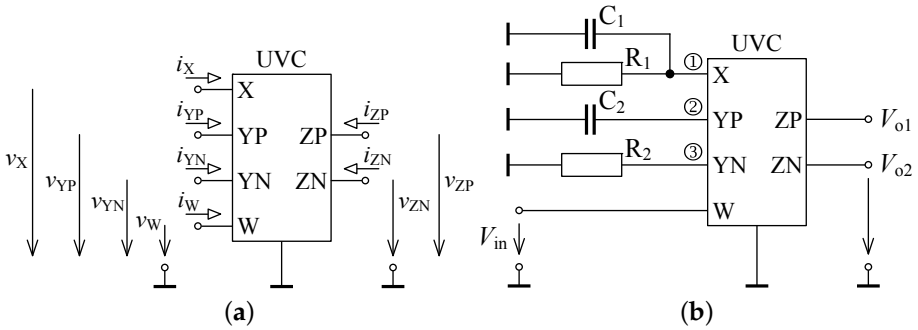

Figure 1. (**a**) Circuit symbol of UVC; (**b**) proposed new voltage-mode first-order all-pass filter.

Here, α_{oj} is DC current, and δ_{oj} and γ_{oj} are DC voltage gains of the UVC, respectively. The bandwidths $1/\tau_{\alpha_j}$, $1/\tau_{\delta_j}$, and $1/\tau_{\gamma_j}$ depend on the fabrication of active devices, and in current technologies on the order of a few gigarad/s are ideally equal to infinity. Hence, at low and medium frequencies—i.e., $f \ll (1/(2\pi)) \times \min\{1/\tau_{\alpha_j}, 1/\tau_{\delta_j}, 1/\tau_{\gamma_j}\}$—Equation (2) becomes:

$$\alpha_j(s) \cong \alpha_{oj} = 1 + \varepsilon_{\alpha_{ij}}, \quad \delta_j(s) \cong \delta_{oj} = 1 + \varepsilon_{\delta_{v1j}}, \quad \gamma_j(s) \cong \gamma_{oj} = 1 + \varepsilon_{\gamma_{v2j}}, \quad (3)$$

whereas $\varepsilon_{\alpha_{ij}}$, $\varepsilon_{\delta_{v1j}}$, and $\varepsilon_{\gamma_{v2j}}$ are current and voltage tracking errors, respectively, and satisfy the inequalities $|\varepsilon_{\alpha_{ij}}| \ll 1$, $|\varepsilon_{\delta_{v1j}}| \ll 1$, and $|\varepsilon_{\gamma_{v2j}}| \ll 1$.

Considering an ideal UVC and assuming $R_1 = R_2 = R$ and $C_1 = C_2 = C$ for the proposed dual-output first-order VM APF shown in Figure 1b, routine analysis yields ideal voltage transfer functions (TFs) in the following forms:

$$T_1(s) = \frac{V_{o1}}{V_{in}} = \frac{sCR-1}{sCR+1}, \quad T_2(s) = \frac{V_{o2}}{V_{in}} = -\frac{sCR-1}{sCR+1}, \quad (4)$$

while the phase responses of the TFs (4) are calculated as:

$$\varphi_1(\omega) = 180^\circ - 2\text{arctg}(\omega CR), \quad \varphi_2(\omega) = -2\text{arctg}(\omega CR), \quad (5)$$

which indicates that the proposed VM APF can simultaneously provide phase shifting between π (at $\omega = 0$) to 0 (at $\omega = \infty$) and 0 (at $\omega = 0$) to $-\pi$ (at $\omega = \infty$) at output terminals V_{o1} and V_{o2}, respectively. Finally, both the zero and pole frequencies are equal, and can be found as $\omega_z = \omega_p = 1/(CR)$. Therefore, their sensitivities to passive elements are $S_{C,R}^{\omega_{z,p}} = -1$; i.e., are not higher than unity in magnitude.

3. Non-Ideal Analysis

For a complete analysis of the circuit, it is also important consider the main non-idealities of the UVC in Equation (1) as also shown in Figure 2, where:

- the parasitic resistance R_X and parasitic capacitance C_X appear between the high-impedance terminal X of the UVC and ground and their values computed in SPICE software are $R_X = 378.73\ \text{k}\Omega \parallel C_X = 17.41\ \text{pF}$, respectively,
- the non-zero parasitic resistance R_{YP} and R_{YN} at two difference current inputs YP and YN have values $R_{YP} = 1.27\ \Omega$ and $R_{YN} = 0.51\ \Omega$, respectively,
- the parasitic resistance R_W and parasitic capacitance C_W appear between the auxiliary terminal W of the UVC and ground and their values are $R_W = 88.19\ \text{M}\Omega \parallel C_W = 4.19\ \text{pF}$, respectively,
- the non-zero parasitic resistance R_{ZP} and R_{ZN} at mutually inverse voltage outputs ZP and ZN have values $R_{ZP} = 1.01\ \Omega$ and $R_{ZN} = 0.71\ \Omega$, respectively.

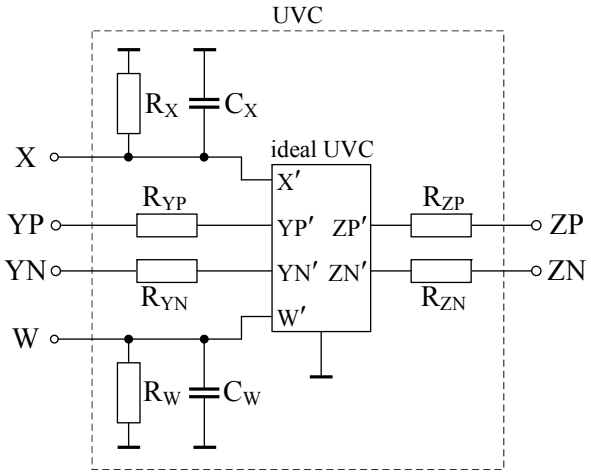

Figure 2. Main parasitic resistance and capacitance of the UVC.

These parameters can be found in greater detail in [22–24]. Now, considering the non-idealities listed above, the proposed VM APF suffers from the following non-idealities:

- at the node ①, a parasitic impedance $Z_X = 1/Y_X = R_X \parallel (1/sC_X)$ can be seen. Note that the capacitance C_X and resistance R_X can be absorbed into external capacitor C_1 and resistor R_1, respectively, as they appear in parallel. Hence, in further analysis the total capacitance and resistance at this node will be considered C_1' and $R_1' = Z_1'$,
- the node ② at low-impedance terminal YP is characterized by a parasitic impedance $Z_{YP} = R_{YP}$, which is in series with external capacitor C_2, and by assuming it as an impedance $Z_{C_2} = 1/Y_{C_2} = 1/sC_2$, the total impedance at this node can be described as Z_{C_2}',
- finally, the node ③ can be characterized by a parasitic impedance $Z_{YN} = R_{YN}$, which appears in series with external resistor $R_2 = Z_2$. Hence, the total impedance at this node can be labeled as Z_2'.

Considering the non-ideal current and voltage gains of the UVC and simultaneously the effect of the aforementioned non-idealities and re-analyzing the proposed VM APF, the ideal TFs (4) convert to:

$$T_1'(s) = \frac{\gamma_{o1} Z_1' \left(\alpha_{o1}\delta_{o1} Z_2' - \alpha_{o2}\delta_{o2} Z_{C_2}'\right)}{Z_2' Z_{C_2}' \left(sC_1' Z_1' + 1\right)}, \qquad T_2'(s) = -\frac{\gamma_{o2}}{\gamma_{o1}} \cdot T_1'(s). \tag{6}$$

Subsequently, the non-ideal zero and pole frequencies differ and can be found as:

$$\omega_z = \frac{\alpha_{o2}\delta_{o2}}{\alpha_{o1}\delta_{o1}} \cdot \frac{Z_{C_2}'}{Z_2'}, \qquad \omega_p = \frac{1}{C_1' Z_1'}. \tag{7}$$

The effect of non-idealities on the proposed VM APF can be significantly minimized by the proper selection of external passive components and/or by precise design of the UVC.

4. Experimental Verification

In order to confirm the theory and prove the real behavior of the proposed VM APF using the readily available UVC-N1C 0520 [22–24] chip, a printed circuit board (PCB) was developed, shown in Figure 3. The experimental measurement results were carried out using an Agilent 4395A Network/Spectrum/Impedance Analyzer (Agilent Technologies: Penang, Malaysia). In all measurements, the passive component values of the filter were selected as $C_1 = C_2 = 560$ pF and $R_1 = R_2 = 1$ kΩ, which ensures a 90° phase shift at $f_{p\_teor} \cong 284.2$ kHz. Figure 4a,b illustrate measured gain and phase responses for both inverting and non-inverting outputs, respectively, from which it can be observed that the obtained pole frequency has a value $f_{p\_meas} \cong 277.8$ kHz and there is an attenuation of about 2.55 dB ±6%. Output noise behavior for both responses with respect to frequency are shown in Figure 5. As it can be seen, the noise behavior of both responses are likely the same. For instance, the output noise for V_{o2} response at the operating pole frequency was found as 1.5089 $\mu V/\sqrt{Hz}$. Measured time-domain responses are depicted in Figure 6, in which a sine-wave input signal of 200 mV_{pp} and frequency of 275 kHz was applied to the filter. Subsequently, the Fourier spectrum of both output signals, showing a high selectivity for the applied signal frequency, is shown in Figure 7a,b, respectively. The total harmonic distortions (THDs) at pole frequency were found as 2.078% and 2.080% for the outputs V_{o1} and V_{o2} of the proposed filter, respectively. Note that the minor deviations are caused by real behavior of the UVC-N1C 0520 chip and extra parasitic capacitances of the fabricated PCB. The real behavior of the filter is very satisfactory.

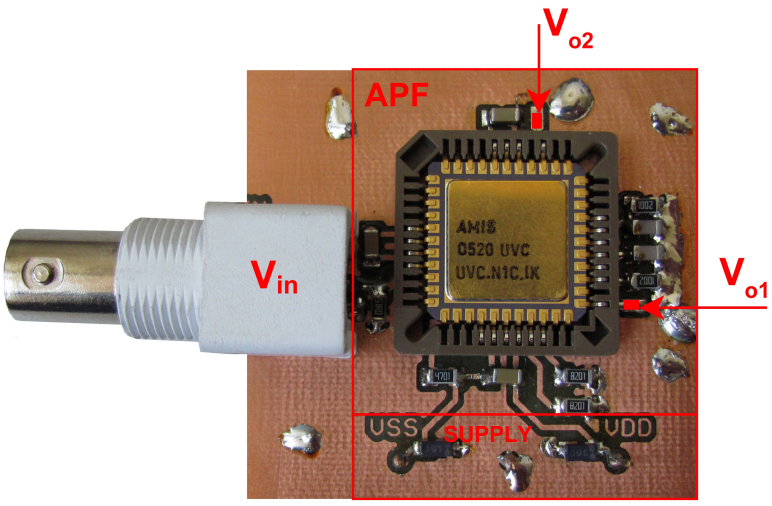

Figure 3. Developed printed circuit board (PCB) prototype.

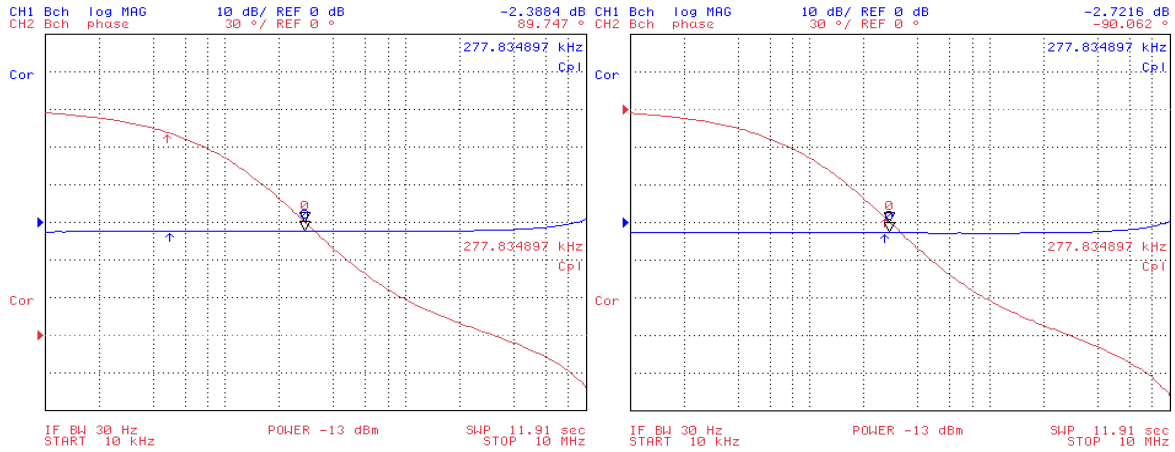

Figure 4. Measured magnitude (blue line) and phase (red line) responses of the VM APF for outputs: (**a**) V_{o1}; (**b**) V_{o2} with cursor position at f_{p_meas}.

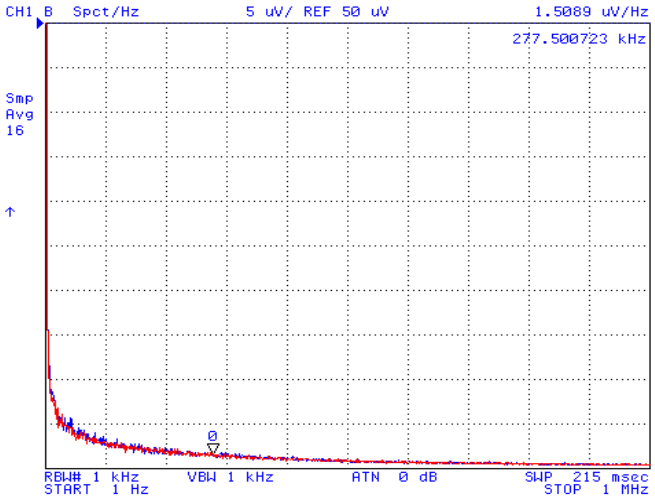

Figure 5. Measured noise variations for both voltage outputs versus frequency (red line—V_{o1}, blue line—V_{o2}).

Figure 6. Measured time-domain waveforms (blue line—input, orange line—V_{o1}, pink line—V_{o2}).

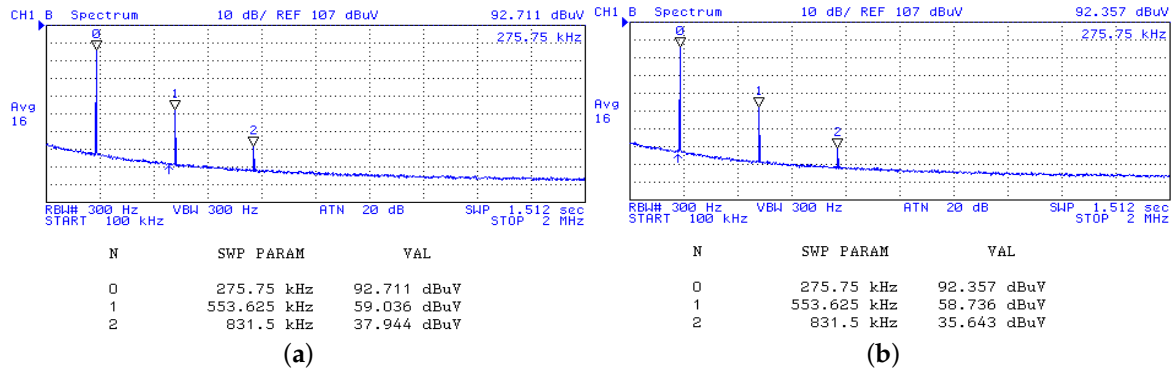

Figure 7. Measured Fourier spectrum of the output signals: (**a**) V_{o1}, (**b**) V_{o2}.

5. Conclusions

In this letter, the usefulness and unique features of UVC discussed above have been demonstrated in a VM first-order APF that offers advantages, such as: (i) simultaneously provides both inverting and non-inverting outputs from the same configuration; (ii) easy cascadability due to infinitely high input and zero output-impedances in theory; (iii) use of only grounded passive components (desirable for monolithic integration); (iv) complex passive components matching constraints are not required; (v) simple circuitry employing single ABB. Experimental measurement results based on the readily available UVC-N1C 0520 chip have proven the workability of the proposed VM APF.

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Author Contributions: Norbert Herencsar conceived the idea and performed the theoretical analysis; Jaroslav Koton and Pavel Hanak performed the experiments and analyzed the results; Norbert Herencsar and Jaroslav Koton wrote the letter.

Conflicts of Interest: The authors declare no conflict of interest.

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