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An Electronically Adjustable Floating Memcapacitor Emulator Circuit Using CDBA

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Abstract

Memristive elements, known as memristors, memcapacitors and meminductors, have become an important topic of research in the electronics world in recent years. As there is still no efficient way to manufacture two-terminal memristive elements, many researchers have focused their efforts on designing emulator circuits that mimic these devices. In this study, a memcapacitor emulator circuit using Current Derivative Buffered Amplifier (CDBA) is proposed, which has significant advantages such as wide dynamic range, differential structure at the input port, high sloping rate and wide bandwidth. The main advantages of the emulator are that it is floating without grounding constraint, it is electronically adjustable, it has charge-controlled incremental and decremental modes and it has a simpler circuit structure since it does not contain a memristor. To ensure the integrity of the circuit theory, the results of the mathematical model and the simulation of the memcapacitor are given together. In addition, the characteristics of the experimentally investigated memcapacitor emulator are in good agreement with the simulation results. To provide an illustration of the performance of the proposed emulator, firstly the second-order active low-pass filter circuit and subsequently the amoeba learning circuit are selected as the working environment. The results show that the filtering performance of the proposed emulator at a value after the cut-off frequency in the filter circuit is 25% more efficient than a standard capacitor and in terms of power consumption, it consumes 27.93% less power than a standard capacitor. Moreover, the emulator successfully accomplishes the learning and data storage tasks in the amoeba learning circuit.

Keywords: memristive elements; memcapacitor; emulator; floating property; CDBA

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1. Introduction

With developments in technology, a low power consumption and a high processing speed have become the most sought-after features in electronic circuits [1]. Memristive elements, called memristors, memcapacitors and meminductors, which are similar to the resistor, capacitor and inductor elements but have memory specialty, are expected to provide these features demanded by the developing electronics world [2]. The investigation of memristive elements first began in 1971 with the memristor element [3]. The main difference between a memristor element and a standard resistor is that the element is defined by the relationship between electric charge and magnetic flux, rather than current and voltage. However, the relationship between the current and voltage of the memristor is in the form of a hysteresis curve that varies with frequency. This feature makes it

possible to achieve new functions such as non-volatile memory and a variable resistance value depending on the direction and magnitude of the applied current [4]. After the discovery of the memristor element, its application areas have become a matter of curiosity and it has found a place in many areas, especially in neuromorphic systems [5–11], programmable Analog Circuits [12–14], chaotic circuits [15–17], image processing [18,19] and sensor applications [20–22].

In the following years, it was realized that the memory elements were not limited to the memristors, and new elements were introduced according to different relationships that had not been used before [23]. Accordingly, it was found that the relationship between the integral of the charge $\sigma(t)$ and the magnetic flux $\varphi(t)$ represents the memcapacitor element [24]. The memcapacitor is a lossless element and is more energy efficient compared to the memristor [25,26]. The ability of the memcapacitor to store energy without the need for a power source is one of the features that make this element interesting [27]. These properties of the memcapacitor make it possible to realize numerous applications such as chaotic oscillators [28–30], neuromorphic circuits [31–35], and logic circuits [36,37].

Circuit studies using memcapacitor elements are largely based on the use of various equivalent emulator designs in place of the element due to the lack of commercially available memcapacitor elements. Experimental performance, floating or grounded form, and electronic controllability are some important criteria for the quality of an emulator designed for the memcapacitor. A number of designs have been proposed for the memcapacitor in the literature [38–42]. In one study, a Current Backward Transconductance Amplifier (CBTA) element was used to form a mutator element, and a floating memcapacitor circuit was designed using this mutator element together with a grounded memristor and capacitor element [38]. In [39], a charge-controlled emulator model was proposed for grounded and floating memcapacitor emulators using two Second-Generation Current Conveyors (CCII), one analog multiplier (AM) and some passive elements. In another study [40], two memcapacitor emulators were proposed, one with two CCIIs and some passive elements and the other with one CCII, one Operational Transconductance Amplifier (OTA) and some passive elements, which were experimentally supported and designed to be electronically controllable. In [41], a floating memcapacitor emulator consisting of OTA, Voltage Difference Transconductance Amplifier (VDTA) and buffer obtained by using MOSFET transistors instead of ICs was designed and the results were experimentally verified. In another study using MOS technology, an emulator designed in floating mode with Dual X Current Conveyor Differential Input Transconductance Amplifier (DXCCDITA) element was simulated [42]. However, it can be seen that these emulators differ in the number of their active and passive elements, whether they are floating or grounded, experimentally verified, contain a memristor or are electronically controllable. Therefore, the design studies on memcapacitor emulator circuits continue with increasing interest.

In general, the work presented in this article includes the following innovations and contributions:

- In our work, the CDBA element, which has important advantages such as wide dynamic range, high slope speed, differential structure at the input port and which has not been used in the design of memcapacitor emulators in the literature to the best of our knowledge, was used.
- The memcapacitor emulator analyzed both in simulation and experimentally has the advantages of not having ground restriction, not having a memristor in its structure, being electronically adjustable and being able to operate in decreasing and increasing modes.
- The designed memcapacitor emulator successfully passed the tests of non-volatility, frequency-dependent variable characteristics, series-parallel connection characteristics and Fourier analysis.

- The proposed memcapacitor emulator circuit was implemented in a second-order active low-pass filter circuit and was found to be more efficient in both filtering performance and power consumption compared to the standard capacitor.
- The proposed memcapacitor emulator also successfully completed the learning and data storage tasks in the amoeba learning circuit.

The rest of the paper is organized as follows. Section 2 presents the proposed memcapacitor emulator circuit and its analytical model. The performance analysis is given in Section 3 to demonstrate the characteristics of the emulator. In Section 4, the applications of memcapacitor emulator-based active filter circuit and amoeba learning circuits are analyzed. Some conclusions are given in Section 5.

2. Proposed Memcapacitor Emulator Circuit

Classical circuit elements such as resistors, capacitors and inductors are expressed by the relationships between voltage, current, charge and flux, which are defined as fundamental electrical quantities. In contrast to these relationships, the definition of the memcapacitor is given by a relation of the form $F(\varphi, \sigma) = 0$ where φ and σ are the time integrals in $(-\infty, t]$ of the voltage and charge, respectively. If this relation is expressible as a map $\sigma \to \varphi$ $(\varphi \to \sigma)$, the memcapacitor is said to be charge- (voltage-) controlled. By assuming that either map is differentiable, we can express the voltage in terms of the charge (or vice versa) in the form $v = C_M^{-1}(\sigma)q$ $(q = C_M(\varphi)v)$, where

$$C_M^{-1}(\sigma) = \frac{v(t)}{q(t)} = \frac{d\varphi}{dt}\frac{dt}{d\sigma} = \frac{d\varphi}{d\sigma}, \tag{1}$$

$$C_M(\varphi) = \frac{q(t)}{v(t)} = \frac{d\sigma}{dt}\frac{dt}{d\varphi} = \frac{d\sigma}{d\varphi}. \tag{2}$$

Here, $C_M^{-1}(\sigma)$ is the inverse memcapacitance of the charge-controlled memcapacitor and $C_M(\varphi)$ is the memcapacitance of the voltage-controlled memcapacitor. This means that the quantity $C_M^{-1}(\sigma)$ $(C_M(\varphi))$ depends on the entire time history of the input variable. The memcapacitor therefore has a memory-dependent property and is an energy-storing electronic element [2,43]. Finally, in this work, we intend to design a charge-controlled memcapacitor emulator circuit that satisfies the following equation

$$v(t) = C_M^{-1}\left(\int_{t_0}^{t} q(\tau)d\tau\right)q(t). \tag{3}$$

However, (3) is inadequate to express any parasitic effects and has no internal state vector. Instead, it is more realistic to use the expression given by

$$v(t) = (\alpha \pm \beta\sigma(t))q(t). \tag{4}$$

Here, α is the initial value of the memcapacitance and β represents the capacitance change corresponding to the charge flow in the memcapacitor, respectively [42,44].

In this section, a new memcapacitor emulator based on the CDBA is proposed. The CDBA, whose block diagram is shown in Figure 1, is implemented using two current feedback operational amplifiers, commercially available as AD844. The CDBA is an active element with four terminals that can be used in current and voltage mode analog signal processing circuits and filters. The p terminal of the CDBA is called the positive (non-inverting) input and the n terminal is called the negative (inverting) input. Both input terminals are virtually grounded, making them the preferred current inputs. The z terminal is a current output and the w terminal is a voltage output, which follows the voltage of

the z terminal. The CDBA has low impedance inputs on the p and n terminals and a low impedance output on the w terminal. This allows it to be used as a cascadable active device [45]. The basic electrical descriptions of the terminals are expressed as follows

$$i_z = i_p - i_n,\ v_p = v_n = 0,\ v_w = v_z. \tag{5}$$

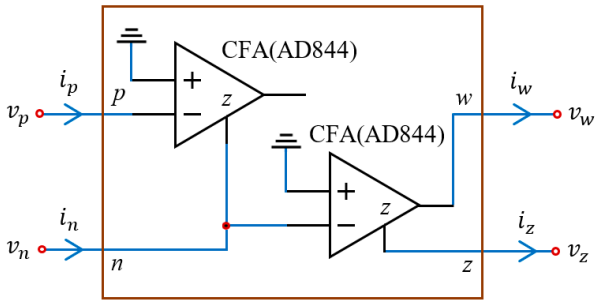


Figure 1. Internal structure of the CDBA.

Among these, the CDBA is notable for offering a balanced trade-off between performance and simplicity. It provides a wide bandwidth in the range of 10–100 MHz, moderate input-referred noise (approximately 20–80 nV/$\sqrt{}$Hz), and low to moderate power consumption (typically 200–600 µW) [46,47]. Thanks to its differential current input and buffered voltage output, the CDBA enables easy cascading in current-mode systems without significant loading effects or signal degradation.

Although Operational Transconductance Amplifier (OTA) structures can achieve very low noise levels (as low as 10–50 nV/$\sqrt{}$Hz) under optimized biasing conditions, they often suffer from limited linearity, narrow bandwidth (around 1–5 MHz), and pronounced sensitivity to process, temperature, and voltage variations [48], which can compromise reliability in practical designs.

The (Current Buffered Transconductance Amplifier) CBTA and Current Differencing Transconductance Amplifier (CDTA) architectures enhance the CDBA by integrating a controllable transconductance stage (g_m block) at the output, allowing electronic tuning of critical circuit parameters such as gain and cutoff frequency via an external control voltage or bias current. However, this added tunability comes at the cost of increased power consumption (typically 500–1200 µW), higher noise levels (ranging from 30 to 100 nV/$\sqrt{}$Hz), and greater structural complexity [49].

The Second-Generation Current Conveyor (CCII) offers excellent high-frequency performance, often achieving bandwidths exceeding 100 MHz, with noise performance in the 40–100 nV/$\sqrt{}$Hz range. However, its lack of a current differencing input makes it less suitable for differential signal processing applications where the CDBA naturally excels [50].

In conclusion, the CDBA offers a compelling combination of robust high-frequency behavior, moderate noise, high slope speed, linear differentiation, buffer output capability low power requirements, and design simplicity [51–53]. These attributes make it a strong candidate for use in high-performance analog and mixed-signal circuits, especially where design stability and signal integrity are critical. Taking these benefits into account, a CDBA-based memcapacitor emulator circuit is proposed as shown in Figure 2. The emulator circuit consists of a CDBA, an integrator, an operational amplifier and some passive elements. The mathematical analysis of the emulator circuit can be given as follows:

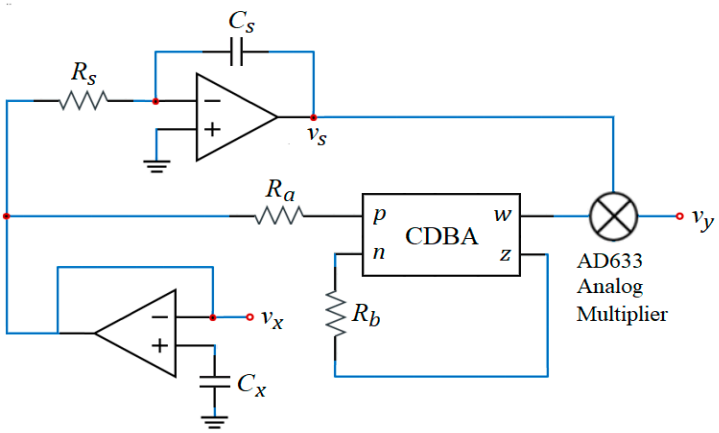


Figure 2. Schematic diagram of the proposed CDBA-based memcapacitor emulator circuit.

The input voltage of the emulator circuit with the floating characteristic is defined as

$$v_{in}(t) = v_x - v_y. \tag{6}$$

Here, v_x is equal to the voltage across capacitor C_x and is expressed by

$$v_x = v_{C_x} = \frac{1}{C_x}\int_{t_0}^{t} i_{C_x} dt = \frac{q(t)}{C_x}. \tag{7}$$

v_y is the output of the four quadrant AD633 analog multiplier and is given by the equation

$$v_y = \pm\alpha.v_s.v_w \tag{8}$$

where $\alpha = 1/(10 \text{ Volt})$ as a property of the AD633 and v_s is the integrator output. If the Y_1 terminal in the schematic of the AD633 is used, (8) takes a positive value, and if the Y_2 terminal is used, it takes a negative value. The current expression in (5) becomes $i_n = i_p/2$ because i_n is equal to i_z due to the resistor R_b in the emulator circuit. Therefore, the voltage of R_b can be written in the form of

$$v_{R_b} = i_n R_b = \frac{i_p R_b}{2} = v_z = v_w. \tag{9}$$

Since the voltage of R_a is equal to v_x and the current passing through R_a is equal to i_p, v_w is stated as

$$v_w = \frac{V_x R_b}{2R_a}. \tag{10}$$

The output of the integrator is

$$v_s = \frac{-1}{R_s C_s}\int v_x dt. \tag{11}$$

Taking into account (7), (11) becomes

$$v_s = \frac{-1}{R_s C_s C_x}\int_{t_0}^{t} q(t) dt. \tag{12}$$

Since the integral of the charge in time is denoted by σ, (12) can be expressed simply as follows

$$v_s = \frac{-1}{R_s C_s C_x}\sigma(t). \tag{13}$$

Using (10) and (13), the output of the analog multiplier in (8) is found as

$$v_y = \pm \frac{R_b V_x}{20 R_a R_s C_s C_x} \sigma(t). \tag{14}$$

The input voltage of the memcapacitor emulator and its inverse memcapacitance are obtained as

$$v_{in}(t) = v_x - v_y = \frac{q(t)}{C_x}\left(1 \mp \frac{R_b}{20 R_a R_s C_s C_x}\sigma(t)\right). \tag{15}$$

$$C_M^{-1} = \frac{v_{in}(t)}{q(t)} = \frac{1}{C_x} \pm \frac{R_b}{20 R_a R_s C_s C_x^2}\sigma(t). \tag{16}$$

As can be seen from (16), the inverse memcapacitance is a first-order polynomial function in the form of (4) with $\sigma(t)$ as its variable. This structure, consisting of fixed and variable parts, facilitates the implementation of the emulator. Moreover, the fact that the variable part of (16) can be easily controlled by using resistors and capacitors is one of the important advantages of the proposed emulator. If the sign of the variable part in (16) is taken as negative, then the inverse memcapacitance has a decreasing characteristic, and in this case the element is referred to as an *incremental memcapacitor*. Conversely, for the inverse memcapacitance with an increasing characteristic, corresponding to the variable part with a positive sign, the element is defined as a *decremental memcapacitor*.

The physical behavior of the proposed memcapacitor emulator can be interpreted in analogy with existing models of memory-based circuit elements. Unlike traditional capacitors with a constant capacitance value, memcapacitors exhibit a charge-dependent dynamic capacitance show in (1), which encodes memory of past electrical activity. This property is given in (16) where the inverse memcapacitance C_M^{-1} varies not only with a fixed base term $1/C_x$, but also through a time-dependent modulation term involving the signal $\sigma(t)$. This additional term, scaled by passive elements such as R_s, R_b, R_a, C_s, C_s implies that the effective capacitance is history-dependent. Such a structure parallels the physical analogies frequently employed in the literature; while a memristor is often likened to a deformable water pipe with resistance varying based on the history of current flow, a memcapacitor is analogously described as an elastic balloon whose stiffness changes depending on previous inflation cycles—that is, the amount of accumulated charge. Furthermore, the presence of the nonlinear term $\sigma(t)$ introduces a dynamic hysteresis in the charge–voltage relationship, akin to pinched hysteresis loops observed in memcapacitive systems.

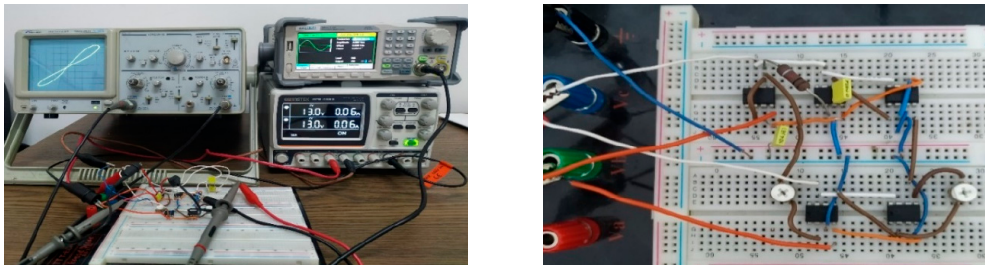
Since the realization of CDBA and analog multiplier with metal oxide semiconductor (MOS) transistors is well known in the literature, the proposed emulator is suitable for monolithic implementation in MOS transistor technology. Thus, it is possible to realize the integrated design of the proposed memcapacitor emulator using the MOS transistor models in [54,55] and obtain post-layout simulation results.

3. Simulation and Experimental Results

In order to confirm the theoretical results and demonstrate the feasibility and operating performance of the proposed memcapacitor, the emulator circuit in Figure 2 is simulated with Multisim program and also experimentally constructed with discrete circuit elements. The values of the passive elements for incremental and decremental memcapacitor emulators are $R_a = 60$ kΩ, $R_b = 80$ kΩ, $R_s = 1$ kΩ, and $C_x = 100$ nF. The value of C_s for the incremental memcapacitor is taken as 220 nF, while this value is 70 nF for the decremental memcapacitor.

In this section, simulation results are given to investigate the voltage–charge characteristics, volatility behavior, electronic controllability and Fourier analysis of the emulator. These results are verified with the results of the emulator circuit built on breadboard using

physical circuit elements as shown in Figure 3. All the elements used in the simulation circuit and the experimental circuit are the same. The CDBA element is obtained with AD844 opamps. The circuit can be considered quite simple, as shown in Figure 3b. The measurements were carried out with both digital and analog oscilloscopes. The digital oscilloscope used was a Uni-T UTD2052CL (Uni-Trend Technology (China) Co., Ltd., Dongguan, Guangdong, China), while the analog oscilloscope was a Twintex TOS-2020CH (Shenzhen Twintex Instrument Ltd., Shenzhen, Guangdong, China).



(a) (b)

Figure 3. Experimental implementation of the proposed memcapacitor emulator: (**a**) experimental platform, (**b**) breadboard circuit diagram.

3.1. Voltage–Charge Characteristics

The basic simulation results of the time responses of voltage and charge at 250 Hz for incremental and decremental memcapacitor emulators are given in Figure 4. The figure shows that for a sinusoidal input voltage, the charge is seen as a sinusoidal signal with the peak shifted to the right in the incremental memcapacitor, and as a signal with the peak shifted to the left in the decremental memcapacitor. The voltage–charge characteristics of the incremental and decremental memcapacitor emulators are given in Figure 5. It is seen from the figure that the voltage–charge characteristics exhibit pinched hysteresis characteristics for the memcapacitor. Once it was demonstrated that the proposed memcapacitor provides basic memcapacitor properties for both the incremental and decremental memcapacitors, from this point onward, only results based on the incremental memcapacitor emulator will be given. Figure 6 shows the pinched hysteresis voltage–charge curves and its variation with frequency. This is one of the main characteristics of the memcapacitor element. As expected, the area enclosed by the hysteresis curve narrows with increase in frequency value. Furthermore, to verify that the memcapacitor is a variable element with operating frequency, the range of memcapacitance values with respect to the applied voltage is shown in Figure 7. As can be seen from this figure, the range of the memcapacitance value decreases with increasing frequency.

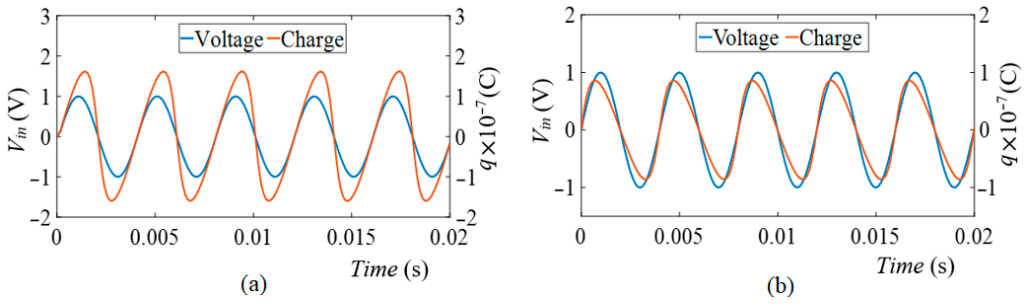


Figure 4. Voltage and charge time responses of the memcapacitor emulator circuits: (**a**) incremental, (**b**) decremental.

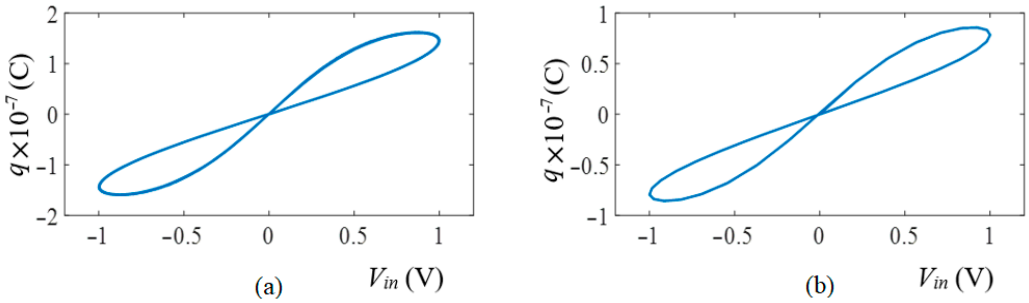


Figure 5. The voltage–charge characteristics of the memcapacitor emulator circuits: (**a**) incremental, (**b**) decremental.

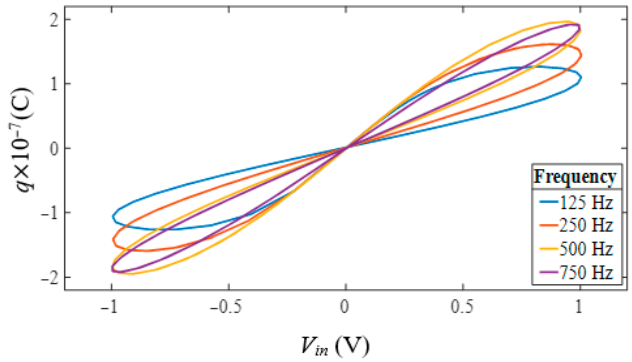


Figure 6. The voltage–charge characteristics at different operating frequencies.

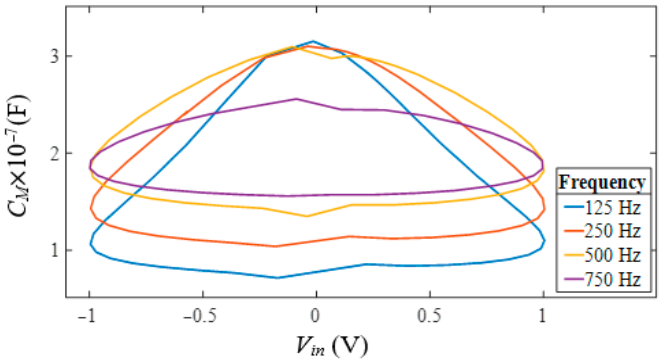


Figure 7. The voltage-memcapacitor characteristics at different operating frequencies.

Experimental results confirming the simulation results in Figure 6 are shown in Figure 8a,b. Again, the hysteresis range in the voltage–charge characteristics narrows with increasing frequency. From (12), it is seen that the voltage v_s is related to the memcapacitance charge and hence to the memcapacitance. Therefore, it can be seen in Figure 8c,d that the range of the v_s voltage, and hence the memcapacitance, decreases with increasing frequency when the v_s voltages at different frequencies are measured experimentally against the applied v_{in} voltages. This result indirectly confirms Figure 7 experimentally. Memcapacitor ranges calculated based on the obtained hysteresis curves are given in Table 1. The observed small differences between the simulation and experimental circuit results are mainly due to modeling ideality, physical parasitic effects, component tolerances and environmental conditions. While ideal conditions and component models are taken as a basis in simulation environments, real circuits are affected by various factors such as manufacturing variations, temperature changes, electromagnetic interference and measurement errors. In addition, the limited accuracy of the device models used and the ignoring of parasitic elements mean that the experimental results are not fully compatible.

In our study, although the simulation and experimental applications are largely consistent, a small difference is observed due to the reasons listed above.

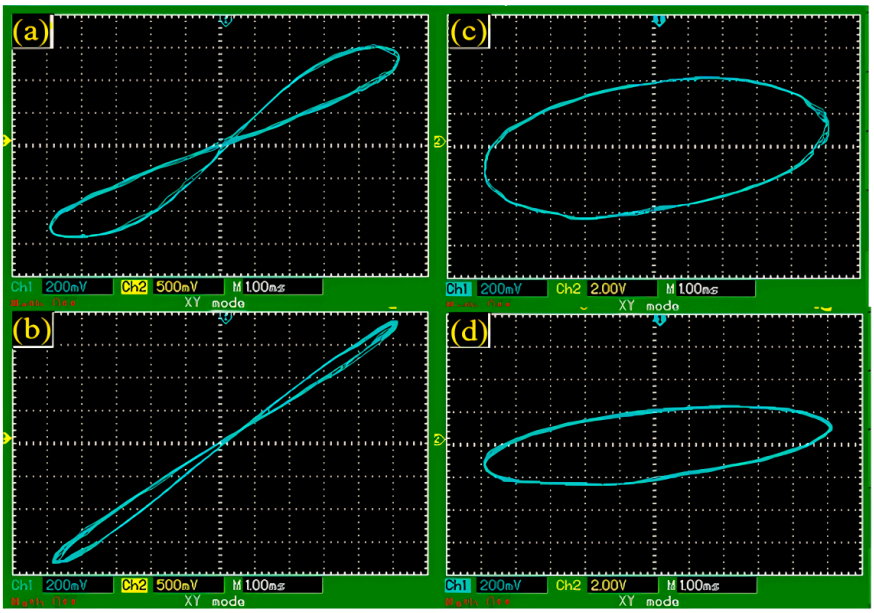


Figure 8. Experimental characteristics between $q - v_{in}$ and between $v_s - v_{in}$ at different frequencies: (**a**) 125 Hz $(q - v_{in})$, (**b**) 750 Hz $(q - v_{in})$, (**c**) 125 Hz $(v_s - v_{in})$, (**d**) 750 Hz $(v_s - v_{in})$.

Table 1. Memcapacitance (C_M) ranges obtained for different frequencies.

Frequency	CM Range	
	With Simulation	**With Experiment**
125 Hz	80–310 nF	80–260 nF
250 Hz	110–295 nF	100–235 nF
500 Hz	140–280 nF	125–210 nF
750 Hz	165–250 nF	130–205 nF

The proposed memcapacitor emulator may require connection in series or parallel in various electronic circuit applications. Therefore, a 300 Hz, 1 V sinusoidal input signal was applied to single, series and parallel connected memcapacitors, and the resulting charge–voltage relationships were investigated. As expected, more capacitor charge values are obtained with memcapacitors connected in parallel than with those connected single and in series, as illustrated in Figure 9.

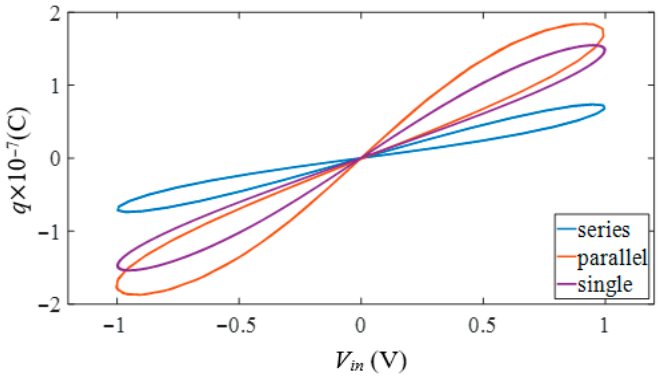


Figure 9. Voltage–charge characteristics of the memcapacitor emulator in single, series and parallel configurations.

3.2. Non-Volatile Memory Property

Non-volatile memory technologies are an important feature for new generation electronic and computer systems. A non-volatile memory test is performed to demonstrate the memory feature of memcapacitor emulators. This test for the proposed memcapacitor emulator was performed by applying a pulse wave with 200 mV amplitude and 20% pulse width to the input of the emulator. During each pulse, the memcapacitor charge follows the pulse as shown in Figure 10. When a pulse voltage is applied to the memcapacitor, the charge value increases and remains almost unchanged when the applied voltage is zero. An important feature is that when the pulse voltage is reapplied to the memcapacitor, the charge value continues to increase from the last value it took at the previous pulse value. As a result, the fact that the emulator circuit maintains the charge amount between two pulses proves that the proposed memcapacitor emulator has a non-volatile memory.

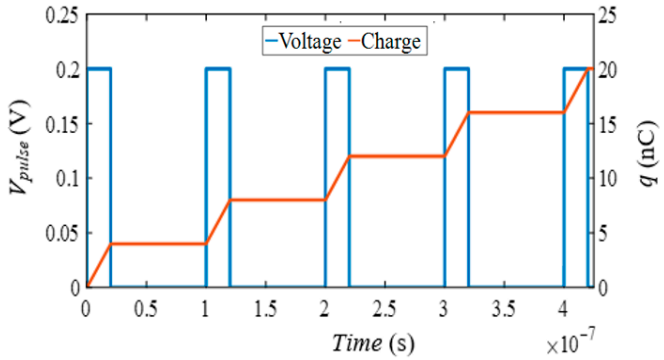


Figure 10. V_{pulse}-q values obtained for non-volatile testing of the designed emulator.

On the other hand, since this is an emulator circuit, small leakage currents are inevitable due to the active and passive elements used. If there is a very small change in the memcapacitor charge when the voltage applied to the circuit is interrupted and reapplied, this indicates a leakage current. In addition, by connecting 0 V DC voltage to the memcapacitor emulator, a leakage current of 53.8 pA was measured in the circuit. However, as can be seen from both Figure 10 and the leakage current test, the amount of leakage current is quite low.

3.3. Electronic Adjustability

Although it is an important feature of a memcapacitor emulator to be electronically adjustable, most of the emulators in the literature do not have this feature. The memcapacitor of the emulator proposed in this study can be tuned by changing the R_b and C_s values while the frequency value is fixed. For the 300 Hz frequency value, the memcapacitance change ranges obtained by first changing the value of R_b resistor and then C_s capacitor are given in Figure 11. In addition, the electronic tunability feature is also examined experimentally and compared with the simulation in terms of quantitative values in Tables 2 and 3. Although it is not possible to have one-to-one overlap of the quantitative results between the simulation and experimental applications considering the parameters such as tolerance values of the elements in the real world, sensitivity of the measurement instruments, etc., the results are quite consistent. The fact that the designed emulator provides electronically adjustable features by giving different memcapacitance ranges according to the change of element values in the circuit makes the proposed emulator stand out among those proposed in the literature.

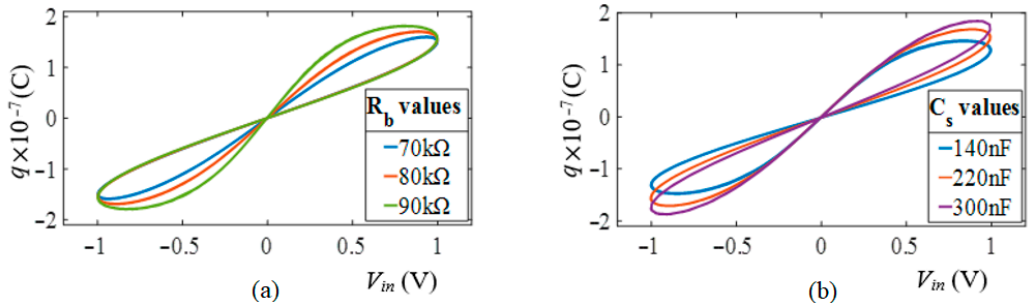


Figure 11. Voltage–charge characteristics of memcapacitor electronically controlled by (**a**) R_b, (**b**) C_s.

Table 2. Memcapacitance (C_M) ranges obtained for different C_s values.

Parameters	C_s	C_M Range Simulation	C_M Range Experimental
$R_s = 1$ **kΩ** $R_b = 80$ **kΩ** $R_a = 60$ **kΩ** $C_s = 100$ **nF**	140 nF	110–300 nF	110–285 nF
	220 nF	118–245 nF	115–225 nF
	300 nF	120–220 nF	120–210 nF

Table 3. Memcapacitance (C_M) ranges obtained for different R_b values.

Parameters	R_b	C_M Range Simuation	C_M Range Experimental
$R_s = 1$ **kΩ** $R_a = 60$ **kΩ** $C_s = 100$ **nF** $C_w = 220$ **nF**	70 kΩ	120–235 nF	123–208 nF
	80 kΩ	118–285 nF	115–260 nF
	90 kΩ	116–340 nF	110–290 nF

The upper frequency limit of the memcapacitor emulator we designed is approximately 25 kHz. Obtaining the memcapacitive behavior at this frequency depends on the passive components in the emulator. In Table 4, while the values of the other passive components are kept constant, the value of the capacitor C_s is changed to obtain different upper frequency limits. Thus, the operating range of the memcapacitor is considerably expanded, increasing its applicability in different applications.

Table 4. The upper frequency limit of the memcapacitor emulator according to the C_s.

Parameters	C_s	Upper Frequency Limit
$R_s = 50$ **Ω** $R_b = 80$ **kΩ** $R_a = 100$ **kΩ** $C_x = 100$ **nF**	20 nF	15 kHz
	10 nF	20 kHz
	5 nF	25 kHz

3.4. Sensitivity Analysis

The sensitivity analysis of the memcapacitor emulator connected to passive elements has also been studied. For this, (17) expresses the sensitivity analysis according to the inverse memcapacitor in (16) and X represents each passive element to be analyzed, respectively. The general form of the sensitivity analysis performed separately for each passive element is available in Table 5. According to Table 5, the sensitivity analysis results of the C_M^{-1} function show approximately how much C_M^{-1} will change when the value of each element is increased by 1%.

$$s_x^{C_M^{-1}} = \frac{X}{C_M^{-1}} \cdot \frac{\partial C_M^{-1}}{\partial X} \tag{17}$$

Table 5. Sensitivity analysis of memcapacitor emulator.

Parameters	Sensitivity Analysis
R_s	−1
R_b	1
R_a	−1
C_s	−1
C_x	−2

3.5. Fourier Analysis

Fourier analysis is an important method widely used in fields such as signal processing and vibration analysis, and shows that any signal can be expressed as a series of sine waves with different amplitudes and phases [56]. In this section, a Fourier analysis was performed on the electrical charge in the memcapacitor corresponding to the designed emulator. According to the result of this analysis shown in Figure 12, the fundamental harmonic was observed at a frequency of 1 kHz, and the second harmonic was observed at a frequency of 2 kHz with very small amplitude. The total harmonic distortion (THD) in the memcapacitor was found to be 1.05% at this frequency. The fact that the harmonics other than the fundamental harmonic are quite small supports this result. Since the memcapacitor charge signal is closer to the sinusoidal signal at high frequencies, it is normal for the Fourier analysis and the THD calculated accordingly to be quite low. As the frequency value decreases, the memcapacitor charge signal is a sinusoidal signal with a slope depending on the increasing or decreasing forms (since the q-v characteristic widens). Therefore, it is possible that the harmonics other than the fundamental harmonic are slightly more pronounced. This causes the THD at low frequencies to be slightly higher than the THD at high frequencies. In general, higher-order harmonics are not observed in the Fourier analysis due to the compressed charge–voltage relationship created by the emulator.

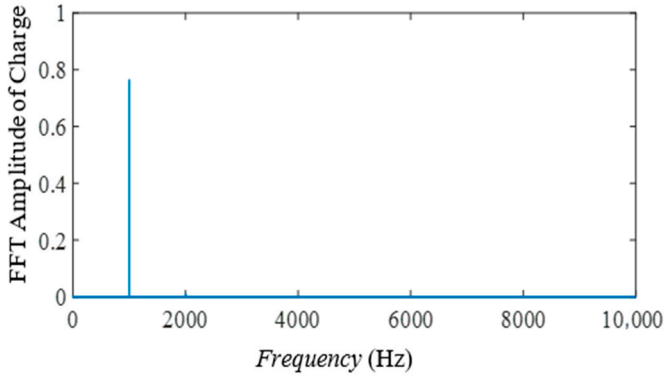


Figure 12. Fourier analysis of the memcapacitor emulator.

In order to examine the performance quality of our designed emulator and its contributions to the literature, the examination and comparison of current studies in the literature in terms of the parameters determining the performance quality are provided in Table 6 below. Compared to the memcapacitor emulator designs presented in the existing literature, the proposed circuit design exhibits a balanced performance in terms of circuit complexity, frequency response and practical applicability. Unlike circuits based solely on simulation data, our study has experimental data compatible with simulation. Some emulators have memristors in their structure or are designed with a large number of active elements, making them complex and costly; in this context, our emulator is at a medium cost. In addition, our circuit, which operates reliably up to approximately 25 kHz, offers higher

performance than grounded or floating emulators that can only operate at lower frequency ranges. Moreover, it provides adaptability to various applications thanks to its electronically adjustable structure. This feature constitutes a significant advantage over studies that do not offer electronic control. All these features make the proposed emulator a powerful and applicable alternative for low and medium frequency analog memory applications.

Table 6. Performance comparison of memcapacitor emulator.

Ref.	Components	Complexity	Frequency Performance	Floating/Grounded	Sim/Exp.	Electronic Control	Cost
[40]	2 CCII, 1 AM 1 R, 3 C	Medium	2 kHz	Grounded	Simulation Experimental	Yes	Medium
[41]	1 VDTA,1 OTA, 1 buffer, 1 R, 2 C	Medium	~ 1.2 MHz	Floating	Simulation Experimental	No	Medium
[57]	4 CCII, 1 Opamp, 1 Varactor Diode, 6 R, 2 C	High	8 kHz	Floating	Simulation Experimental	No	High
[58]	1 FDCCII, 1 AM, 2 MOSFETs, 3 C	Medium	1 MHz	Grounded	Simulation Only	Yes	Medium
[59]	4 CCII, 1 Memristor, 1 L1 R	High	Not specified	Floating	Simulation Only	No	High
This study	1 CDBA, 2 opamp, 1 AM, 3 R, 2 C	Medium	~ 25 kHz	Floating	Simulation Experimental	Yes	Medium

4. Application Examples

4.1. Second-Order Active Low Pass Filter

In this section, in order to observe the performance of the proposed memristor emulator in a real circuit, a second-order active low-pass filter (2nd order active LPF) circuit is implemented as shown in Figure 13. In the circuit, instead of the standard capacitor with a value of 210 nF, a memcapacitor emulator with the same average memcapacitance value is used. The values of the other passive elements are $R = 22$ kΩ, $R_1 = 10$ kΩ and $C_1 = 70$ nF and the cut-off frequency of the filter circuit is $f_c = 1/2\pi RC_1 = 103.34$ Hz. The effect of the memcapacitor on the circuit is analyzed and the results are compared. Figure 14 shows the voltage-frequency characteristics of the active low pass filter circuit when both the standard capacitor and the memcapacitor are used. It can be seen from Figure 14 that the low-pass filter with the memcapacitor is more effective than the standard capacitor filter in suppressing the signals. In order to verify this result, the filter circuit was implemented experimentally and it is seen in Figure 15a,b that the amplitude of the output voltage of the memcapacitor filter at a frequency of 300 Hz is 0.23 V, while the amplitude of the standard capacitor circuit is 0.32 V. This finding indicates that the memcapacitor filter circuit exhibits more efficient filtering performance than the standard capacitor filter in the stopband.

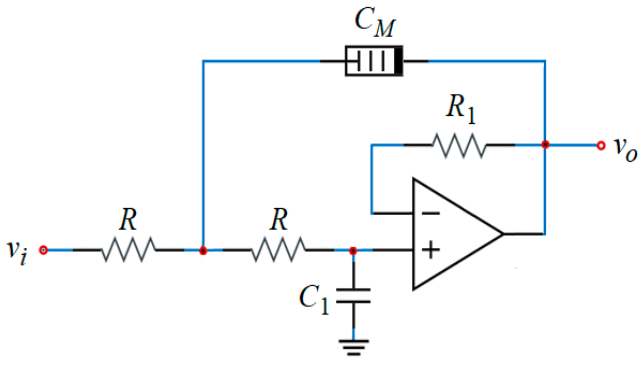


Figure 13. Second-order active LPF circuit with memcapacitor.

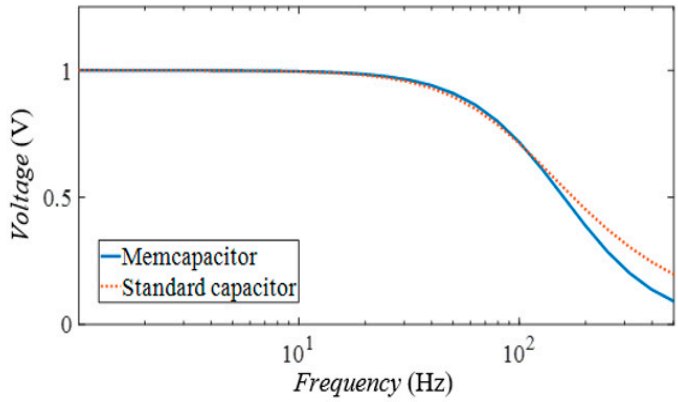


Figure 14. Filter frequency characteristics for standard capacitor and memcapacitor.

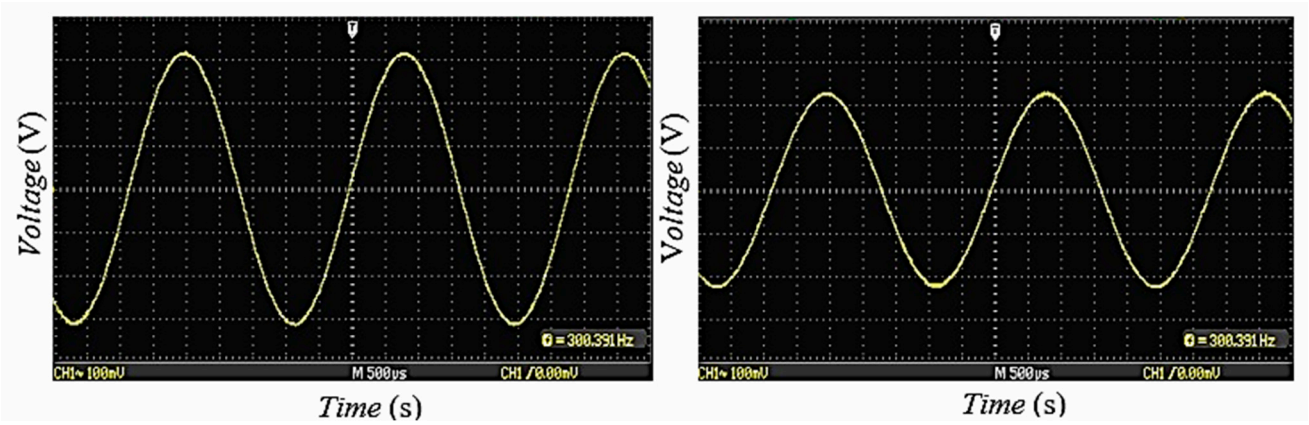


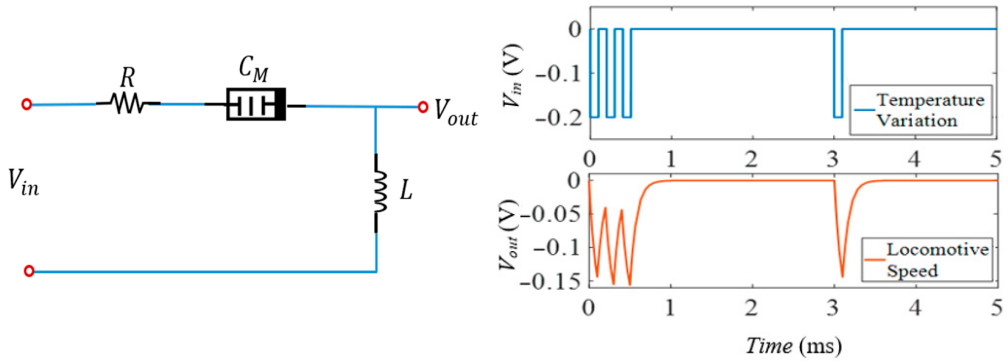
Figure 15. Experimental output voltages of 2nd order active LPF circuit with (**a**) standard capacitor, (**b**) memcapacitor at 300 Hz.

A further analysis of the filter circuit involves the comparison of the reactive power value for the capacitor selected in the circuit. The reactive power values calculated using the formula $Q = -i^2 X_c$ are $Q_{C_M} = -10.84$ µVAR for the memcapacitor, and $Q_c = -15.04$ µVAR for the standard capacitor. This analysis indicates that the memcapacitor in the filter circuit consumes less reactive power than the standard capacitor and therefore has better performance in this respect. This real electrical circuit application demonstrates that the utilization of the recommended memcapacitor emulator in place of the standard capacitor yields more efficacious electrical results.

4.2. Amoeba Learning Circuit

The memory property of memcapacitors opens up a range of application areas in different electronic circuits. In this application, an RLC circuit containing a memory element is considered, which is used to electrically model the ability of amoeba-like cells to adapt their actions and change speed according to approaching stimuli such as temperature and humidity [44,60]. The series RLC circuit depicted in Figure 16a is subjected to a pulse signal with an amplitude of 200 mV as the input signal on three occasions in succession at 0.1 ms intervals and once after 3 ms. Figure 16b shows the graphs of the locomotive movement of the amoeba corresponding to the output signal for the temperature change corresponding to the input signal. As is evident from the figure, it is seen that the voltage corresponding to the locomotive speed decreases at each temperature drop point and the locomotive speed of the amoeba decreases gradually compared to the previous drop due to the decreasing temperature at the triple input signal. This result clearly demonstrates that

the memcapacitor circuit has a learning and memory feature when a signal is applied more than once.



(**a**) (**b**)

Figure 16. (**a**) Amoeba's learning circuit using memcapacitor emulator ($R = 1$ kΩ and $L = 1$ mH). (**b**) Response of the amoeba's learning application.

5. Conclusions

In this paper, an electronically tunable memcapacitor emulator circuit designed using CDBA element is presented both in mathematical analysis, simulation and experimental aspects. The development of technology has led to the increasing use of memristive elements in various scientific and technological fields. Mem elements, which are applied in many fields such as communication, neural networks, chaos, biology etc., are currently not available in the market as a commercial two-terminal element, which emphasizes the importance of designing better emulators to emulate them. The main advantages of the CDBA-based memcapacitor emulator proposed in this study are that it has a floating structure without grounding restriction, does not contain a memristor in its structure, has both incremental and subtractive forms and has an electronically tunable feature. The designed emulator has successfully passed the tests of frequency-dependent stepwise charge–voltage and memcapacitance-voltage characteristics, single-serial-parallel connection characteristics, non-volatility, Fourier analysis and electronic tunability. The performance of the proposed memcapacitor emulator was tested in two different electronic circuit applications and we found that it has the potential to provide significant advantages in various electronic applications. According to the measurement results, the memcapacitor emulator has 25% better filtering ability and 27.93% less power consumption compared to the standard capacitor in the low-pass filter circuit. In addition, the emulator effectively performs the learning and data storage functions in the amoeba learning circuit. It is thought that further studies on the proposed emulator circuit will make significant contributions to the literature by evaluating various electrical properties such as signal speed, power efficiency, chaotic signal generation, signal regulation, and investigating additional benefits.

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