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An Enhanced Integrated Optimization Strategy for Wide ZVS Operation and Reduced Current Stress Across the Full Load Range in DAB Converters

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Abstract

The dual-active-bridge (DAB) converter has emerged as a promising topology for renewable energy applications and microgrid systems due to its high power density and bidirectional energy-transfer capability. Enhancing the overall efficiency and reliability of DAB converters requires the simultaneous realization of zero-voltage switching (ZVS) across all switches and the minimization of current stress over wide load and voltage ranges—two objectives that are often in conflict. Conventional modulation strategies with limited degrees of freedom fail to meet these dual goals effectively. To address this challenge, this paper introduces an enhanced integrated optimization strategy based on triple phase shift (EIOS-TPS). This approach formulates the power transmission requirement as an equality constraint and incorporates ZVS and mode boundary conditions as inequalities, resulting in a comprehensive optimization framework. Optimal phase-shift parameters are obtained using the Karush–Kuhn–Tucker (KKT) conditions. To mitigate zero-current switching (ZCS) under a light load and achieve full-range ZVS with reduced current stress, a modulation factor λ is introduced, enabling a globally optimized control trajectory. An experimental 1176 W prototype is developed to validate the proposed method, which achieves full-range ZVS while maintaining low current stress. In the low-power region, it improves efficiency by up to 2.2% in buck mode and 2.0% in boost mode compared with traditional control strategies, reaching a peak efficiency of 96.5%.

Keywords: dual-active-bridge (DAB) converter; zero-voltage switching (ZVS); minimize current stress (MCS); regulatory factor λ; full load range

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1. Introduction

The dual-active-bridge (DAB) converter, a high-frequency DC–DC conversion topology, was first proposed in the 1990s [1]. After decades of development, the DAB converter has been widely adopted in various applications, including DC microgrids [2,3], new energy vehicles [4,5], energy storage systems [6,7], and aerospace systems [8], due to its advantages of bidirectional power flow, galvanic isolation, high power density, soft-switching capability, and multi-voltage adaptability [9,10]. However, achieving high efficiency across a wide load range remains a key challenge in these applications [11]. The current approaches to improving DAB converter efficiency focus on two aspects: optimizing the current waveform of an inductor using advanced control methods to suppress conduction losses, and facilitating soft-switching to minimize switching losses [12,13].

Among the various strategies developed for inductor current waveform optimization, current-stress optimization (CSO) [14–16] and root-mean-square current optimization (RMSO) [17–20] have been shown to effectively reduce conduction losses. In this context, current stress is characterized by the peak value of the inductor current. While both techniques offer comparable current optimization performance, RMSO suffers from significant limitations. Specifically, analytical solutions often involve square root terms, posing implementation challenges for digital controllers [17,18]. For numerical solutions, the modulation schemes are typically unsuitable for real-time computation, heavily reliant on control chips, and lack generality and portability [19,20]. In contrast, CSO demonstrates higher practicality and adaptability in engineering applications.

For both Si MOSFETs and SiC MOSFETs, turn-on losses dominate over turn-off losses [18,21], making ZVS particularly critical. ZVS realization criteria are generally classified into three categories: energy-based (EB ZVS) [22,23], current-based (CB ZVS) [17,24], and charge-based (QB ZVS) [25,26]. While CB ZVS is theoretically less accurate than EB ZVS and QB ZVS, it offers higher engineering feasibility and is better suited for practical applications. From a device perspective, SiC MOSFETs, with significantly lower junction capacitance compared to Si MOSFETs, require lower switch–current thresholds for ZVS, making ZVS more easily achievable. ZVS implementation methods fall into two main categories: topology modifications [27,28] and control strategy optimizations. Although topology modifications can achieve ZVS, they increase system cost and converter complexity. In contrast, control-based ZVS techniques, which rely solely on algorithmic adjustments without additional hardware changes, provide a more economical and practical solution for soft-switching operation.

For conventional DAB converters operating at a fixed switching frequency, modulation strategies are typically categorized by their degrees of freedom: single-degree-of-freedom (single phase-shift modulation, SPS), two-degrees-of-freedom (dual phase-shift modulation, DPS, and extended phase-shift modulation, EPS), and three-degrees-of-freedom (triple phase-shift modulation, TPS). Among these, TPS serves as the fundamental form, with SPS, DPS, and EPS regarded as special cases [29,30]. SPS modulation suffers from significant limitations, including a narrow ZVS range, high current stress, and large inductor current RMS values, especially under light load conditions or voltage conversion ratio mismatches. These issues lead to reduced efficiency and limited applicability [31,32].

In contrast, higher-degree modulation strategies such as DPS, EPS, and TPS offer greater flexibility, enabling reduced current stress and extended ZVS operation. To address these challenges, various phase-shift modulation methods have been proposed, including DPS [33–37] and EPS [38,39]. For instance, the authors of [33] investigated efficiency characteristics and optimization techniques under wide DC-link voltage variations, highlighting limited light-load performance. The study detailed in [34] improved light-load performance via bidirectional conduction angle control, but at the expense of losing ZVS for one half-bridge on the secondary side. In [35], the authors proposed a current-stress optimization (CSO) DPS strategy, which reduces current stress but introduces higher system losses in the medium power range compared to EPS, resulting in limited efficiency gains [30,40]. The approach in [36] optimizes current stress via magnetizing inductance control, which is effectively a topology modification that enables full-load ZVS only in buck mode. In [37], the authors introduced a CSO-DPS strategy that reduces current stress under buck and boost modes, yet with limited ZVS capability. Using EPS modulation, the authors of [38] proposed an optimized power control (OPCB-EPS) strategy to minimize current peaks. While effective in medium power ranges, OPCB-EPS remains suboptimal at low power [30]. For TPS modulation, studies [14–16,41–49] have explored various optimization strategies aimed at minimizing current stress and expanding the ZVS range. Notably, the authors

of [14] proposed a CSO-TPS strategy that provides optimal phase-shift combinations across the full load range, a result corroborated by [15,16] using different analytical approaches. However, these works primarily focus on current-stress minimization, neglecting the ZVS range and the impact of switching losses on overall efficiency, limiting their effectiveness in efficiency optimization. In [41], the authors proposed a strategy that achieves ZVS for six switches under medium-load conditions, full-switch ZVS at light and heavy loads, and near-optimal peak inductor currents in both buck and boost modes; however, it still leaves two switches without ZVS at medium loads, increasing switching losses. In [42], the authors explored TPS optimization using reinforcement learning (RL) and artificial neural networks (ANN), though RL systems face challenges for real-time industrial deployment. In [43], the authors employed artificial intelligence (AI) techniques to build current-stress models from simulation data and applied particle swarm optimization (PSO) and fuzzy inference systems (FIS) to learn and store optimal modulation results. However, this approach relies on extensive simulation or experimental data and requires optimizing each operating condition separately, resulting in a complex and time-consuming process. In [44], the authors creatively proposed a reactive power controller based on triple phase shift, which significantly reduces the inductor current under all load conditions by optimizing the reactive power. However, the ZVS performance over the full operating range has not been further explored. In [45], the authors perform nonlinear modeling of the switching process, improving ZVS performance and achieving high efficiency across the full load range. However, the method is implemented based on lookup tables, preventing real-time computation and limiting portability. In [46], the author proposed an optimal primary-side duty cycle modulation scheme to reduce current stress; however, its performance under light-load conditions still has room for improvement [47]. Moreover, although the ZVS range is extended compared to SPS, full-switch ZVS cannot be achieved under high voltage conversion ratios and elevated power transfer conditions. In [48], the authors explored the intrinsic correlation between current stress and RMS optimization under TPS control and proposed an optimization strategy; however, ZVS analysis was omitted. Additionally, the switching frequency was limited to 5 kHz, leaving the effectiveness under high-frequency operation unverified. In [49], a triple phase shift-based approach was proposed to minimize current stress under varying DC-link voltages. Although minimum current stress was achieved under light-load conditions, full ZVS was not ensured for all switches.

To overcome the inherent limitations of conventional modulation strategies, this paper proposes an enhanced integrated optimization strategy based on triple phase shift (EIOS-TPS). This strategy employs time-domain analysis and formulates current peak minimization as the optimization objective, solved using the KKT conditions. The ZVS criterion is simplified by using current direction determination, and TPS, as the highest degree-of-freedom modulation strategy, is adopted without modifying the DAB converter topology. The proposed EIOS-TPS balances the trade-off between ZVS realization and current-stress optimization (CSO), enabling full-switch ZVS and minimal current stress across the entire load range under both buck and boost modes. Furthermore, EIOS-TPS requires no hardware modifications, ensuring high software portability and ease of implementation.

2. DAB Topology and Modeling Analysis

2.1. DAB Basic Topology

Figure 1 presents the topology of the DAB converter, which comprises two full-bridge circuits, denoted as FB_1 and FB_2. Each full bridge is constructed from a pair of half-bridge modules, with FB_1 consisting of HB_1 and HB_2, and FB_2 comprising HB_3 and HB_4. FB_1 and FB_2 are interconnected via a high-frequency transformer with a defined turns ratio of n:1. The inductor L represents the total inductance, encompassing both the leakage inductance

of the transformer and any additional external series inductance. The direction of positive power flow is defined as flowing from V_1 to V_2. The voltage conversion ratio is given by $k = V_1/nV_2$. A value of $k > 1$ corresponds to buck-mode operation, while $k < 1$ indicates operation in the boost mode.

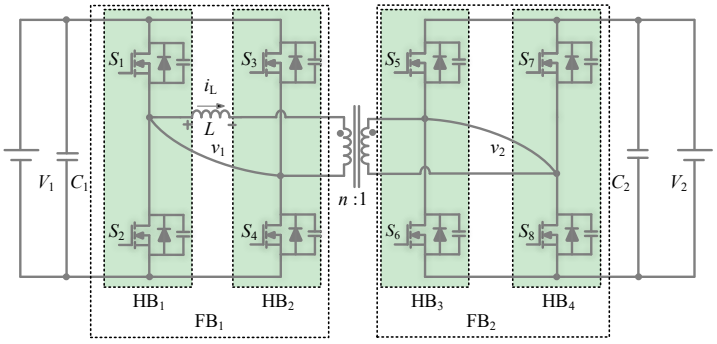


Figure 1. The topology of the DAB converter.

Figure 2 illustrates the operating waveforms of the DAB converter under TPS modulation. Here, D_1 and D_2 represent the duty cycles of v_1 and v_2, respectively, while Φ denotes the phase shift between the centers of v_1 and v_2. The ranges of D_1, D_2, and Φ are within [0,1]. T_s is the switching period, and f_s is the switching frequency, with $T_{hs} = T_s/2$. The parameters D_1, D_2, and Φ serve as the three key control variables in the TPS modulation strategy. These variables collectively shape the leakage current waveform, define the peak inductor current, and govern the average power transferred from the primary side to the secondary side.

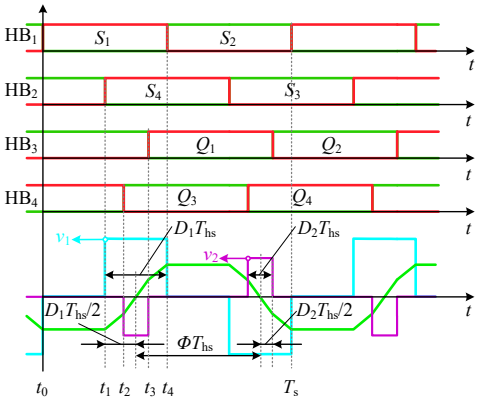


Figure 2. Triple phase-shift modulation waveforms of DAB.

2.2. ZVS Conditions of DAB Converter

In SiC MOSFET-based DAB converters, ZVS is attainable only when the junction capacitance of the switching device is completely discharged and a reverse current flows through the body diode to initiate conduction. The required polarity of the inductor current for achieving ZVS across different switches is summarized in Table 1.

Table 1. The required polarity of the inductor current for achieving ZVS in the DAB converter.

Polarity of the Inductor Current	Switches
$i_L < 0$	S_1, S_4, S_6, S_7
$i_L > 0$	S_2, S_3, S_5, S_8

2.3. TPS Mode Classification and Mode Selection of the DAB Converter

Figure 3 illustrates the typical voltage and current waveforms under the eight TPS modulation modes. The transmitted power for each mode is derived according to (1), and Table 2 summarizes the constraint conditions and normalized power expressions for each mode. In this work, p denotes the normalized power transferred through the converter. The transmitted power is normalized against the maximum transmitted power of the SPS modulation, defined as $P_n = nV_1V_2/8f_sL$.

$$\mathrm{P} = \frac{1}{T_{\mathrm{hs}}}\int_0^{T_{\mathrm{hs}}} v_1 i_L(t)dt \tag{1}$$

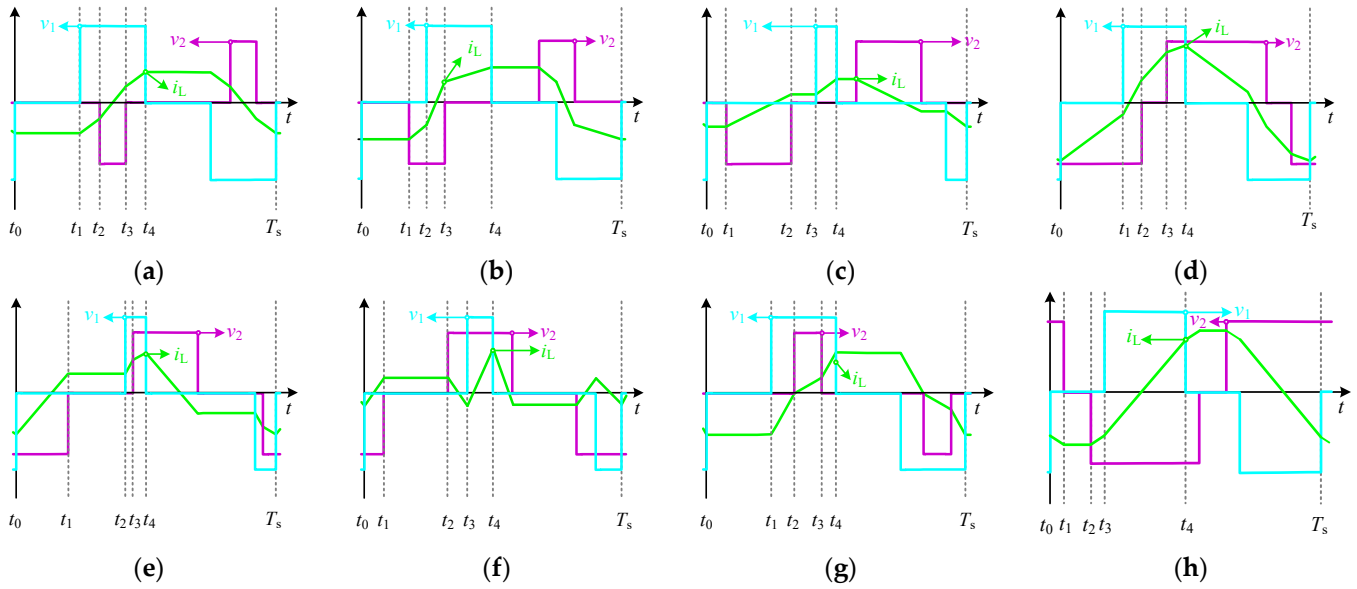


Figure 3. Typical voltage and current waveforms under eight TPS modulation modes. (**a**) Mode A. (**b**) Mode B. (**c**) Mode C. (**d**) Mode D. (**e**) Mode E. (**f**) Mode F. (**g**) Mode G. (**h**) Mode H.

Table 2. Constraints, transmitted power expressions, and operating ranges of eight modulation modes.

Mode	Mode Constraints	Expression of Normalized Transmitted Power p	Range of p
A	$1+\frac{D_1-D_2}{2} \le \Phi \le 1+\frac{D_2-D_1}{2}$	$4D_2(1-\Phi)$	[0, 0.5]
B	$\min\left\{\frac{D_1+D_2}{2}, 1-\frac{D_1+D_2}{2}\right\} \le \Phi \le \min\left\{1+\frac{D_2-D_1}{2}, 1+\frac{D_1-D_2}{2}\right\}$	$2D_1D_2-2\left(\Phi+\frac{D_1+D_2}{2}-1\right)^2$	[0, 0.5]
C	$\frac{D_1+D_2}{2} \le \Phi \le 1-\frac{D_1+D_2}{2}$	$2D_1D_2$	[0, 0.5]
D	$1-\frac{D_1+D_2}{2} \le \Phi \le \frac{D_1+D_2}{2}$	$1-(1-D_1)^2-(1-D_2)^2-(1-2\Phi)^2$	[0, 1]
E	$\min\left\{\frac{D_1-D_2}{2}, \frac{D_2-D_1}{2}\right\} \le \Phi \le \min\left\{\frac{D_1+D_2}{2}, 1-\frac{D_1+D_2}{2}\right\}$	$-\frac{(D_1-D_2)^2}{2}+2(D_1+D_2)\Phi-2\Phi^2$	[0, 0.666]
F	$0 \le \Phi \le \frac{D_2-D_1}{2}$	$4D_1\Phi$	[0, 0.5]
G	$0 \le \Phi \le \frac{D_1-D_2}{2}$	$4D_2\Phi$	[0, 0.5]
H	$1+\frac{D_1-D_2}{2} \le \Phi \le 1+\frac{D_2-D_1}{2}$	$4D_1(1-\Phi)$	[0, 0.5]

All eight modulation modes support forward power transfer. However, modes A, B, C, and H do not feature intervals in which v_1 and v_2 exhibit the same polarity. As a result, direct energy transfer from the primary to the secondary side is not possible. Instead, these modes rely on the inductor to temporarily store and transfer energy, which leads to elevated current stress and increased conduction losses. Therefore, under forward power transmission conditions, only modes D–G are practically meaningful for optimization. This

study aims to optimize the operational performance of the DAB converter in both buck and boost modes under forward power transfer. The current stress is characterized by the peak inductor current corresponding to each operating mode. By analyzing the voltage and current waveforms of the converter, the current stresses associated with modes D through G in both buck and boost scenarios are analytically derived and systematically presented in Table 2.

The current stress is normalized as $I_n = nV_2/4f_sL$, where the actual inductor current is represented by $i_L(t_x)$, and the normalized current is denoted as $i_{Ln}(t_x)$, with x = 0, 1, 2, 3, 4, The current stress corresponding to each mode is indicated as i_{py} , where y = D, E, F, G. The normalized inductor current values at each time instant for modes D–G are presented in Table 3. Table 4 summarizes the peak current stresses for these four operating modes under both buck and boost conditions.

Table 3. The normalized inductor current values at each time instant for modes D–G.

Mode	$i_{Ln}(t_0)$	$i_{Ln}(t_1)$	$i_{Ln}(t_2)$	$i_{Ln}(t_3)$	$i_{Ln}(t_4)$
D	$D_1(1-k)-2\Phi$	$2-D_1(1+k)-2\Phi$	$D_2(1+k)+2k(-1+\Phi)$	$D_2(1-k)+2k\Phi$	$D_1(-1+k)+2\Phi$
E	$D_1(1-k)-2\Phi$	D_2-D_1k	D_2-D_1k	$D_2(1-k)+2k\Phi$	$D_1(-1+k)+2\Phi$
F	$D_1(1-k)-2\Phi$	D_2-D_1k	D_2-D_1k	$D_1(1-k)+2\Phi$	$D_1(-1+k)+2\Phi$
G	D_2-D_1k	D_2-D_1k	$D_2(1-k)+2k\Phi$	$D_2(-1+k)+2k\Phi$	D_1k-D_2

Table 4. Maximum current stress of modes D, E, F, and G.

Mode	Maximum Current Stress When $k > 1$	Maximum Current Stress When $k < 1$
D	$D_1(-1+k)+2\Phi$	$D_2(1-k)+2k\Phi$
E	$D_1(-1+k)+2\Phi$	$D_2(1-k)+2k\Phi$
F	$D_1(-1+k)+2\Phi$	$\max\{D_2-D_1k, D_1(-1+k)+2\Phi\}$
G	D_1k-D_2	$\max\{D_2(1-k)+2k\Phi, D_1k-D_2\}$

3. Principle of the Proposed EIOS-TPS

Under the same transmitted power requirement, there exist infinitely many solutions for the combination of D_1, D_2, and Φ. The current stress depends not only on D_1, D_2, and Φ but also on the voltage conversion ratio k. For a given transmitted power p and k, the objective is to determine the combination of D_1, D_2, and Φ that minimizes the current stress. This problem is a constrained optimization problem, where the equality constraint enforces transmitted power consistency, and the inequality constraints include the ZVS condition and mode-selection restrictions. To solve this problem, an enhanced integrated optimization strategy based on TPS (EIOS-TPS) is proposed in this paper. Karush–Kuhn–Tucker (KKT) conditions and the Lagrange multiplier method (LMM) are applied to address the formulated optimization problem. The resulting solution space is then further refined to extract the optimal trajectory, which ensures ZVS for all switches over the entire load range while simultaneously minimizing current stress.

3.1. Modulation Strategy in the Low-Power Range When k > 1

When the DAB converter operates in buck mode under low-power conditions, mode E is identified as the optimal switching strategy for the DAB converter. Taking mode E as a representative case, the corresponding Lagrange function is established to characterize the interdependence among normalized current stress, normalized transferred power, ZVS constraints, and the duty-cycle limitations inherent to the operating mode, as formulated below:

$$\begin{aligned} L_{\mathrm{f}} = & -D_1 + D_1 k + 2\Phi + \lambda\left(-\frac{(D_1-D_2)^2}{2} + 2(D_1+D_2)\Phi - 2\Phi^2 - p\right) \\ & + \mu_1\left(\frac{D_1-D_2}{2} - \Phi\right) + \mu_2\left(\Phi - \left(1 - \frac{D_1+D_2}{2}\right)\right) + \mu_3\left(\frac{D_2-D_1}{2} - \Phi\right) + \mu_4\left(\Phi - \frac{D_1+D_2}{2}\right) \end{aligned} \tag{2}$$

where λ denotes the equality constraint multiplier, and the μ_i values (i = 1, 2, 3, 4) denote the inequality constraint multipliers. By applying the LMM and the KKT conditions, the following results can be obtained:

$$\begin{cases} \frac{\partial L_{\mathrm{f}}}{\partial D_1} = 0, \frac{\partial L_{\mathrm{f}}}{\partial D_2} = 0, \frac{\partial L_{\mathrm{f}}}{\partial \Phi} = 0 \\ \lambda \neq 0, \mu_1, \mu_2, \mu_3, \mu_4 \geq 0 \\ -\frac{(D_1-D_2)^2}{2} + 2(D_1+D_2)\Phi - 2\Phi^2 - p = 0 \\ \mu_1\left(\frac{D_1-D_2}{2} - \Phi\right) = 0, \mu_2\left(\Phi - \left(1 - \frac{D_1+D_2}{2}\right)\right) = 0, \mu_3\left(\frac{D_2-D_1}{2} - \Phi\right) = 0, \mu_4\left(\Phi - \frac{D_1+D_2}{2}\right) = 0 \\ \frac{D_1-D_2}{2} - \Phi \leq 0, \Phi - \left(1 - \frac{D_1+D_2}{2}\right) \leq 0, \frac{D_2-D_1}{2} - \Phi \leq 0, \mu_4\left(\Phi - \frac{D_1+D_2}{2}\right) \leq 0 \\ k > 1 \end{cases} \tag{3}$$

By solving (3), the optimal duty-cycle combination can be expressed as:

$$\begin{cases} D_1 = \sqrt{\frac{p}{2(k-1)}} \\ D_2 = k\sqrt{\frac{p}{2(k-1)}} \\ \Phi = \frac{1}{2}\sqrt{\frac{(k-1)p}{2}} \end{cases} \tag{4}$$

As shown in (4), for any given p and k, there always exists a set of corresponding D_1, D_2, and Φ values. Moreover, the intrinsic relationship among D_1, D_2, and Φ can be expressed as:

$$\begin{cases} \Phi = \frac{1}{2}(D_2 - D_1) \\ D_2 = kD_1 \end{cases} \tag{5}$$

Applying the same procedure to mode F yields the optimal duty-cycle combination, which is consistent with the results in (5). It is noteworthy that the optimal operating trajectory precisely resides at the boundary between mode E and mode F. Based on (5), the optimal trajectories for modes E and F are plotted.

As shown in Figure 4, the cyan plane represents the interface between mode E and mode F, and the red line illustrates the optimal path. Under optimal operating conditions, the transmitted power range is $[0, 2(k-1)/k^2]$. According to (4) and (5), the waveform under low-power operation with $k > 1$ is shown in Figure 5a, where only two switches achieve ZVS, and the remaining six switches operate under ZCS. Although ZCS mitigates turn-off losses, the lack of ZVS leads to the dissipation of energy stored in the output capacitance of the switches as heat. Consequently, it is essential to optimize the duty-cycle combinations to ensure ZVS for all switches while simultaneously minimizing the peak inductor current. While ZCS reduces turn-off losses, the absence of ZVS results in energy stored in the switch's output capacitance being dissipated as heat. Therefore, it is necessary to adjust the duty-cycle combinations to achieve ZVS for all switches while maintaining a low inductor current peak.

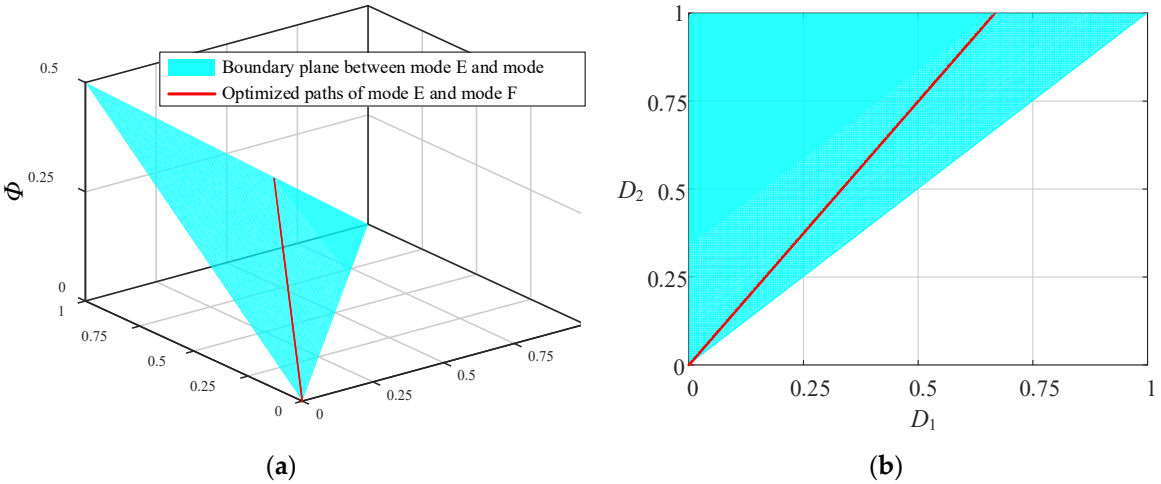


Figure 4. The optimized operating path in the low-power region for $k > 1$. (**a**) A three-dimensional visualization of the optimized path. (**b**) A two-dimensional projection of the optimized path.

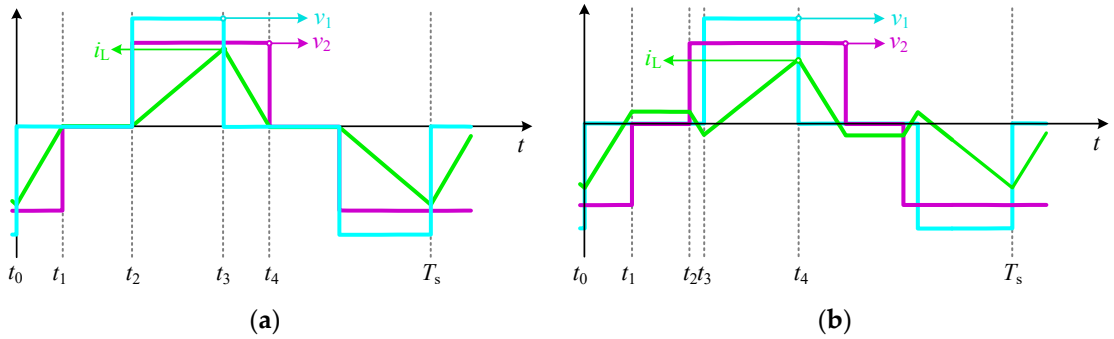


Figure 5. (**a**) Operating waveforms of mode E and mode F under minimum current-stress conditions. (**b**) Further optimized waveforms under low-power operation for $k > 1$.

As shown in Figure 5a, at t_1, the switch current is zero, leading to a ZVS failure for S_5. At t_2, the rising edges of v_1 and v_2 overlap, causing a ZVS conflict for switches S_4 and S_8. By modifying the relationship among D_1, D_2, and Φ to enter mode F, as shown in Figure 5b, and ensuring $i_L(t_2) > 0$ and $i_L(t_3) < 0$, ZVS can be achieved for all switches. Specifically, by imposing the condition $i_L(t_2) + i_L(t_3) = 0$, both current polarities and an appropriate current magnitude are ensured, enabling full ZVS operation. From this condition, the intrinsic relationship among D_1, D_2, and Φ can be derived as:

$$\Phi = (k - \frac{1}{2})D_1 - \frac{1}{2}D_2 \tag{6}$$

According to mode F constraints, it is known that $1 - kD_1 > 0$. Introducing a scaling factor λ $(0 < \lambda < 1)$ and setting $1 - D_2 = \lambda(1 - kD_1)$, the normalized inductor current $i_{Ln}(t_2)$ can be expressed as:

$$i_{Ln}(t_2) = (1 - \lambda)(1 - kD_1) \tag{7}$$

Therefore, it can be ensured that $i_L(t_2) > 0$ and $i_L(t_3) < 0$, enabling full ZVS for all switches. For mode F, when the transmitted power is positive, $i_L(t_0) < 0$ is always satisfied. As shown in Figure 6a, the ZVS region of mode F is defined by the planes $i_L(t_1) = i_L(t_2) = 0$ and $i_L(t_3) = 0$, as well as the coordinate planes, forming a closed volume. Different values of λ correspond to different optimization paths, all of which lie on the green surface, which itself is located within the ZVS region of mode F.

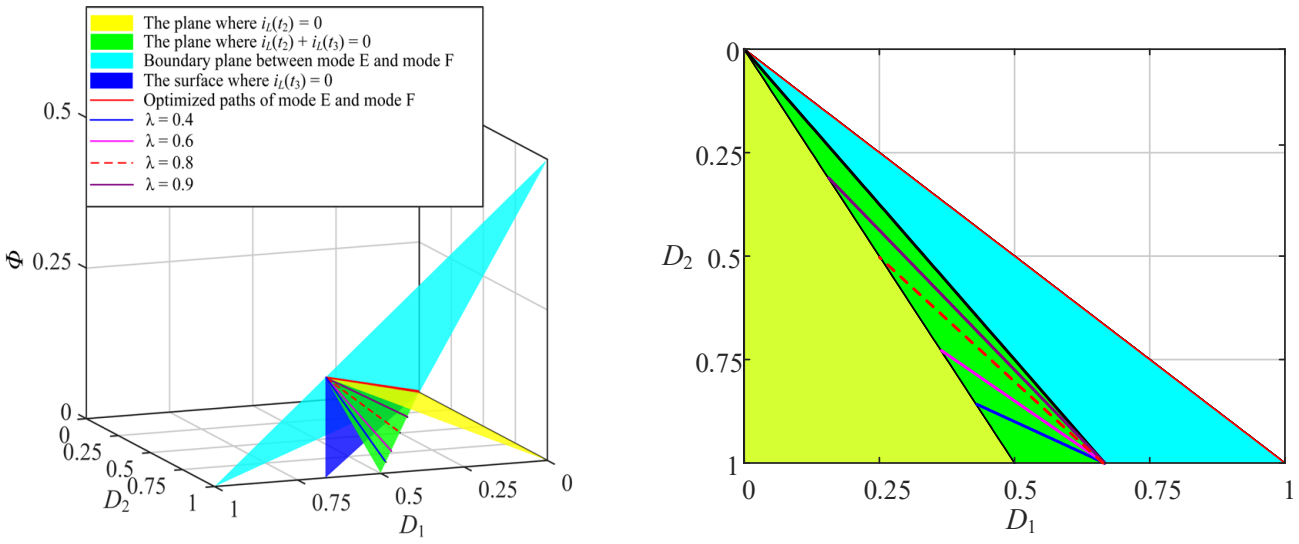


Figure 6. The further optimized operating path in the low-power region for $k > 1$. (**a**) A three-dimensional visualization of the optimized path. (**b**) A two-dimensional projection of the optimized path.

Figure 7 illustrates the relationships between the normalized transmitted power p, the normalized current stress i_{pn}, and the normalized inductor current $i_{Ln}(t_2)$ for different values of λ (0.4, 0.6, 0.8, and 0.9). As shown in Figure 7a, for different λ values, the maximum transmitted power of mode F remains constant at $[0, 2(k-1)/k^2]$. As λ increases, the current stress decreases. Conversely, as depicted in Figure 7b, for the same transmitted power, the inductor current $i_{Ln}(t_2)$ decreases with increasing λ. To ensure sufficient discharge of the parasitic capacitance of SiC MOSFETs, the inductor current $i_{Ln}(t_2)$ should retain a relatively high magnitude. Therefore, a slightly smaller λ value should be selected to maintain the required current magnitude. Considering the trade-off between current-stress minimization and the requirement to fully discharge the device capacitance, an appropriate value of λ should be selected based on the DAB converter's design parameters. This paper selects $\lambda = 0.8$ as the optimal value.

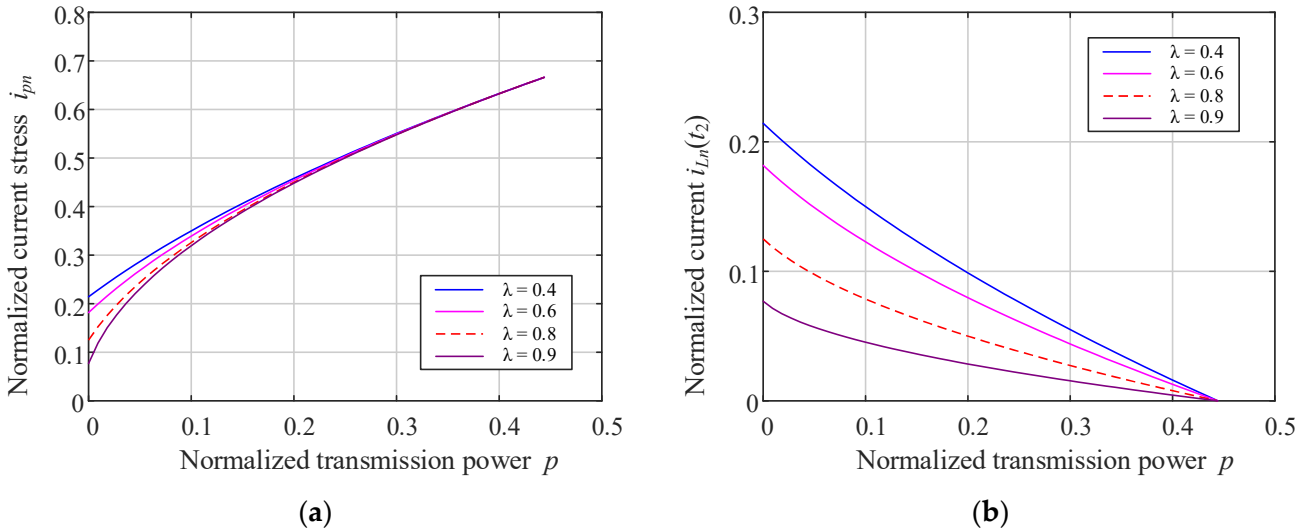


Figure 7. The effects of λ on the normalized current stress i_{pn} and the normalized inductor current $i_{Ln}(t_2)$ for mode F. (**a**) The relationship between i_{pn} and normalized transmitted power p. (**b**) The relationship between $iLn(t_2)$ and normalized transmitted power p.

The optimal duty-cycle combination for mode F is given by

$$\begin{cases} D_1 = \frac{1+\sqrt{1-50p+60kp}}{2(-5+6k)} \\ D_2 = \frac{1}{5}(1+4kD_1) \\ \Phi = \frac{1}{10}(-1+(6k-5)D_1) \end{cases} \tag{8}$$

3.2. Modulation Strategy in the Medium and High-Power Range When k > 1

Under medium and high-power operating conditions in the buck mode, mode D is selected as the backup optimized mode. By applying the same approach to solve mode D, the optimal duty-cycle combination is obtained as follows:

$$\begin{cases} D_1 = \sqrt{\frac{p}{2(k-1)}} \\ D_2 = k\sqrt{\frac{p}{2(k-1)}} \\ \Phi = \frac{1}{2}\sqrt{\frac{(k-1)p}{2}} \end{cases} \tag{9}$$

where the intrinsic relationship among D_1, D_2 and Φ can be expressed as:

$$\Phi = \frac{-2+D_1+k}{2(-1+k)} \tag{10}$$

For $k > 1$, in mode D, the conditions of $i_L(t_0) > 0$ and $i_L(t_2) < i_L(t_3)$ are always satisfied. Therefore, switches S_1 and S_2 can achieve ZVS, and after S_5 and S_6 achieve ZVS, S_7 and S_8 can also achieve ZVS. The ZVS conditions are defined as $i_L(t_1) < 0$ and $i_L(t_2) > 0$. As shown in Figure 8a, the ZVS region of mode D is enclosed by the planes $i_L(t_1) = 0$, $i_L(t_2) = 0$, as well as the coordinate planes, forming a closed space. The magenta curve represents the optimal trajectory of mode D, located entirely within the ZVS region. Under this optimized operation, the transmitted power range for mode D is $[2(k-1)/k^2, 1]$.

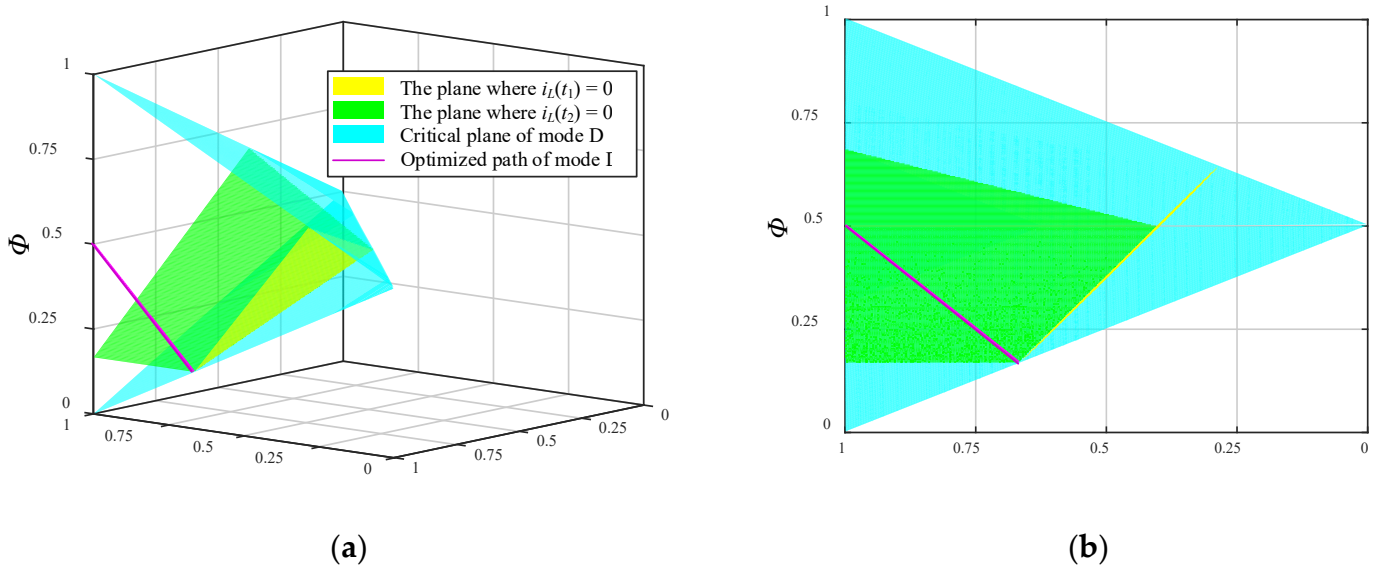


Figure 8. The optimized operating path in the medium and high-power region for $k > 1$. (**a**) A three-dimensional visualization of the optimized path. (**b**) A two-dimensional projection of the optimized path.

3.3. Modulation Strategy in the Low-Power Range When k < 1

Under boost-mode conditions in the operation of the DAB converter, modes E and G are selected as the optimal modulation strategies for low-power operation. These two

modes share the same optimal duty-cycle combination, as shown in (11). Based on (11), the intrinsic relationship among D_1, D_2, and Φ can be further derived, as expressed in (12). According to (12), the optimized trajectory lies on the interface between modes E and G. The corresponding waveforms of the optimized solution are shown in Figure 9a, where two switches achieve ZVS and the remaining six switches operate under ZCS conditions.

$$\begin{cases} D_1 = \sqrt{\frac{p}{2k(1-k)}} \\ D_2 = \sqrt{\frac{kp}{2(1-k)}} \\ \Phi = \frac{1}{2}\sqrt{\frac{p(1-k)}{2k}} \end{cases} \tag{11}$$

$$\begin{cases} D_2 = kD_1 \\ \Phi = \frac{D_1 - D_2}{2} \end{cases} \tag{12}$$

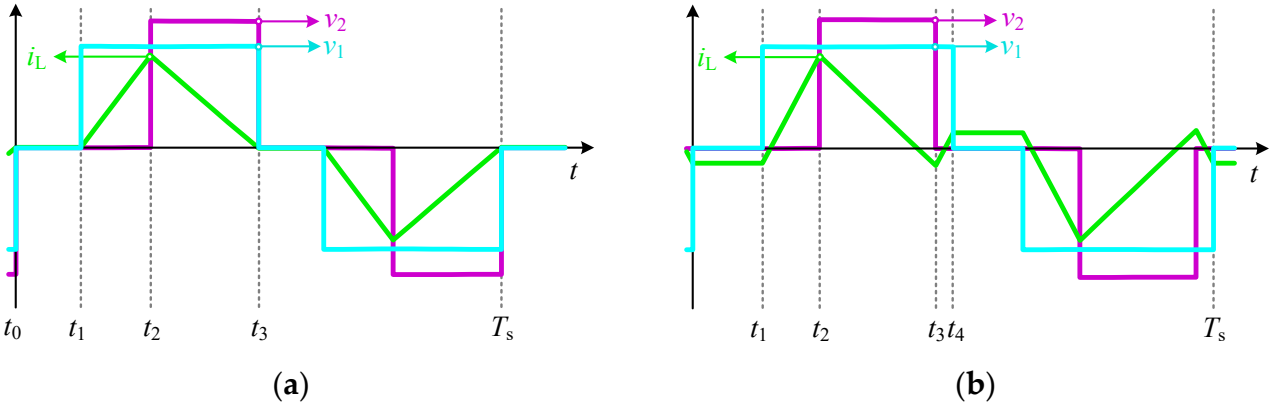


Figure 9. (**a**) Operating waveforms of mode E and mode G under minimum current-stress conditions. (**b**) Further optimized waveforms under low-power operation for $k < 1$.

As illustrated in Figure 9b, by adopting an optimization strategy analogous to that employed under low-power buck-mode operation, the ZVS failure can be effectively mitigated. This is achieved by appropriately tuning the control parameters D_1, D_2, and Φ while imposing the equality constraint $i_L(t_3) + i_L(t_4) = 0$, thereby ensuring soft-switching for all bridge switches under the boost mode. From this condition, the intrinsic relationship among D_1, D_2, and Φ can be derived as:

$$D_2(-2+k) + k(D_1 + 2\Phi) = 0 \tag{13}$$

Combining (13) with the boundary conditions for mode G, $k > D_2$ is derived. For $i_L(t_4) > 0$, by introducing the auxiliary factor λ ($0 < \lambda < 1$) and enforcing $1 - D_1 = \lambda(1 - D_2/k)$, the normalized inductor current can be expressed as:

$$i_{Ln}(t_4) = k(1-\lambda)(1-\frac{D_2}{k}) \tag{14}$$

As shown in Figure 10, the ZVS region of mode F is defined by the planes $i_L(t_3) = 0$ and $i_L(t_4) = 0$, as well as the coordinate planes. Different values of λ correspond to distinct optimized trajectories, all located on the green surface. The green surface lies entirely within the ZVS region of mode F.

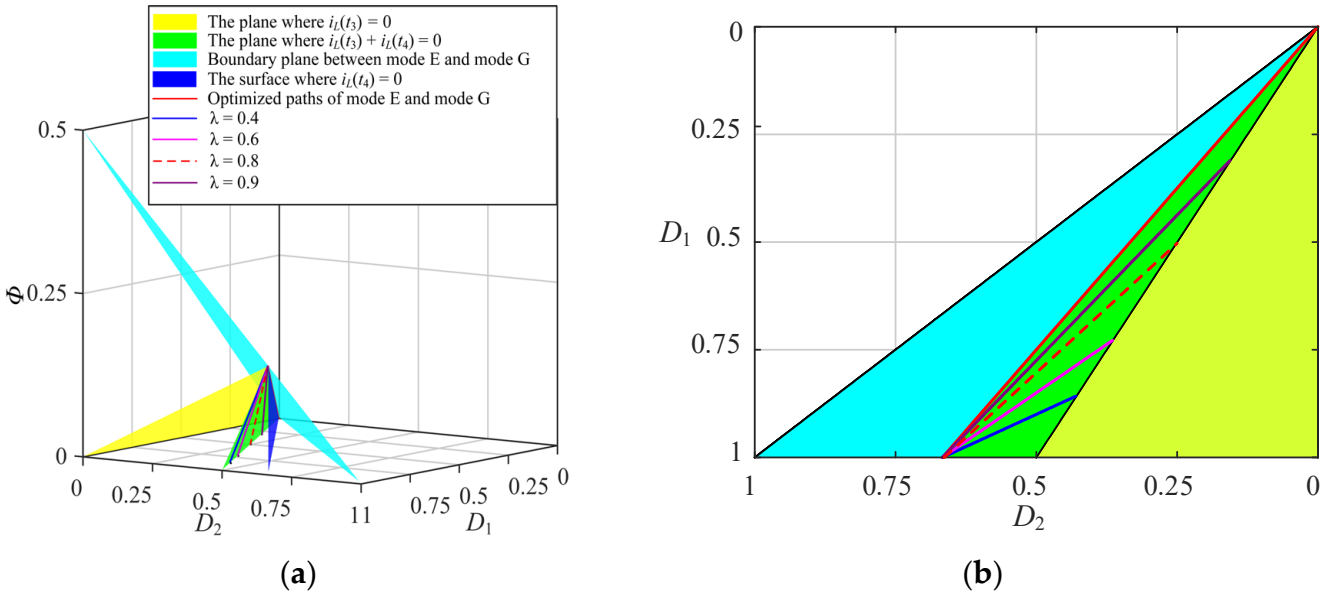


Figure 10. The optimized operating path in the low-power region for $k < 1$. (**a**) A three-dimensional visualization of the optimized path. (**b**) A two-dimensional projection of the optimized path.

Figure 11 illustrates the relationships between the normalized transmitted power p, the normalized current stress i_{pn}, and the normalized inductor current $i_{Ln}(t_2)$ for different values of λ (0.4, 0.6, 0.8, and 0.9). As shown in Figure 11, for different λ values, the maximum transmitted power of mode G remains constant at $[0, 2(k-1)/k^2]$. As shown in Figure 11a, as λ increases, the current stress decreases. Conversely, as depicted in Figure 7b, for the same transmitted power, the inductor current $i_{Ln}(t_2)$ decreases with increasing λ. To ensure sufficient discharge of the parasitic capacitance in SiC MOSFETs, $i_L(t_2)$ must maintain an appropriate value, and thus λ should be slightly lower. The specific value of λ should be determined by a comprehensive consideration of the DAB converter design parameters, balancing ZVS realization and current-stress reduction. In this study, λ = 0.8 is selected as the optimal choice.

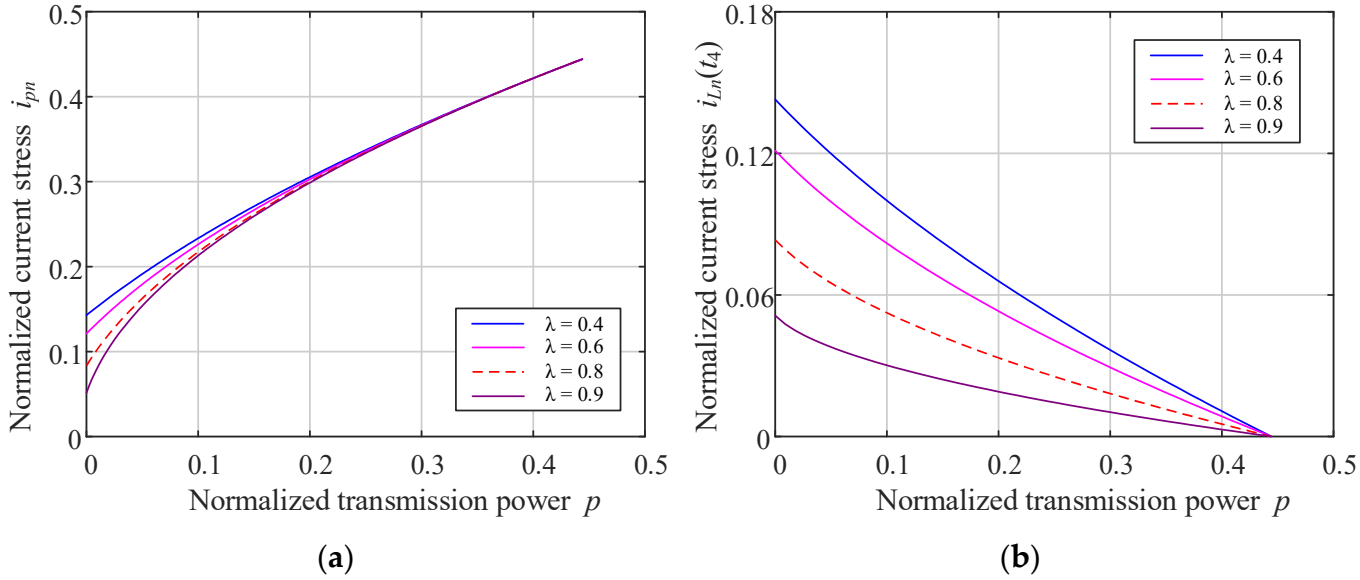


Figure 11. The effects of λ on the normalized current stress i_{pn} and the normalized inductor current $i_{Ln}(t_2)$ for mode G. (**a**) The relationship between i_{pn} and normalized transmitted power p. (**b**) The relationship between $i_{Ln}(t_2)$ and normalized transmitted power p.

The optimal duty-cycle combination for mode G is given as follows:

$$\begin{cases} D_1 = \frac{1}{5}\left(1 + \frac{4D_2}{k}\right) \\ D_2 = \frac{k+\sqrt{k(k+60p-50kp)}}{12-10k} \\ \Phi = \frac{1}{10}\left(-1 + D_2\left(-5 + \frac{6}{k}\right)\right) \end{cases} \tag{15}$$

3.4. Modulation Strategy in the Medium and High-Power Range When k < 1

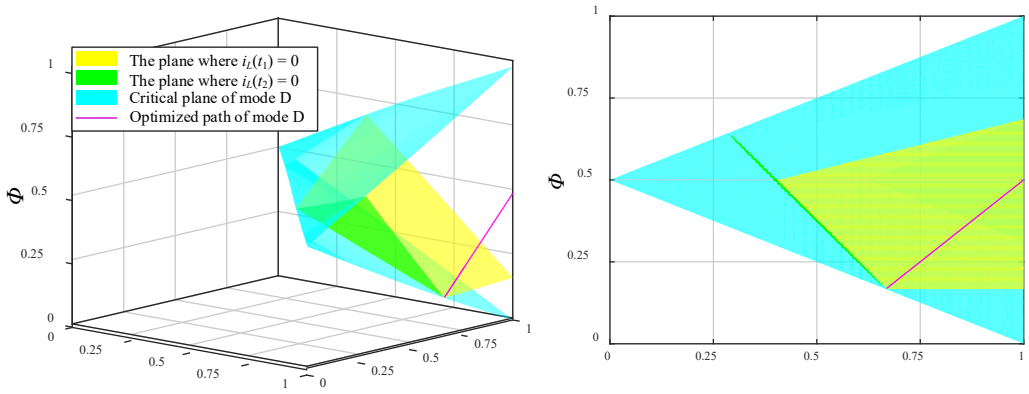
Under medium- and high-power conditions in the boost mode, mode D is identified as the optimal modulation strategy for achieving efficient operation. Applying the same solution approach, the optimal duty-cycle combination for mode D can be derived as follows:

$$\begin{cases} D_1 = 1 \\ D_2 = 1 - (k-1)\sqrt{\frac{1-P}{k^2-2k+2}} \\ \Phi = \frac{1}{2}\left(1 - k\sqrt{\frac{1-P}{2k^2-2k+1}}\right) \end{cases} \tag{16}$$

The intrinsic relationship among D_1, D_2, and Φ can be expressed as:

$$\Phi = \frac{1 + (-2 + D_2)k}{2(1-k)} \tag{17}$$

For $k < 1$, in mode D, the ZVS conditions are defined as $i_L(t_1) < 0$ and $i_L(t_2) > 0$. As shown in Figure 12, the ZVS region of mode D is enclosed by the planes $i_L(t_1) = 0$ and $i_L(t_2) = 0$, as well as the coordinate planes, forming a closed space. The magenta curve represents the optimal trajectory of mode D, located entirely within the ZVS region. Under these optimized operating conditions, the transmitted power range for mode D is [2k (1 − k),1].



(**a**) (**b**)

Figure 12. The optimized operating path in the medium and high-power region for $k < 1$. (**a**) A three-dimensional visualization of the optimized path. (**b**) A two-dimensional projection of the optimized path.

4. Simulation Comparison with Existing Schemes

A comprehensive comparison among SPS [15], CSO-DPS [37], OPCB-EPS [38], CSO-TPS [14], and the proposed EIOS-TPS is performed under identical operating conditions to validate the effectiveness of the proposed modulation strategy in enhancing the efficiency of the DAB converter. The ZVS range and current stress are quantitatively analyzed using MATLAB R2020a simulations based on the parameters summarized in Table 5.

Table 5. The parametric details of the experimental DAB converter setup.

Circuit Parameters	Specifications
Power	Input Voltage V_1 = 80 V Output Voltage V_2 = 53.33 V, 120 V Maximum Power P_{max} = 1176 W Switching Frequency f_s = 40 kHz Transformer Turns Ratio n = 1
	Inductor L = 25.5 µH
Switch	S_1–S_4, S_5–S_8: C3M0075120K V_{DSS} = 1200 V, I_D = 32 A, $R_{ds(on)}$ = 40 mΩ, C_{oss} = 58 pF
SiC MOSFET Drivers	1EDI60N12AF
Microcontroller	TMS320F28335
Filter Capacitor (C_1, C_2)	Input Capacitor C_1 = 450 µF Output Capacitor C_2 = 450 µF

4.1. Current Stress

Figure 13 compares the current-stress performance of the five modulation strategies under different voltage conversion ratios k and normalized transmitted power p. Figures 13a and 13b present the curves of normalized current stress i_{pn} versus normalized transmitted power p for k = 1.5 and k = 0.667, respectively. As shown in Figure 13, SPS exhibits the highest current stress under both buck and boost conditions, particularly at low transmitted power levels. The current-stress performance of OPCB-EPS and CSO-TPS is identical, as indicated by the cyan curve in the figure; therefore, only CSO-TPS is considered in subsequent analyses. Both CSO-DPS, CSO-TPS, and EIOS-TPS effectively reduce current stress. Under extremely low-power conditions ($p < 0.07$) the current-stress relationship is EIOS-TPS > CSO-DPS > CSO-TPS. In practice, a slight increase in current stress is expected to enable ZVS. For $0.07 < p < 1$, EIOS-TPS and CSO-TPS exhibit almost identical current stress, both lower than that of CSO-DPS. Overall, EIOS-TPS maintains lower current stress across most power ranges, except for slightly higher stress at extremely low transmitted power levels.

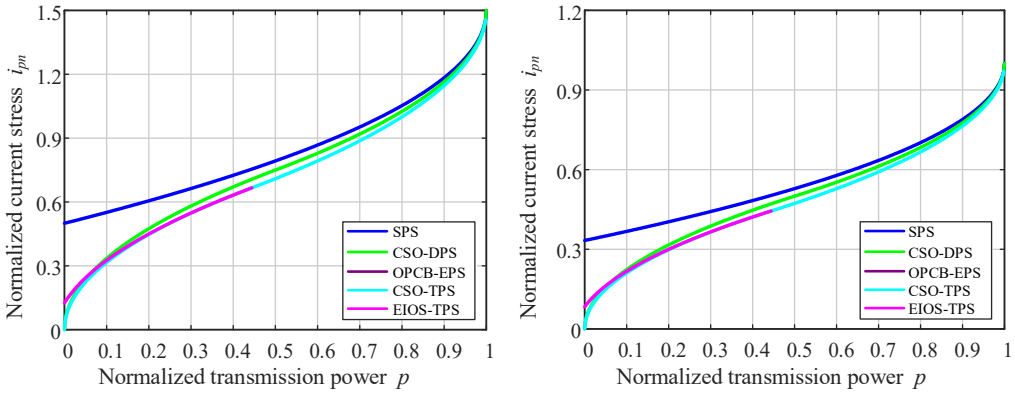


Figure 13. Curves of normalized current-stress variation with normalized power p for different voltage conversion ratios. (**a**) k = 1.5. (**b**) k = 0.667.

4.2. ZVS Range

Figure 14 illustrates the ZVS operating ranges of five modulation strategies: SPS, CSO-DPS, OPCB-EPS, CSO-TPS, and the proposed EIOS-TPS. The green region denotes the operating conditions under which all switches achieve ZVS, whereas the other colored regions indicate scenarios where ZVS is not attainable for certain switches. As shown in Figure 14, all four strategies exhibit a large ZVS failure region at low transmitted power levels; therefore, the analysis focuses on the low-power range. In boost mode,

switches S_1–S_4 cannot achieve ZVS. In buck mode, switches Q_1–Q_4 fail to achieve ZVS. This limitation is inherent to the SPS strategy, where all switches can achieve ZVS only when $k = 1$ (i.e., primary and secondary voltages are matched). For CSO-DPS and OPCB-EPS, switches Q_1–Q_2 cannot achieve ZVS in boost mode, and switches S_3–S_4 cannot achieve ZVS in buck mode. Notably, the ZVS range of CSO-DPS is narrower than that of OPCB-EPS. For CSO-TPS, six switches fail to achieve ZVS in both buck and boost modes, although they operate under ZCS conditions. In contrast, the proposed EIOS-TPS enables ZVS for all switches across the full power range under both buck and boost modes.

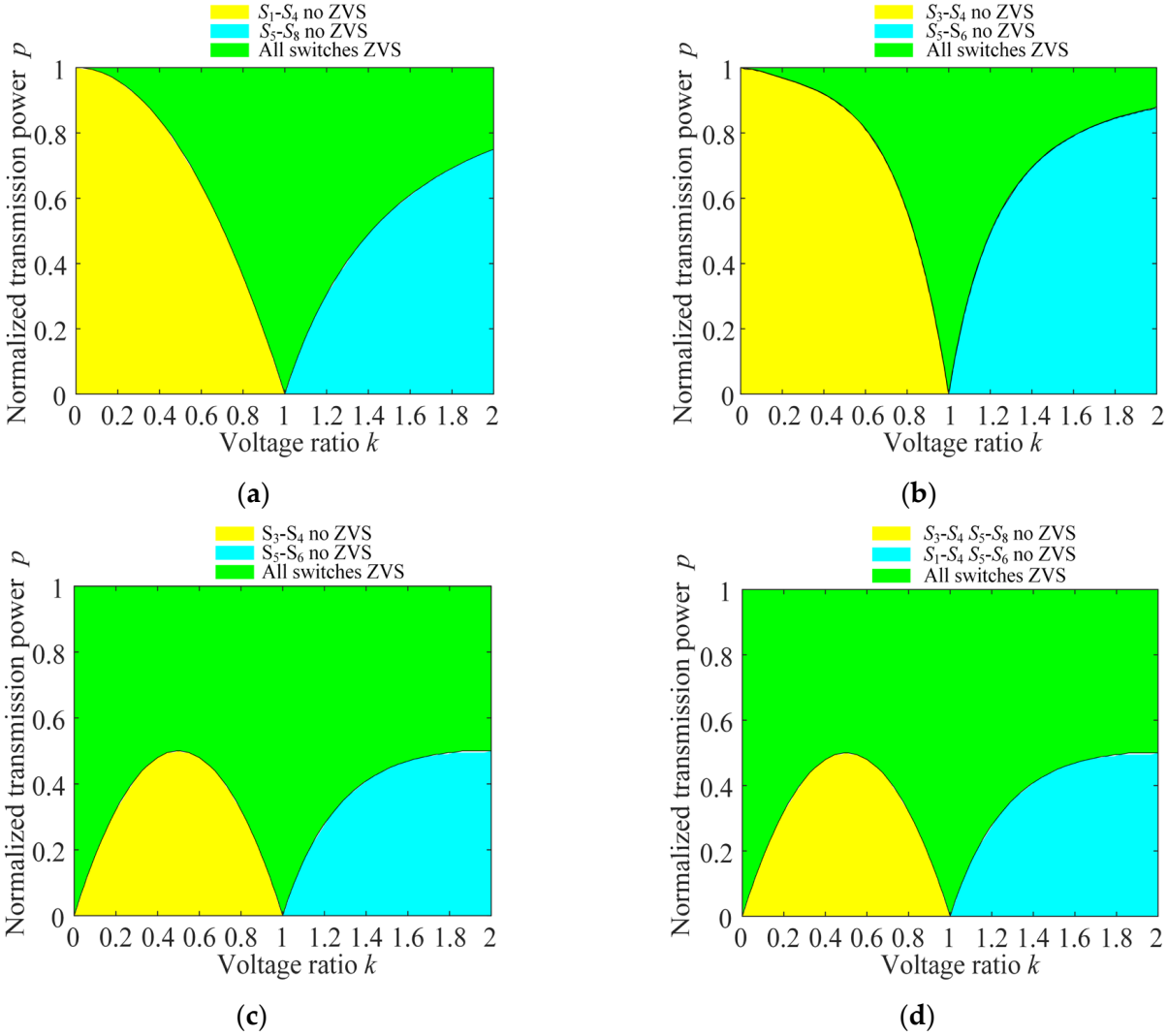


Figure 14. ZVS range of each scheme. (**a**) SPS. (**b**) CSO-EPS. (**c**) OPCB-EPS. (**d**) CSO-TPS.

The switching losses of the DAB converter significantly impact overall efficiency, particularly in the low-power operating region. Achieving ZVS for all switches at low power levels significantly enhances converter efficiency. The proposed modulation strategy enables ZVS for all switches across different voltage conversion ratios and the full power range, effectively reducing the DAB converter's switching losses.

5. Experimental Verification

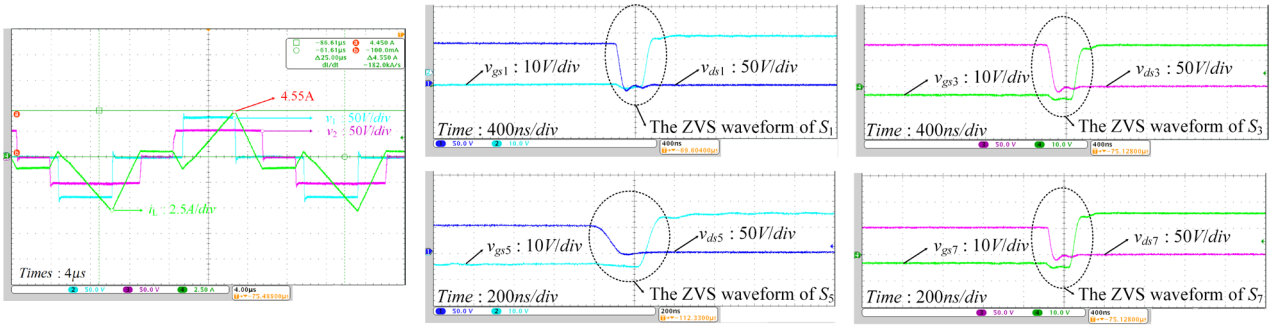
To evaluate the feasibility of the proposed control strategy, an experimental platform based on a DAB converter was constructed. The corresponding hardware configuration and technical parameters are detailed in Table 4. Furthermore, the IT6522C programmable

power supply from Tektronix was used to provide the DC input voltage, while an IT8830HS electronic load was employed to regulate various output power levels. To ensure the accurate measurement of experimental waveforms and related data. The voltage and current signals were measured using P5205A differential-type voltage probes and TCP0150 current probes from Tektronix, the converter efficiency was measured using Yokogawa WT500, and Tektronix MDO4034 was used for capturing real-time waveforms.

This section compares the current-stress characteristics of five modulation strategies: SPS, CSO-DPS, OPCB-EPS, CSO-TPS, and EIOS-TPS. The operating waveforms of EIOS-TPS under buck and boost modes at both low and high power levels are presented, along with their ZVS performance and efficiency comparisons.

5.1. Experimental Verification with k > 1

Figure 15 presents the experimental waveforms of the EIOS-TPS modulation strategy under a voltage conversion ratio of k = 1.5 (V_1 = 80 V, V_2 = 53.33 V). When the converter operates in mode F with an output power of 71 W, the transformer voltage and inductor current waveforms in Figure 15a closely match the theoretical analysis. The theoretical current stress is 4.8 A, while the measured value is 4.55 A, resulting in an error of less than 5.2%, thereby validating the accuracy of the theoretical model. Figure 15b illustrates the gate-source voltage v_{gs} and drain-source voltage v_{ds} of switches S_1, S_3, S_5, and S_7. The complementary switching pattern of each half-bridge exhibits symmetrical characteristics. The results confirm that the control system applies the gate signal v_{gs} only when the drain-source voltage v_{ds} naturally resonates to zero, ensuring ZVS for all switches in the DAB converter.



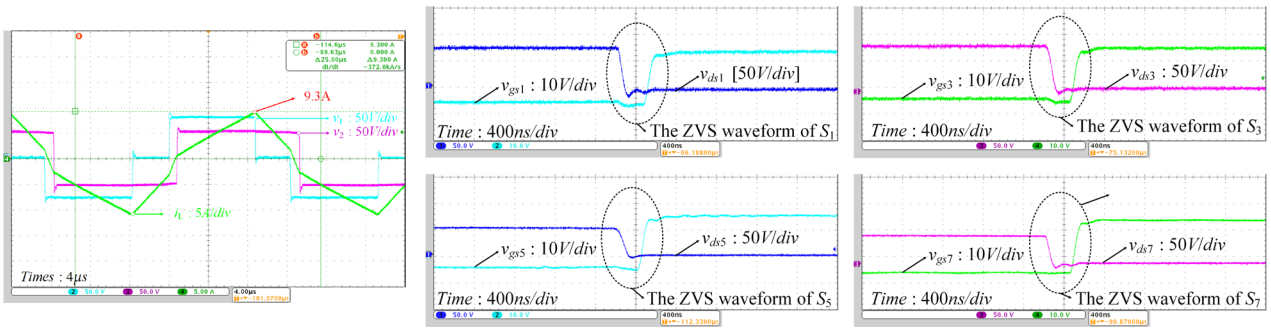
(**a**) (**b**)

Figure 15. Experimental waveforms of low power (71 W) by using EIOS-TPS when V_1 = 80 V and V_2 = 53.33 V. (**a**) Operation waveforms of the voltages and current. (**b**) Switching waveforms.

Figure 16 shows the experimental waveforms of the EIOS-TPS modulation strategy under the same voltage conversion ratio k = 1.5. When the converter operates in mode D with an output power of 313 W, the transformer voltage and inductor current waveforms in Figure 16a exhibit excellent agreement with theoretical predictions. The theoretical current stress is 10.3 A, while the measured value is 9.3 A. As shown in Figure 16b, all switches achieve ZVS.

Figure 17 shows the experimental current stress versus output power for SPS, CSO-DPS, CSO-TPS, and EIOS-TPS under a voltage conversion ratio of k = 1.5. At P = 71 W, the measured current stress for SPS, CSO-DPS, CSO-TPS, and EIOS-TPS is 7.4 A, 4.85 A, 4.65 A, and 4.55 A, respectively. The current stress of CSO-TPS and EIOS-TPS is nearly identical, while EIOS-TPS achieves a 38.5% reduction compared to SPS. At P = 313 W, the measured current stress for SPS, CSO-DPS, CSO-TPS, and EIOS-TPS is 11.5 A, 10.35 A, 9.2 A, and 9.3 A, respectively. EIOS-TPS exhibits comparable current stress to CSO-TPS, achieving

a 12.5% reduction compared to CSO-TPS and a 20% reduction compared to SPS. These results demonstrate the advantage of EIOS-TPS in reducing current stress when $k > 1$.



(**a**) (**b**)

Figure 16. Experimental waveforms of low power (313 W) by using EIOS-TPS when V_1 = 80 V and V_2 = 53.33 V. (**a**) Operation waveforms of the voltages and current. (**b**) Switching waveforms.

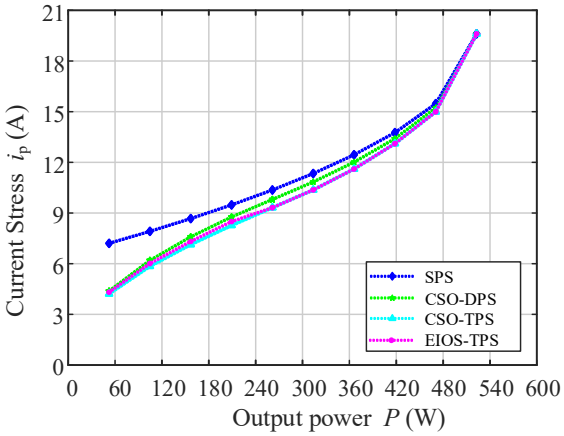
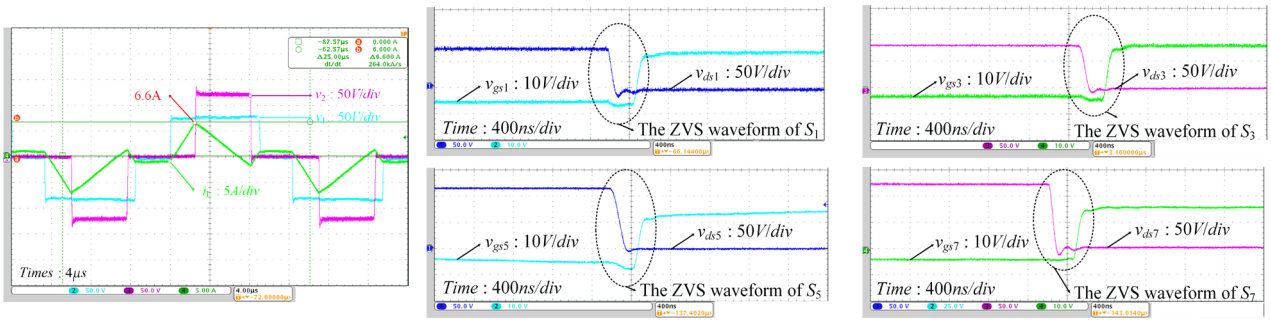


Figure 17. Current-stress variation with output power P when V_1 = 80 V and V_2 = 53.33 V.

5.2. Experimental Verification with k < 1

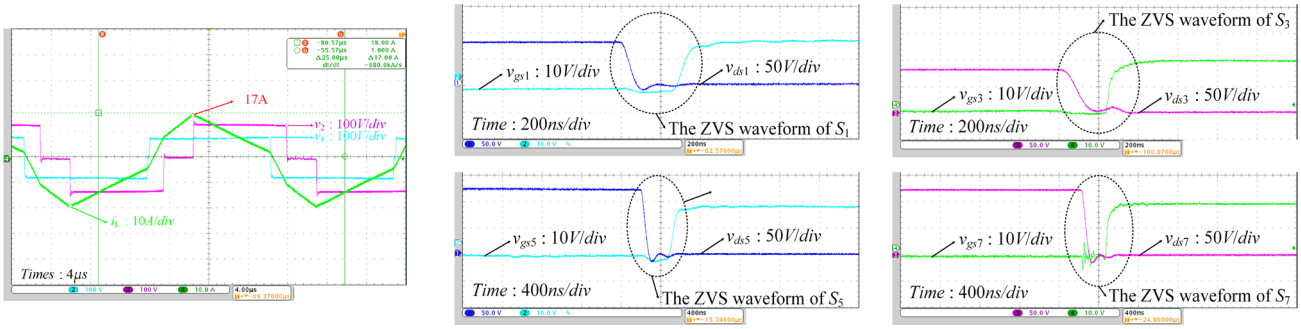
Figure 18 presents the experimental waveforms of the EIOS-TPS modulation strategy under a voltage conversion ratio of k = 1.5 (V_1 = 80 V ,V_2 = 120 V). When the converter operates in mode G with an output power of 160 W, the transformer voltage and inductor current waveforms in Figure 18a closely match theoretical predictions. The theoretical current stress is 7.3 A, while the measured value is 6.6 A. As shown in Figure 18b, all the switches in the DAB converter achieve ZVS.



(**a**) (**b**)

Figure 18. Experimental waveforms of low power (313 W) using EIOS-TPS when V_1 = 80 V and V_2 = 120 V. (**a**) The waveforms of the voltages and current during operation. (**b**) Switching waveforms.

Figure 19 presents the experimental waveforms of the EIOS-TPS modulation strategy under a voltage conversion ratio of k = 1.5 (V_1 = 80 V, V_2 = 120 V). When the converter operates in mode D with an output power of 1000 W, the transformer voltage and inductor current waveforms in Figure 19a closely match theoretical predictions. The theoretical current stress is 21 A, while the measured value is 20.2 A. As shown in Figure 19b, all switches in the DAB converter achieve ZVS.



(**a**) (**b**)

Figure 19. Experimental waveforms of high power (706 W) using EIOS-TPS when V_1 = 80 V and V_2 = 120 V. (**a**) The waveforms of the voltages and current during operation. (**b**) Switching waveforms.

Figure 20 shows the experimental current stress versus transmitted power for SPS, CSO-DPS, CSO-TPS, and EIOS-TPS under a voltage conversion ratio of k = 0.667. When the converter operates in mode D with an output power of 706 W, the measured current stress for SPS, CSO-DPS, CSO-TPS, and EIOS-TPS is 11.17 A, 7 A, 6.8 A, and 6.6 A, respectively. The current stress of CSO-TPS and EIOS-TPS is nearly identical, while EIOS-TPS achieves a 40.9% reduction compared to SPS. At P = 706 W, the measured current stress for SPS, CSO-DPS, CSO-TPS, and EIOS-TPS is 19 A, 18 A, 17.25 A, and 17 A, respectively. EIOS-TPS achieves a similar current stress to CSO-TPS, with a 10.5% reduction compared to SPS. These results confirm the advantage of EIOS-TPS in reducing current stress.

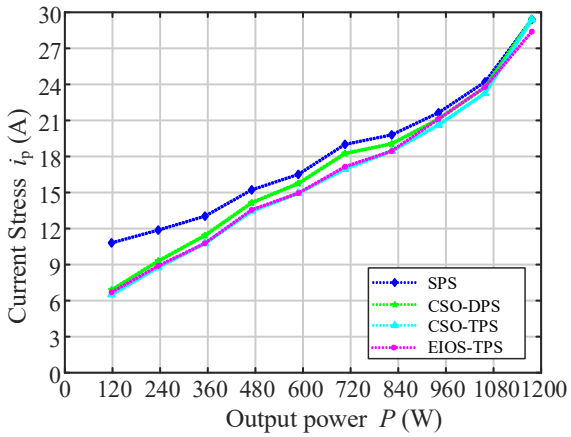


Figure 20. Current-stress variation with output power P when V_1 = 80 V and V_2 = 120 V.

5.3. Efficiency

Figure 21a and 21b show the efficiency curves in the buck (k = 1.5) and boost (k = 0.667) modes, respectively. The overall efficiency in boost mode is slightly higher than that in buck mode. At medium and high power levels, the efficiency ranking is EIOS-TPS = CSO-TPS > CSO-DPS > SPS. At low power levels, the ranking is EIOS-TPS > CSO-TPS > CSO-DPS > SPS. As shown in Figure 21, EIOS-TPS demonstrates a significant efficiency improvement over CSO-TPS, CSO-DPS, and SPS in the low-power region. The maximum efficiency

improvement of EIOS-TPS over the second-best strategy, CSO-TPS, is 2.2% in buck mode and 2% in boost mode, consistent with theoretical analysis. EIOS-TPS achieves ZVS and low current stress across the full load range, ensuring the highest efficiency in both buck and boost modes. In contrast, CSO-TPS exhibits ZCS issues under light-load conditions, leading to higher switching losses. Since switching losses dominate at low power levels in the DAB converter, the efficiency improvement of EIOS-TPS is particularly pronounced in this region.

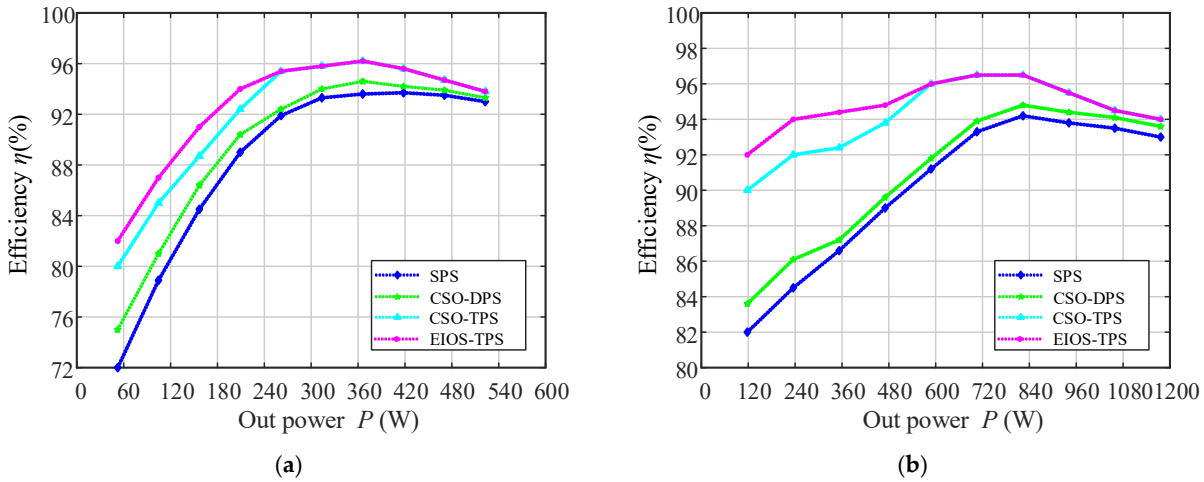


Figure 21. Experimentally measured efficiency curves for each modulation strategy. (**a**) $k > 1$. (**b**) $k < 1$.

6. Conclusions

Conventional single-degree-of-freedom (SPS), dual-degree-of-freedom (DPS, EPS), and triple-degree-of-freedom (TPS) modulation strategies cannot simultaneously achieve ZVS and low current stress, leading to reduced efficiency in DAB converters. To address this limitation, this paper proposes an enhanced integrated optimization strategy based on TPS (EIOS-TPS). The theoretical analysis and experimental results demonstrate that, by establishing an optimization path with a tunable λ parameter, EIOS-TPS dynamically balances current peak suppression and full-switch ZVS operation. This strategy extends the ZVS range across wide voltage-gain conditions (both buck and boost modes) while ensuring low current stress over the full power range. Furthermore, in high-frequency applications utilizing wide-bandgap semiconductors, EIOS-TPS effectively co-optimizes switching and conduction losses, providing significant efficiency improvements and offering a practical solution for high-power-density power electronic systems.

Author Contributions: Conceptualization, L.C.; Methodology, L.C.; Visualization, L.C.; Project Administration, Y.Z.; Validation, X.W.; writing—review and editing, D.Z. All authors have read and agreed to the published version of the manuscript.

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Conflicts of Interest: The authors declare no conflicts of interest.

Abbreviations

DAB	Dual-active bridge (converter)
ZVS	Zero-voltage switching
MCS	Minimizing current stress
EIOS-TPS	Enhanced Integrated Optimization Strategy based on triple phase shift
KKT	Karush–Kuhn–Tucker (conditions)
ZCS	Zero current switching
CSO	Current-stress optimization
RMSO	Root-mean-square current optimization
EB ZVS	Energy-based zero-voltage switching
CB ZVS	Current-based zero-voltage switching
QB ZVS	Charge-based zero-voltage switching
SPS	Single phase-shift modulation
DPS	Dual phase-shift modulation
EPS	Extended phase-shift modulation
TPS	Triple phase-shift modulation
LMM	Lagrange Multiplier Method
RL	Reinforcement learning
ANN	Artificial neural networks
AI	Artificial Intelligence
PSO	Particle swarm optimization
FIS	Fuzzy inference systems

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