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Fast State-of-Charge-Balancing Strategy for Distributed Energy Storage Units Interfacing with DC–DC Boost Converters

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Abstract: State-of-charge balance is vital for allowing multiple energy storage units (ESUs) to make the most of stored energy and ensure safe operation. Concerning scenarios wherein boost converters are used as the interfaces between ESUs and loads, this paper proposes a balancing strategy for realizing consistent state-of-charge (SoC) levels and equal currents among different ESUs. This strategy is valid for both parallel and series applications. Its advantages also include its high precision of SoC equalization without extra sensors and fast convergence. A common outer voltage loop is used to accomplish tight voltage regulation, while multiple inner current loops are utilized to achieve current control and SoC balance simultaneously. Firstly, by introducing SoC-based current distribution ratios (CDRs) to modify current references online, the currents are gradually adjusted to eliminate SoC deviations. Secondly, to expedite the balancing process, current saturations are further adopted. Thirdly, the influences of accelerating factor and current limits in CDR expressions are analyzed, and their selection guidelines are subsequently provided. Fourthly, the controller design, consisting of a dual loop, is illustrated to guarantee sufficient stability margins. Fifthly, an experimental platform consisting of three battery ESUs is developed to verify the proposed strategy.

Keywords: distributed energy storage unit (ESU); boost converter; state-of-charge (SoC) equalization; current balance; current saturation; fast convergence

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1. Introduction

Regarded as a key component of future power networks [1], a microgrid consists of renewable energy resources, energy storage systems (ESSs), and loads. Compared with AC microgrids, DC microgrids are superior in terms of efficiency, synchronization, and harmonics [2]. Thus, more and more attention is being paid to DC microgrids. The general configuration of a DC microgrid is shown in Figure 1. The inherent intermittency of renewable energy resources has negative effects on power quality and system stability. A battery ESS is usually used to mitigate this problem. It commonly contains an energy storage unit (ESU), a battery management system, and a power converter unit (PCU). Popular batteries used in microgrids are briefly described as follows: (1) Lead–acid batteries are cheap, but their specific energy is low. (2) Ni-Cd batteries have high power density and a long service life, but their memory effect is undesired, and they pollute the environment. (3) Ni-MH batteries are environmentally friendly and their self discharge is low, but their high price reduces their competitiveness. (4) Li-ion batteries have desired voltage platforms, long cycle life, and a wide temperature range, but technical protections are essential to prevent overuse. In fact, there exists a common issue for diverse batteries wherein the mismatches of internal impendence, self-discharge rate, and temperature cause imbalanced state-of-charge (SoC) levels in battery cells or ESUs. To fully use the rated capacities of batteries and prolong their lifetimes, effective solutions are needed for SoC equalization. So far, balancing topologies and balancing control strategies are the two categories of methods for eliminating SoC deviations.

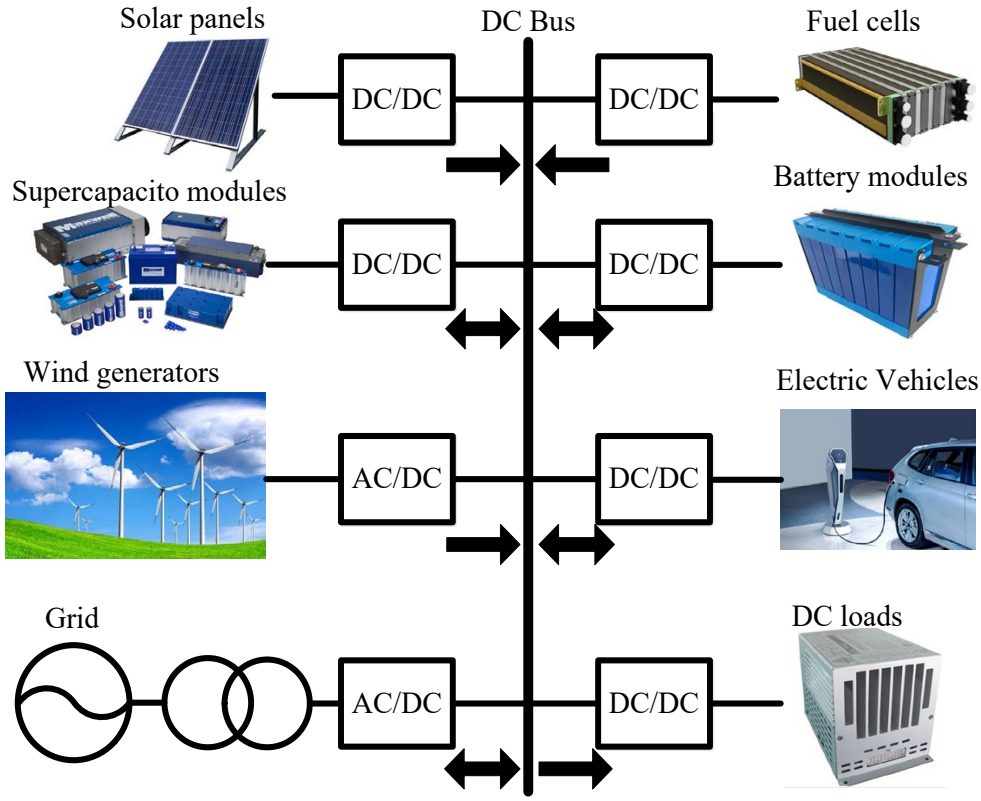


Figure 1. General configuration of a DC microgrid.

Balancing topologies mainly include the dissipative and non-dissipative types [3]. The former transfers excess energy to heat in power resistors. It is a simple approach, but it is only applicable to the charging process, and considerable energy losses are inevitable. The latter type adopts active balancing circuits to redistribute excess energy. Numerous balancing topologies with different virtues have been presented, such as multi-winding transformers [4], switched-capacitor circuits [5], LC resonant circuits [6] and non-inverting buck–boost circuits [7]. Favorable balancing results can be achieved, but the system costs increase.

As for the control algorithms used to realize a consistent SoC, there are two main kinds, namely, the centralized and decentralized types. To accomplish centralized control, a central controller [8,9] is employed to coordinate the sources, ESSs, and loads in real time. Nevertheless, potential single-point failures decrease system reliability [10].

Decentralized methods reduce dependence on communications and therefore enhance system reliability. As typical representatives of decentralized methods, plenty of SoC-based droop control schemes have been investigated. Due to virtual damping and inertia, the transient stability of dc-bus voltage was improved after a bidirectional dc-dc circuit was equivalently converted to an equivalent virtual dc machine in [11]. However, the line resistances and voltage drops were ignored, so the actual accuracy of SoC equalization deteriorated to some extent. In [12], SoC levels, line impedances, and virtual power ratings were all considered to achieve accurate power sharing. But five PI regulators were needed for each PCU, thus increasing implementation complexity. In [2], the droop coefficient was inversely proportional to the high-order term of the local SoC. Free from communications, power sharing and SoC balance were gradually obtained. Nevertheless, voltage deviation was inescapable, though it was constrained by choosing a proper exponent. Balancing speed is a vital index for balancing control. In [13], the adaptive virtual resistances were applied to flexibly adjust the power and status of ESUs for the rapid elimination of SoC errors. In [14], the relationship of the arctangent function is determined between droop coefficients and the individual SoC for faster SoC balancing. However, the overall scheme

involves multiple control loops, and this is quite inconvenient for controller design. In [10], the reference voltage and virtual impedance were devised as two piecewise functions of local SoC so that coordinated operation could be achieved between ESSs and the utility grid. Moreover, *I-V* SoC-based droop approaches have also been applied to inner current loops for better dynamic response [15,16]. Deriving from inverse droop, the balancing method in [17] adaptively modifies the reference voltage by adjusting the frequency–power curve. But power losses are also neglected for SoC estimation. Through sparse communication, three-layer hierarchical control schemes [18,19] have been presented to cope with the issues of bus voltage deviation and inconsistent line resistances. But additional balancing factors [18] or control loops [19] require an elaborate design to ensure system stability.

Some active balancing strategies are also used to achieve SoC consistency. For hybrid ESSs with different parameters, the event-triggered control theory was used to acquire balanced SoC levels in [20]. But complex principles may cause inconvenience for engineering applications. Based on the remaining energy of all batteries and the output signal of the voltage loop, a common time reference was produced to indirectly change the individual reference currents for an equal SoC in [21]. For modular multilevel ESSs, SoC balance was accomplished by directly adjusting the reference currents of inner loops in [22]. But large-signal stability analysis should also be provided for proper controller design because the supercapacitor voltages decrease obviously during the balancing process. For output-series hybrid ESSs, the cooperative control of a three-port converter was studied in [23]. The problems of imbalanced SoC and voltages are addressed, while excellent transient performance cannot be guaranteed in the absence of an inner current loop.

A simple structure, high efficiency, and boosted output voltage are the main virtues of dc-dc boost converters, leading to their extensive applications in microgrids. Based on interfacing boost converters, the novel contributions of this article are summarized as follows:

(1) A SoC-balancing strategy based on the current distribution ratio (CDR) is presented for multiple ESUs interfacing with boost converters by adjusting the reference currents.
(2) Current saturation is used to shorten the SoC equalization time by fully utilizing the current capability and enabling a large accelerating factor. The impacts of current limits and the accelerating factor are analyzed, and their selection rules are provided.
(3) The controller design is given to guarantee sufficient margins during discharge.
(4) The adaptive current limits that vary in proportion to the sum current are utilized for series applications to prevent unexpected step reference currents under conditions of load change.

Comparisons with representational balancing methods are listed in Table 1. The main advantages of this strategy are described below:

(1) *High Precision of SoC Equalization without Extra Sensors*: In boost converters, the inductor current is also the ESU current. Instead of approximate estimation, these two currents are precisely measured by a single current sensor in each PCU. Then, the real-time SoC can be directly calculated after the initial SoC is determined. This makes the proposed strategy a cost-effective solution for accurate SoC equalization.
(2) *Applicability for Parallel and Series Scenarios*: In parallel scenarios, this strategy distributes the load current to mitigate SoC deviations. In series scenarios, it regulates individual voltage gains for SoC consistency while the sum voltage is unchanged.
(3) *Accelerated Balancing Process*: The current capacity of the converter is fully exploited by introducing saturation. Thus, high current deviations are maintained for a long time, and this leads to the fast elimination of SoC differences. Moreover, the large accelerating factor in the approaching law is enabled by saturation, and high convergence speed is thereupon activated after some ESUs cease being saturated.

Table 1. Comparisons with the existing balancing methods.

Balancing Method	Suitable Application	Style of SoC Estimation	Accuracy of SoC Estimation	Number of Voltage Sensors	Number of Current Sensors	Total Number of Sensors	Sensor Cost
[1]	parallel	calculation	High	m	$2m$	$3m$	High
[2]	parallel	approximation	Not high	$2m$	$2m$	$4m$	High
[10]	parallel	approximation	Not high	m	m	$2m$	High
[15]	series	calculation	High	1	$m+1$	$m+2$	Not high
[17]	series	approximation	Not high	m	$2m$	$3m$	High
[22]	series	approximation	Not high	$m+1$	1	$m+2$	Not high
proposed	both	calculation	High	1	m	$m+1$	Low

m is the number of ESUs (or PCUs).

2. Proposed SoC-Balancing Strategy without Saturation

Usually, an ESU consists of some cells connected in series or parallel. To remove the potential SoC differences among ESUs, a SoC-balancing strategy based on the CDR is presented in this paper. Note that the SoC balance among battery cells is not the concern of this paper.

2.1. Basic Principle of SoC-Balancing Strategy

If boost converters function as the interfaces between distributed ESUs and loads, they are actually independent of the input side and parallel (or series) circuit connected on the output side. Owing to this feature, the individual SoC can be regulated by its own PCU. The corresponding configuration is outlined in Figure 2, where the ESUs are batteries. Inductor L_k, power switch S_k and diode D_k constitute the PCU#k, where $k = 1, 2, \ldots, m$. Capacitor C and load R are shared by the PCUs on the output side. The input voltage of PCU#k is denoted as u_{ik}. Moreover, u_{dc} and i_{o} are the dc-bus voltage and load current, respectively.

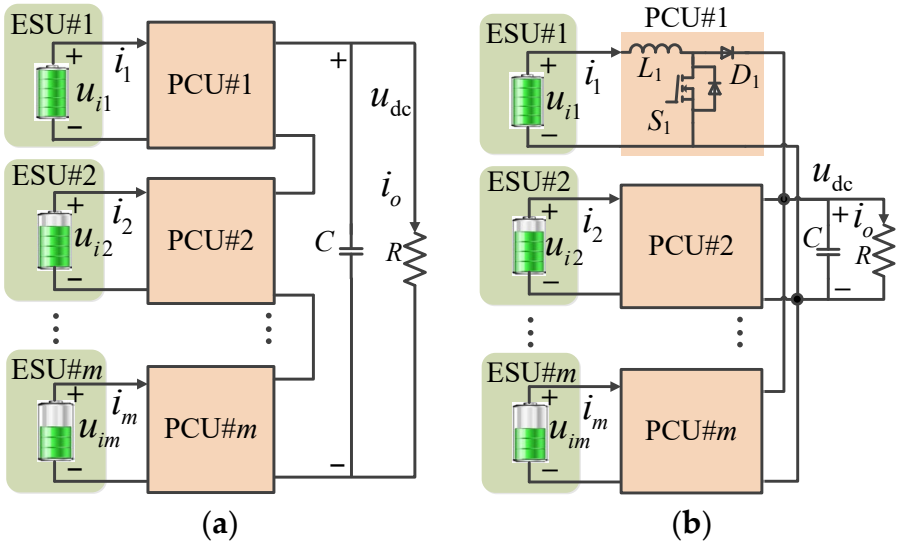


Figure 2. Configuration of the distributed battery ESUs interfaced with boost converters: (**a**) Series application; (**b**) parallel application.

As seen in Figure 3, dual-loop control is used to coordinate multiple units. A common outer loop is used for voltage regulation, while multiple inner loops are used for current control and SoC equalization. Here, $i_{\mathrm{r}k}$, i_k, d_k, and CDR_k are reference current, feedback current, duty cycle, and the current distribution ratio of the PCU#k, respectively.

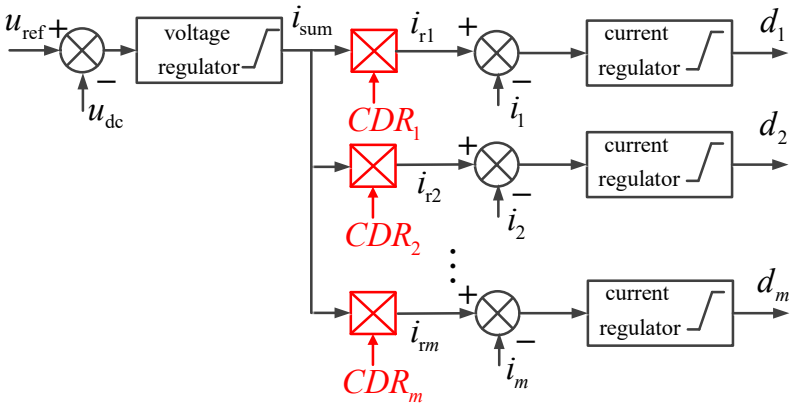


Figure 3. Schematic diagram of the proposed SoC-balancing strategy.

The parallel form helps to enhance system capacity, while the series form enables applications at higher voltage levels. In terms of discharge, the proposed method is valid for both parallel and series applications. When the PCUs are paralleled on the output side, u_{dc} is constant, and thus the load current can be reasonably distributed by CDRs according to the individual SoC level. When the PCUs are connected in series, the load current is unchanged and shared by all units. Then, the individual output voltages can be flexibly regulated while u_{dc} is fixed. In fact, the individual voltage gains are modified little by little, and the phase currents thereupon vary towards a consistent SoC status. To fulfill this strategy, the CDRs are introduced, which are expressed as

$$CDR_k = \frac{SoC_k^n}{\sum_{k=1}^{m} SoC_k^n}, k = 1, 2, \cdots, m \tag{1}$$

where n is an accelerating factor used to shorten the SoC-balancing duration. The output of the voltage regulator is the common input of all the current loops and acts as the reference of the sum current i_{sum}. The product of i_{sum} and CDR_k is the current reference of PCU#k, which is expressed as

$$i_{rk} = i_{sum} \times CDR_k \tag{2}$$

Then, the error between reference and feedback is processed by the current regulator to produce the duty cycle of each PCU. Thus, we can adjust the current distribution according to the relative value of the SoC so that individual states of charge are forced to be identical. On the one hand, lower current is anticipated for the ESU with a lower SoC to slow down the SoC decrease. On the other hand, a higher current is expected for the ESU with a higher SoC in order to expedite the SoC decrease. If these conditions are met, the SoC deviations will gradually be reduced, and the same SoC level will eventually be shared by all the ESUs. In the meantime, the currents of different PCUs become closer and closer. Furthermore, current sharing is achieved once a consistent SoC is obtained, according to Figure 3.

2.2. Estimation of SoC

SoC estimation is expressed as

$$SoC_k = SoC_{k0} - \frac{\int i_k dt}{Q}, k = 1, 2, \cdots, m \tag{3}$$

where Q is the rated capacity of the ESU and SoC_{k0} is the initial SoC level of ESU#k. To make the best of the coulomb-counting method and the open-circuited voltage (OCV) method [24], a joint method is used here to estimate SoC. The latter is used to obtain the initial SoC, while the former is employed to calculate the depth of discharge.

In this paper, the ESUs are lead–acid batteries, and the rated voltage is 12 V. Based on actual data, the characteristic curve of OCV versus SoC is plotted in Figure 4. Using the polynomial style to perform curve fitting, the relationship can be formulated as follows:

$$OCV = 0.5692 \times SoC^3 - 1.14 \times SoC^2 + 1.765 \times SoC + 11.11 \quad (4)$$

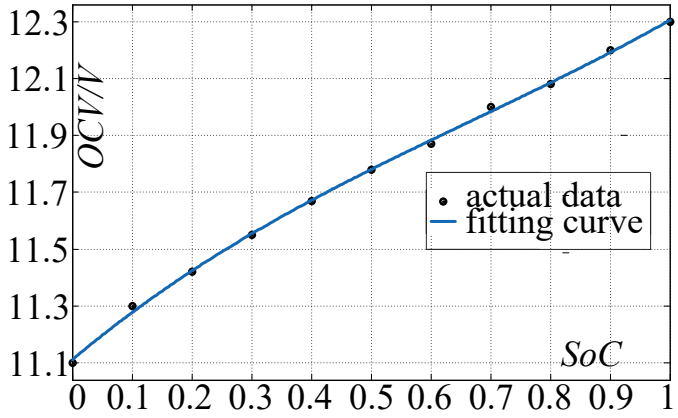


Figure 4. Curve of OCV versus SoC.

2.3. Selection of the Accelerating Factor in CDRs

To be convenient and general, m is set as 3 in this paper. Then, the value of n is discussed in detail. At first, n should be a positive integer to reduce the computing burden of the microprocessors. Assuming that each phase current can follow its reference immediately, this is an ideal case. Combining Equations (1)–(3), the ideal curves with the proposed strategy in parallel applications are plotted in Figure 5 when i_{sum} remains constant. The system parameters are given in Table 2. Under the same conditions, n mainly affects the balancing time and initial current distribution. If a higher value of n is used, the required time to realize SoC consistency is shorter, but the ESU with a higher SoC releases a higher current, and this threatens the safe operation of the relevant unit. For the shortest balancing time, it is essential to confirm the maximum n. Its selection process is described as follows.

Table 2. Key system parameters.

Parameters	Symbol	Value
Switching frequency	f_s	20 kHz
Inductance	L_1, L_2, L_3	4 mH
Capacitance	C	2200 uF
Load current	i_o	20 A (parallel) 6 A (series)
DC-bus voltage	u_{dc}	30 V (parallel) 90 V (series)
Initial SoC	SoC_{10}; SoC_{20}; SoC_{30}	0.9; 0.8; 0.7
Battery capacity	Q	45 Ah
Magnitude of carrier waves	A_m	37,500
Proportional gain of voltage loop	k_{pv}	0.5
Integral gain of voltage loop	k_{iv}	5
Proportional gain of current loop	k_{pi}	1000
Integral gain of current loop	k_{ii}	10,000

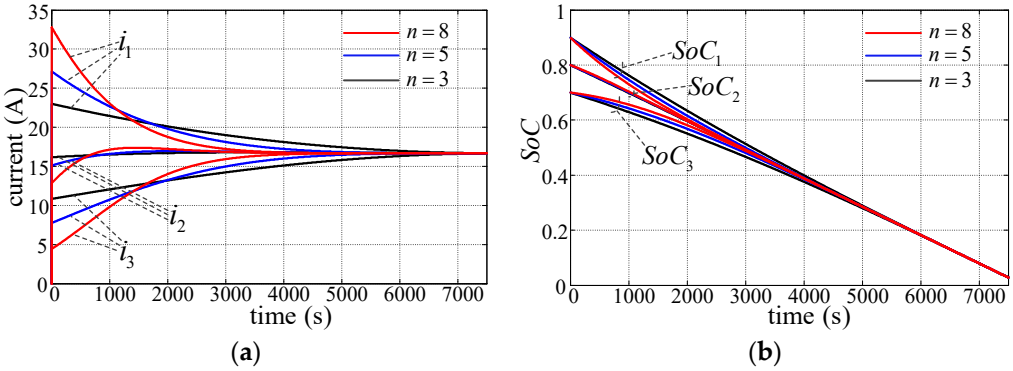


Figure 5. Ideal curves without saturation using different accelerating factors: (**a**) Current; (**b**) SoC.

In parallel scenarios, the upper limitation of n is governed by i_{allow}, the maximum allowable current of the PCU. For our testing platform, the allowable currents of the power switch, battery, and inductor are 120 A, 450 A, and 40 A, respectively. Thus, i_{allow} is set as 40 A to ensure the safe operation of the overall system. Then, n should satisfy the following inequality:

$$\frac{\max(SoC_{k0}^{n})}{\sum_{k=1}^{m} SoC_{k0}^{n}} \times i_{\text{sum}} \times (1+\eta) < i_{\text{allow}} \tag{5}$$

where max( ) is the maximum function. Positive η is a margin coefficient used to prevent overcurrent in real applications. Here, the actual upper limit of the current $i_{\text{allow}}/(1+\eta)$ is denoted as i_{satu}. According to Figure 5, the highest peak current appears at the initial stage of discharge. Then, i_{sum} can be roughly estimated according to energy conservation. Here, i_{sum} is 50 A, and η = 0.2. Consequently, i_{satu} is 33 A, and the maximum n is 8.

As for series scenarios, the load current in a boost converter also serves as the lower limit of the phase currents, i_{satl}. Thus, both i_{satu} and i_{satl} should be considered to achieve a maximum n. In a system with three units, it is evident that $3i_{\text{satl}} \le i_{\text{sum}} \le 3i_{\text{satu}}$. Besides Inequation (5), the following restriction also needs to be fulfilled, which is expressed as

$$i_{\text{sum}} \times \frac{\min(SoC_{k0}^{n})}{\sum_{k=1}^{m} SoC_{k0}^{n}} \ge i_{\text{satl}} \tag{6}$$

where min( ) is the minimum function. Combing Inequation (6) with Inequation (5), the maximum n is 5 when i_{sum} = 45 A and i_{satl} = 6 A. Due to the similarity of the ideal curves in the two applications, the corresponding curves in series applications are omitted.

3. Enhanced SoC-Balancing Strategy with Saturation

In the strategy in Section 2, the high current deviations only last for a short time. While the discharge process continues, the SoC differences become low, and then the approaching speed decreases rapidly. Although this strategy is brief and clear, it sacrifices more time to reach the balanced point. To accelerate the balancing process, current saturations are further utilized to enhance the aforementioned strategy.

For parallel scenarios, the preprocessed current reference is set as i_{satu} if it exceeds i_{satu}. Moreover, the rest of i_{sum} is redistributed by the other unsaturated units according to their own SoC levels. As the equalization process continues, the units with a higher SoC will desaturate one by one. As for series scenarios, i_o provides an inherent lower limit for the phase currents in boost converters. Therefore, i_k is increased to i_{satl} if it is lower than i_{satl}.

This improved strategy enables the usage of a larger n. During the initial stage, the high current deviations are maintained for a longer duration, so the eliminating rate of SoC deviations is high. When the ESUs are no longer saturated, a larger n leads to a faster balancing process that resembles a power function. In view of these two factors, current saturations can expedite the entire balancing process.

3.1. Expressions of CDRs

Above all, we assume that $SoC_{10} > SoC_{20} > SoC_{30}$. Moreover, some intermediate variables are needed, and they are defined as follows:

$$\begin{cases} CDR_{11} = SoC_1^n / \left(SoC_1^n + SoC_2^n + SoC_3^n\right) \\ CDR_{12} = SoC_2^n / \left(SoC_1^n + SoC_2^n + SoC_3^n\right) \\ CDR_{13} = SoC_3^n / \left(SoC_1^n + SoC_2^n + SoC_3^n\right) \\ CDR_{22} = \left(1 - i_{\text{satu}}/i_{\text{sum}}\right) \times SoC_2^n / \left(SoC_2^n + SoC_3^n\right) \\ CDR_{23} = \left(1 - i_{\text{satu}}/i_{\text{sum}}\right) \times SoC_3^n / \left(SoC_2^n + SoC_3^n\right) \\ CDR_{31} = \left(1 - i_{\text{satl}}/i_{\text{sum}}\right) \times SoC_1^n / \left(SoC_1^n + SoC_2^n\right) \\ CDR_{32} = \left(1 - i_{\text{satl}}/i_{\text{sum}}\right) \times SoC_2^n / \left(SoC_1^n + SoC_2^n\right) \end{cases} \tag{7}$$

Figure 6a gives the flow path used to assign CDRs in series applications, and it is performed once in each control period. Detailed expressions of CDRs are listed in Table 3. Here, g and h are the unit amounts at the upper and lower saturations. The main workflow is summarized in three steps. Firstly, the judging conditions are used to confirm the values of g and h. Secondly, the current distributions of all the units are kept within an allowable range again. Finally, the CDRs are assigned according to the specific case. The assigning task in parallel applications is shown in Figure 6b. Compared with that in series applications, it is regarded as a simplified version, setting $i_{\text{satl}} = 0$ and $h = 0$. In fact, its expressions of CDRs correspond to the first three cases in Table 3.

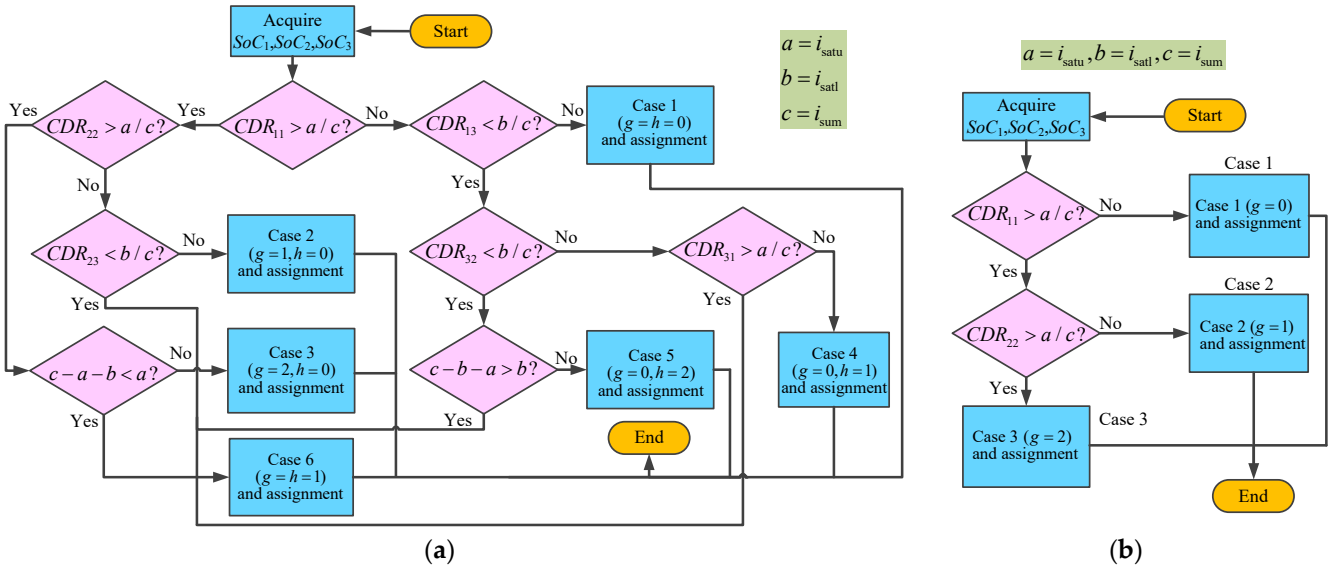


Figure 6. Flowchart of CDR assignment: (**a**) series application; (**b**) parallel application.

Table 3. Expressions of CDRs with saturation.

Case	g	h	CDR_1	CDR_2	CDR_3
1	0	0	CDR_{11}	CDR_{12}	CDR_{13}
2	1	0	$i_{\text{satu}}/i_{\text{sum}}$	CDR_{22}	CDR_{23}
3	2	0	$i_{\text{satu}}/i_{\text{sum}}$	$i_{\text{satu}}/i_{\text{sum}}$	$1 - 2i_{\text{satu}}/i_{\text{sum}}$
4	0	1	CDR_{31}	CDR_{32}	$i_{\text{satl}}/i_{\text{sum}}$
5	0	2	$1 - 2i_{\text{satl}}/i_{\text{sum}}$	$i_{\text{satl}}/i_{\text{sum}}$	$i_{\text{satl}}/i_{\text{sum}}$
6	1	1	$i_{\text{satu}}/i_{\text{sum}}$	$1 - (i_{\text{satu}} + i_{\text{satl}})/i_{\text{sum}}$	$i_{\text{satl}}/i_{\text{sum}}$

3.2. Selection of the Accelerating Factor in CDRs

With an increasing n, the related execution time of CDR calculation is prolonged. As the duration required to execute entire program in the microprocessors must be shorter than the control period, n cannot be too large. This is indicated by

$$t_{\text{else}} + n \times t_{\text{mul}} < t_{\text{ctrl}} \tag{8}$$

where t_{mul} is the required time of a single multiplication and t_{else} is the rest time of the whole program. Moreover, t_{ctrl} is the control period; here, it is equal to the switching period. The closed-loop control and data communications are accomplished using DSP28335 chips. The power function can be used to calculate high-order terms of SoC, but it takes much more time than continuous multiplication. Thus, continuous multiplication was utilized to reduce the execution time. Based on Inequation (8), the maximum n is confirmed.

Under the enhanced strategy, the minimum n for parallel applications should make $g \geq 1$ so that the current capacity of the converter is fully utilized. If $i_{\text{sum}} - i_{\text{satu}} < i_{\text{satu}}$, that is, $i_{\text{sum}} < 2i_{\text{satu}}$, the following requirement should be satisfied:

$$\frac{\max(SoC_{k0}^{n})}{\sum_{k=1}^{m} SoC_{k0}^{n}} \times i_{\text{sum}} > i_{\text{satu}} \tag{9}$$

The ESU current with lowest SoC_{k0} decreases when n increases. But it cannot be lower than the least significant current (LSC), which is decided by the range of current sensor and the bit number of analog-to-digital converter in microprocessors. The maximum n should correspond to the following:

$$(i_{\text{sum}} - i_{\text{satu}}) \times \frac{SoC_3^n}{SoC_2^n + SoC_3^n} > 1 \text{ LSC} \tag{10}$$

Inequations (8) and (10) are both considered for a maximum n.

If $i_{\text{sum}} - i_{\text{satu}} > i_{\text{satu}}$, that is, $i_{\text{sum}} > 2\ i_{\text{satu}}$, it is possible that two units are saturated. To establish the above situation, the minimum n can be found, which is formulated as

$$CDR_{11}|_{t=0} > i_{\text{satu}}/i_{\text{sum}}, CDR_{22}|_{t=0} > i_{\text{satu}}/i_{\text{sum}} \tag{11}$$

In addition, the maximum n is derived according to Inequation (8).

As for series applications, the minimum n should let $g + h = 2$ so that the high current deviations help shorten the balancing duration. In Figure 6a, four potential paths exist, and they are separately expressed as

$$CDR_{11}|_{t=0} > i_{\text{satu}}/i_{\text{sum}}, CDR_{22}|_{t=0} > i_{\text{satu}}/i_{\text{sum}} \tag{12}$$

$$\begin{cases} CDR_{11}|_{t=0} \leq i_{\text{satu}}/i_{\text{sum}}, CDR_{13}|_{t=0} < i_{\text{satl}}/i_{\text{sum}} \\ CDR_{32}|_{t=0} < i_{\text{satl}}/i_{\text{sum}} \end{cases} \tag{13}$$

$$\begin{cases} CDR_{11}|_{t=0} > i_{\text{satu}}/i_{\text{sum}} \\ CDR_{22}|_{t=0} < i_{\text{satu}}/i_{\text{sum}}, CDR_{23}|_{t=0} < i_{\text{satl}}/i_{\text{sum}} \end{cases} \tag{14}$$

$$\begin{cases} CDR_{11}|_{t=0} \leq i_{\text{satu}}/i_{\text{sum}}, CDR_{13}|_{t=0} < i_{\text{satl}}/i_{\text{sum}} \\ CDR_{32}|_{t=0} \geq i_{\text{satl}}/i_{\text{sum}}, CDR_{31}|_{t=0} > i_{\text{satu}}/i_{\text{sum}} \end{cases} \tag{15}$$

In fact, only one of the above four expressions is feasible if a specific set of i_{sum}, SoC_{k0}, and current limits is adopted. And Inequation (8) is applied to acquire maximum n.

3.3. Selection of the Current Limits in CDRs

If the enhanced strategy is used for parallel applications, i_{satu} cannot be too low. It should satisfy the following:

$$\frac{i_{\text{satu}}}{i_{\text{sum}}} > \frac{SoC_{10}}{SoC_{10} + SoC_{20} + SoC_{30}} \tag{16}$$

Otherwise, the equilibrium point is not reachable before the SoC reaches zero.

When $i_{\text{sum}} < 2i_{\text{satu}}$, only one ESU may be saturated, namely, ESU#1. The other two ESUs are equalized at the very start. Then, the two currents correspond to

$$i_2 = (i_{\text{sum}} - i_{\text{satu}}) \times \frac{SoC_3^n}{SoC_3^n + SoC_2^n}, i_3 = (i_{\text{sum}} - i_{\text{satu}}) \times \frac{SoC_3^n}{SoC_3^n + SoC_2^n} \tag{17}$$

After ESU#2 and ESU#3 are balanced, CDR_{11} should continuously decrease until reaching $1/3$ and the equalization of the three ESUs is acquired. The slope of CDR_{11} is calculated as

$$\begin{cases} CDR'_{11} = \frac{nSoC_1^{n-1}[ASoC_2^{n-1} + BSoC_3^{n-1}]}{(SoC_1^n + SoC_2^n + SoC_3^n)^2} \\ A = SoC_2SoC'_1 - SoC_1SoC'_2, B = SoC_3SoC'_1 - SoC_1SoC'_3 \end{cases} \tag{18}$$

where '$\prime$' is a time-derivative operator. The following is introduced:

$$\begin{cases} SoC_2 = SoC_3 \\ SoC'_2 = SoC'_3 = -(i_{\text{sum}} - i_{\text{satu}})/(2Q) \\ SoC'_1 = -i_{\text{satu}}/Q \end{cases} \tag{19}$$

Afterwards, the numerator of Equation (18) is deduced as follows:

$$\text{num}(CDR'_{11}) = nSoC_1^{n-1}SoC_2^{n-1}[i_{\text{sum}} \times SoC_1 - i_{\text{satu}}(SoC_1 + SoC_2 + SoC_3)]/Q \tag{20}$$

Thus, the reachable restriction is represented as

$$\frac{i_{\text{satu}}}{i_{\text{sum}}} > \frac{SoC_1}{SoC_1 + SoC_2 + SoC_3} \tag{21}$$

Accordingly, CDR_{11} will decline. To actualize Inequation (21), the maximum of the right side needs to be found. In fact, it persistently drops until reaching $1/3$, as the individual SoC levels come closer and closer under the balancing control. Thus, its maximum is just the initial value. Undoubtedly, Inequation (21) is guaranteed if only Inequation (16) is realized.

When $i_{\text{sum}} > 2i_{\text{satu}}$, ESU#1 and ESU#2 are saturated in the beginning. With the SoC levels approaching each other, ESU#2 becomes unsaturated earlier, and the following condition is met:

$$(i_{\text{sum}} - i_{\text{satu}}) \times \frac{SoC_2^n}{SoC_2^n + SoC_3^n} = i_{\text{satu}} \tag{22}$$

By simplifying Equation (22), we have

$$\frac{SoC_3}{SoC_2} = \sqrt[n]{\frac{i_{\text{sum}}}{i_{\text{satu}}} - 2} = w \in (0, 1] \tag{23}$$

Then, $i_2 = i_{\text{satu}}$ and $i_3 = i_{\text{sum}} - 2i_{\text{satu}}$. Combination with Equation (3) yields

$$t_0 = \frac{Q(wSoC_{20} - SoC_{30})}{(w+2)i_{\text{satu}} - i_{\text{sum}}} < \min\left(\frac{QSoC_{30}}{i_{\text{sum}} - 2i_{\text{satu}}}, \frac{QSoC_{20}}{i_{\text{satu}}}\right) \tag{24}$$

Equation (23) implies that $i_{sum} = (2 + w^n)\, i_{satu} < (2 + w)\, i_{satu}$. Moreover, we determined that $w = SoC_3/SoC_2 > SoC_{30}/SoC_{20}$ as $i_2 > i_3$. Thus, t_0 is positive. Another question is whether the moment t_0 occurs before SoC_2 and SoC_3 decrease to zero as Inequation (24) states. This restriction is assumed correct, and then the balancing operation begins between ESU#2 and ESU#3. After the SoC levels of the two ESUs are identical, the situation is the same as that when $i_{sum} < 2i_{satu}$. Three balanced ESUs can be obtained once Inequation (16) is met. Based on Inequations (16) and (24), it is inferred that

$$\frac{i_{sum} - 2i_{satu}}{(w+2)i_{satu} - i_{sum}} < \frac{SoC_{20} + SoC_{30} - SoC_{10}}{(w+1)SoC_{10} - SoC_{20} - SoC_{30}} < \frac{SoC_{30}}{wSoC_{20} - SoC_{30}} \tag{25}$$

Therefore, it is ensured that $t_0 < Q * SoC_{30}/(i_{sum} - 2i_{satu})$. For convenient analysis, auxiliary function $f_1(x)$ is defined as

$$f_1(x) = \left(\sqrt[n]{x-2} + 2 - x\right)^{-1}, x = i_{sum}/i_{satu} \in (2, 3] \tag{26}$$

In fact, $f_1(x)$ is positive, and it increases when x increases. Based on Inequation (16), the following relationship can be deduced:

$$\frac{i_{satu}}{(w+2)i_{satu} - i_{sum}} < \frac{SoC_{10}}{(w+1)SoC_{10} - SoC_{20} - SoC_{30}} \tag{27}$$

Also, $f_2(y)$ is defined as follows

$$f_2(y) = \frac{y}{(w+1)y - SoC_{20} - SoC_{30}}, y = SoC_{k0} \in (0, 1] \tag{28}$$

In fact, $f_2(y)$ decreases while y increases, thus proving that

$$\frac{SoC_{10}}{(w+1)SoC_{10} - SoC_{20} - SoC_{30}} < \frac{SoC_{20}}{wSoC_{20} - SoC_{30}} \tag{29}$$

Combining Inequation (27) with Inequation (29), we attain the following: $t_0 < Q * SoC_{20}/i_{satu}$. In brief, the assumption in Inequation (24) is true as long as Inequation (16) is established.

In series scenarios, the minimum i_{satu} is the same as that in parallel scenarios. However, there exists an upper limit i_{satuu} for i_{satu}. If i_{satu} exceeds i_{satuu}, a step change in the reference current will appear when some ESUs become desaturated. Furthermore, this leads to the deterioration of u_{dc} in actual systems. To improve power quality, this phenomenon ought to be avoided.

According to Equation (7), CDR_{11} decreases and CDR_{23} increases after the balancing strategy is enabled. If CDR_{11} drops to i_{satu}/i_{sum} after CDR_{23} increases to i_{satl}/i_{sum}, the unexpected step reference current is actually averted, which is expressed as

$$CDR_{11}|_{t=t_1} = i_{satu}/i_{sum}, CDR_{23}|_{t=t_2} = i_{satl}/i_{sum}, t_1 \geq t_2 \tag{30}$$

Suppose that n is large enough to make each phase current constant in the beginning. If $i_{satl} < i_{sum} - i_{satu} - i_{satl} < i_{satu}$, three currents are separately distributed as

$$i_1 = i_{satu}, i_2 = i_{sum} - i_{satl} - i_{satu}, i_3 = i_{satl} \tag{31}$$

By substituting Equation (31) into CDR_{23}, we have

$$\left(1 - \frac{i_{satu}}{i_{sum}}\right) \times \frac{SoC_3^n(t_1)}{SoC_2^n(t_1) + SoC_3^n(t_1)} = \frac{i_{satl}}{i_{sum}} \tag{32}$$

Combining Equations (3), (31), and (32) yields

$$t_1 = \frac{\sqrt[n]{(i_{\text{sum}} - i_{\text{satu}} - i_{\text{satl}})/i_{\text{satl}}} \times SoC_{30} - SoC_{20}}{\sqrt[n]{(i_{\text{sum}} - i_{\text{satu}} - i_{\text{satl}})/i_{\text{satl}}} \times i_{\text{satl}} - i_{\text{sum}} + i_{\text{satu}} + i_{\text{satl}}} \times Q \tag{33}$$

To obtain the critical i_{satu} in Equation (30), replace t_2 with t_1. After combination with Equation (31), CDR_{11} is rewritten as

$$\frac{[SoC_{10} - i_{\text{satu}} t_1/Q]^n}{[SoC_{20} - (i_{\text{sum}} - i_{\text{satu}} - i_{\text{satl}})t_1/Q]^n + [SoC_{30} - i_{\text{satl}} t_1/Q]^n} = \frac{i_{\text{sum}} - i_{\text{satu}}}{i_{\text{satu}}} \tag{34}$$

An analytical solution is hard to acquire, as Equation (34) is a high-order equation about i_{satu}. Instead, tool software can be used to facilitate the solving procedure. Then, a numerical solution can be obtained, and that is exactly the value of i_{satuu}.

When load change occurs, i_{satl} and i_{satu} require proper adjustment so that the equilibrium point is still accessible and the step current references are escapable. According to energy conservation, i_{sum} varies in the same direction and proportion when i_o suddenly changes. That is to say, the variation in i_{sum} directly reflects the variation in i_o. Accordingly, i_{satl} and i_{satu} are rearranged as

$$i_{\text{satu}} = i_{\text{satu0}} \times i_{\text{sum}}/i_{\text{sum0}}, i_{\text{satl}} = i_{\text{satl0}} \times i_{\text{sum}}/i_{\text{sum0}} \tag{35}$$

where i_{sum0}, i_{satu0}, and i_{satl0} are the initial values of i_{sum}, i_{satu}, and i_{satl}, respectively. By using Equation (35) to update the two limits, $i_{\text{satu}}/i_{\text{sum}}$ remains constant when i_o varies. By substituting Equation (35) into Equation (33), the required duration becomes $i_{\text{sum0}}/i_{\text{sum}}$ times its original value. Meanwhile, each phase current is $i_{\text{sum}}/i_{\text{sum0}}$ times its original value based on Equation (31). Furthermore, the depth of discharge of each ESU remains unchanged. Thus, Equation (34) is still fulfilled, and a smooth transition of the reference current is guaranteed.

When $i_{\text{sum}} - i_{\text{satu}} - i_{\text{satl}} > i_{\text{satu}}$, the phase currents are i_{satu}, i_{satu}, and $i_{\text{sum}} - 2i_{\text{satu}}$, respectively. When $i_{\text{sum}} - i_{\text{satu}} - i_{\text{satl}} < i_{\text{satl}}$, the phase currents are $i_{\text{sum}} - 2i_{\text{satl}}$, i_{satl}, and i_{satl}, respectively. In a similar way, Equations (33) and (34) can be calculated by replacing Equation (31). It can be further verified that the variable current limits formulated as Equation (35) are still effective for preventing step reference currents.

In addition, the reachable condition is also analyzed when i_o varies. On the one hand, $i_{\text{satu}}/i_{\text{sum}}$ is constant with the variable i_{satu}. On the other hand, the ratio increases with a fixed i_{satu} because the accelerating factor and current limits are designed under full load. Thus, i_{sum} is lower than i_{sum0}, and Inequation (16) is always satisfied under load change.

To select proper i_{satu} for series applications, there are two key points. First, in order to remove the potential step reference currents, i_{satu} should not be too high, although a higher i_{satu} helps reduce the equalization time. Second, i_{satu} is designed to be proportional to i_{sum} in case the step reference currents occur under load change.

3.4. Theoretical Comparisons of Balancing Performance

In DSP28335 chips, the bit number of the analog-to-digital converter is 12, and the analog input voltage ranges from 0 to 3 V. The rated current of the adopted current sensor, LA50P, is 50 A. Through signal conditioning, 50 A is transformed to 3 V on DSP pins. As a result, 1 LSC = 50 A/($2^{12} - 1$) = 0.012 A, which is mentioned in Inequation (10). Based on the actual test, 1000 multiplications require about 170 us. This means t_{mul} is 0.17 us. When i_{satu0} = 33 A, i_{sum0} = 50 A, and t_{else} = 37 us in parallel applications, it can be derived that $n \leq 54$ based on Inequations (8) and (10), while $n \geq 9$ based on Inequation (9). When i_{satu0} = 33 A, i_{satl0} = 6 A, $_{\text{isum0}}$ = 45 A, and t_{else}= 39 us in series applications, we can acquire that $n \geq 11$ based on Inequation (14) and $n \leq 64$ based on Inequation (8). Furthermore, i_{satuu} was calculated as 24.2 A. The practical i_{satu0} is adopted as 24 A for series applications. For fast convergence, n is set as 50 for both applications.

As shown in Figure 7, a numerical simulation was carried out to acquire theoretical curves under various conditions. For simplicity, power losses are ignored. Moreover, it is assumed that i_k follows its reference current immediately and u_{ik} is constant at its nominal value (12 V). Figure 8 gives the theoretical curves when the proposed strategy is used in parallel scenarios. As seen in Figure 8a,d, the equilibrium point is not accessible if i_{satu} = 18 A because Inequation (16) is not fulfilled. In addition, a higher i_{satu} contributes to shorter balancing duration because higher current deviations enable a faster approaching speed of SoC levels. As Figure 8b,e exhibit, a larger n also helps to accelerate the balancing process among unsaturated ESUs, but the improved effect is no longer remarkable if n is large enough. When load is reduced at 200 s and then restored at 1000 s, current balance and SoC equalization are still achieved. The relevant process is shown in Figure 8c,f.

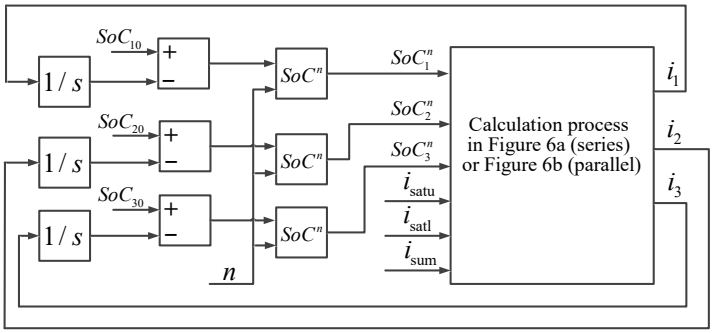


Figure 7. Schematic diagram of numerical simulation.

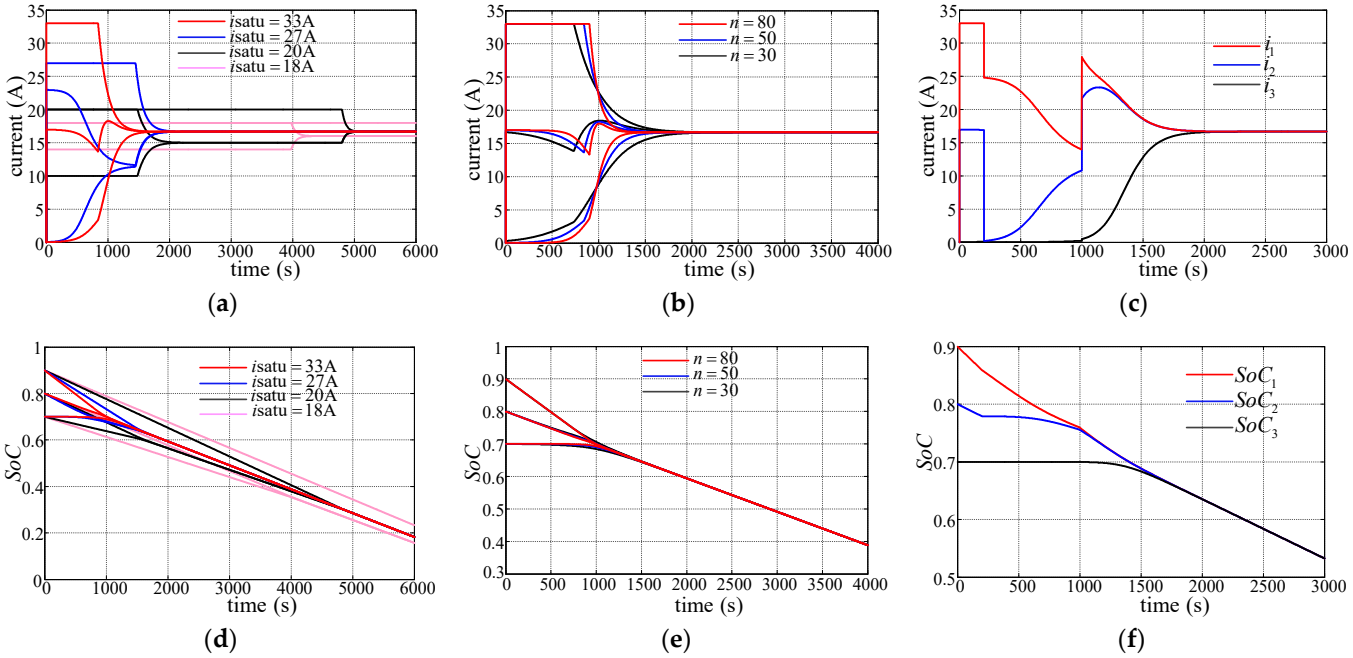


Figure 8. Ideal curves in parallel applications: (**a**) currents under different values of i_{satu}, (**b**) currents under different accelerating factors, (**c**) currents under load change, (**d**) SoC under different values of i_{satu}, (**e**) SoC under different accelerating factors, and (**f**) SoC under load change.

Figure 9 displays the ideal waveforms when the proposed strategy is utilized in series scenarios. Figure 9a,d reveal that step reference currents are generated if i_{satu} > 24.2 A, e.g., i_{satu} = 30 A. If i_{satu} is fixed as 24 A under load variation, this may also lead to step reference current even if the load is restored. This is seen in Figure 9b,e. To fix this issue, a variable i_{satu} is applied. In Figure 9c,f, the undesired step references are avoided, and the corresponding balancing duration is not obviously lengthened.

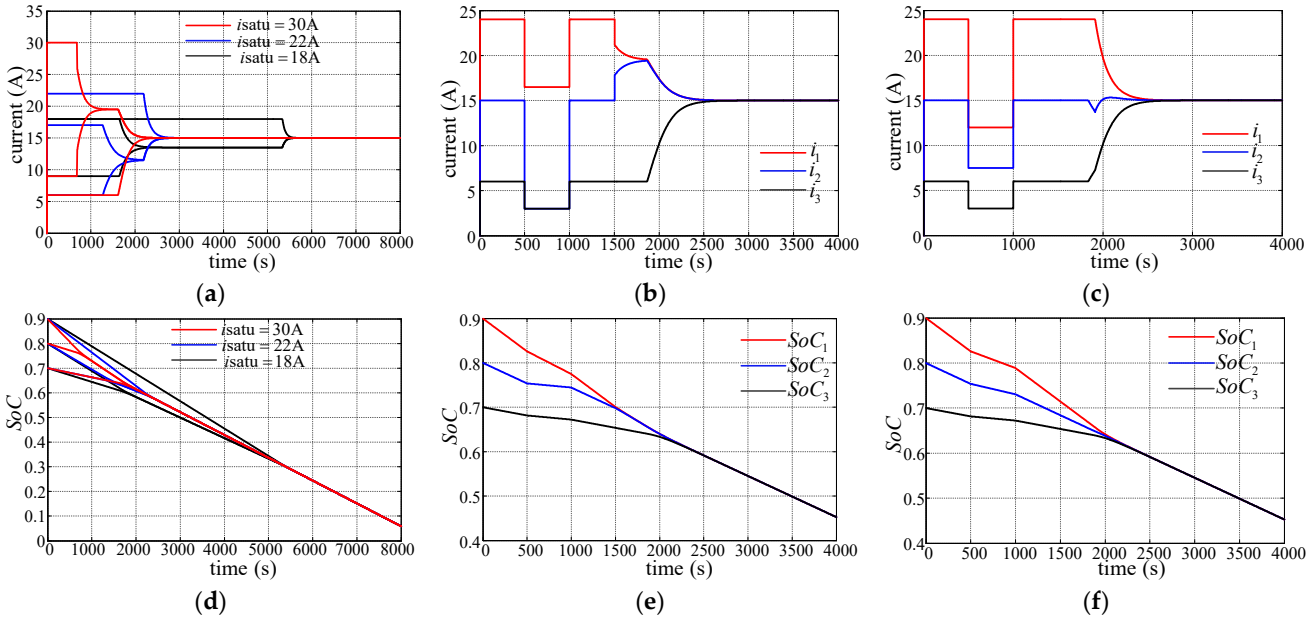


Figure 9. Ideal curves in series applications: (**a**) currents under different i_{satu}, (**b**) currents under load change with fixed i_{satu}, (**c**) currents under load change with variable i_{satu}, (**d**) SoC under different i_{satu}, (**e**) SoC under load change with fixed i_{satu}, and (**f**) SoC under load change with variable i_{satu}.

In Figure 10, ESU#1 is the master unit. Here, i_{satu} is 33 A in parallel applications and 24 A in series applications, respectively. When ESU#2 is suddenly stopped (letting $d_2 = 0$), the SoC_2 is subsequently set to zero so that the energy of ESU#1 and ESU#3 can be redistributed for SoC balance. Under the proposed strategy, the balanced point is still reached between the rest units after a slave ESU exits the microgrids.

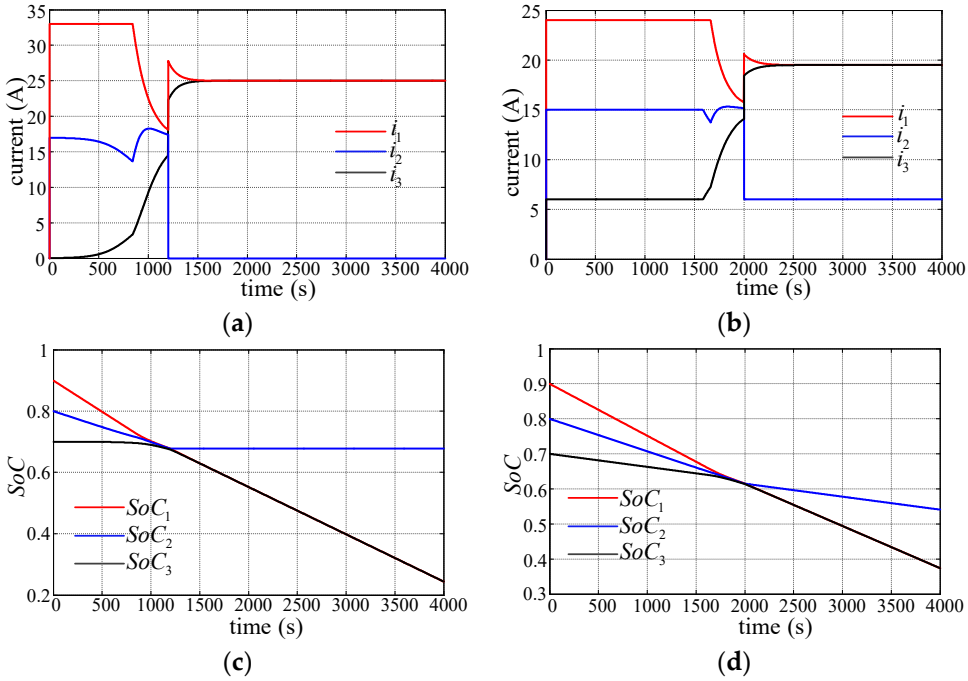


Figure 10. Ideal curves when ESU#2 is ceased: (**a**) currents in parallel applications, (**b**) currents in series applications, (**c**) SoC in parallel applications, and (**d**) SoC in series applications.

Battery degradation is commonly existent after numerous charge and discharge cycles. Furthermore, the usable capacity thereupon decreases. Thus, it is important to evaluate the

effectiveness of the proposed strategy in such a scenario. Figure 11 exhibits the ideal curves when the proposed strategy is applied in a scenario wherein batteries degrade. Here, i_{satu} is 33 A in parallel applications and 24 A in series applications. Moreover, the three battery capacities, Q_1, Q_2, and Q_3, are 45 Ah, 38.4 Ah, and 41.7 Ah, respectively. The results show that this balancing method can still mitigate SoC deviations when battery capacities are inconsistent. Note that i_1, i_2, and i_3 are 16.2 A, 13.8 A, and 15 A, respectively, after SoC balance is achieved. In fact, they are proportional to the corresponding capacities of their own ESUs. In this case, the equal declining rate of SoC is shared by all ESUs and thus SoC balance can be maintained.

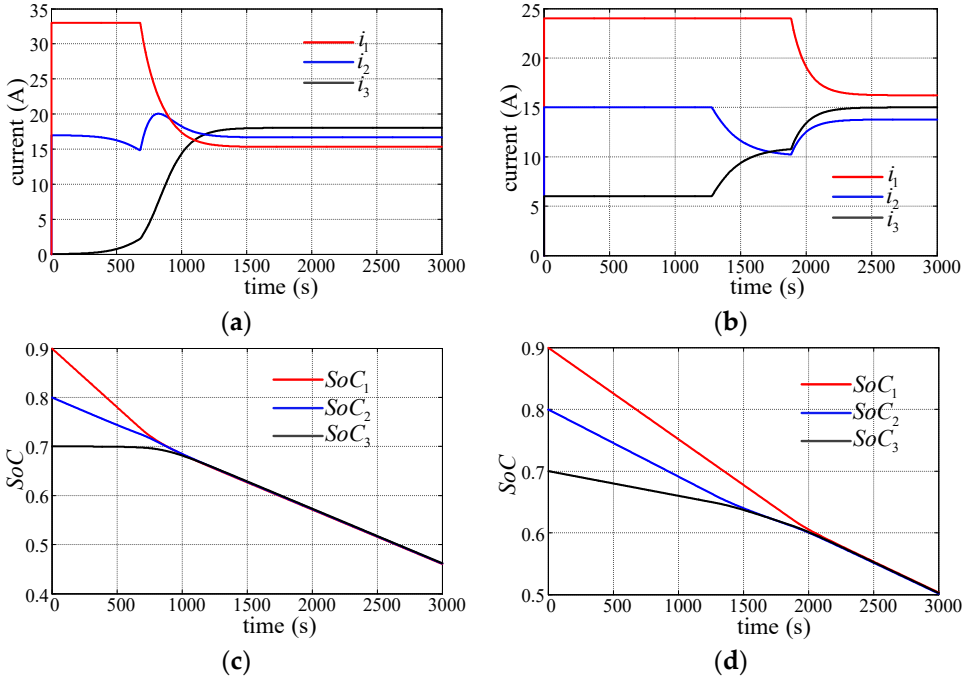


Figure 11. Ideal curves under conditions of battery degradation: (**a**) currents in parallel applications, (**b**) currents in series applications, (**c**) SoC in parallel applications, and (**d**) SoC in series applications.

3.5. Design of a Dual-Loop Controller

The selection of controller parameters is vital to implement a control scheme. In fact, it directly influences the stability and dynamic performance of energy storage systems. Compared with other balancing methods, the main difference of the proposed strategy is the voltage loop after CDRs are introduced. A simplified control diagram of the k-th unit is outlined in Figure 12. Typical PI regulators are applied for both voltage and current control. In parallel applications, the transfer functions from d_k to i_k, G_{idk} and from i_k to u_{dc}, G_{vik} are formulated as

$$G_{idk} = \frac{u_{ik}(RCs+2)}{[L_kCRs^2 + L_ks + mR(1-d_k)^2](1-d_k)} \tag{36}$$

$$G_{vik} = \frac{mR(1-d_k)^2 - sL_k}{(1-d_k)(RCs+2)} \tag{37}$$

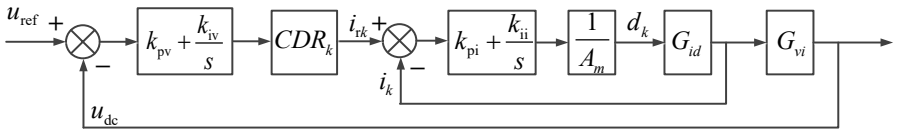


Figure 12. Simplified control block diagram for k-th unit.

As u_{ik} varies little during discharge, it is considered to equal 12 V, which is the nominal battery voltage.

The adopted controller parameters are shown in Table 2. A bode diagram of the open current loop is given in Figure 13a, and w_c is the cut-off frequency. The stability margin of the inner loop is at least 83° and w_c is at least 370 rad/s when R ranges from 3 Ω to 1.5 Ω. The upper and lower limits of the CDR are 0.66 and 0.00024, which correspond to 33 A (i_{satu} in parallel applications) and 0.012 A (1 LSC in Inequation (10)). There are usually deviations between the real and nominal resistances. Similar phenomena also occur for the inductance and capacitance in actual converters. In addition, the CDR of each unit gradually varies until SoC balance is achieved. Therefore, the abovementioned cases were all considered when choosing k_{pv} and k_{iv}. Sufficient stability margins are effective solutions to mitigating these issues. For conventional applications, the phase margin is usually designed to be no less than 45 degrees. In order to ensure stable operation under CDR variations and mismatches of circuit parameters, the phase margin is enhanced to no less than 70 degrees in this paper. In Figure 13b, the magnitude and phase response curves under several boundary conditions are depicted. The expected phase margins are acquired. Although the voltage-loop w_c is low, it is acceptable, as the guaranteed system stability is a prerequisite for balancing control.

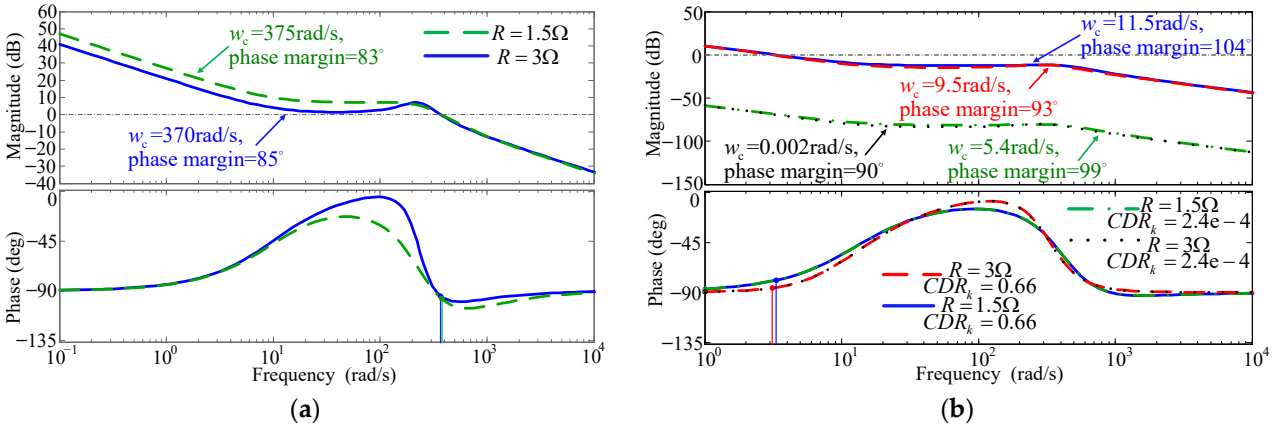


Figure 13. Bode diagram of open-loop system: (**a**) current loop and (**b**) voltage loop.

As for series applications, the values of the control parameters are the same. The procedures for controller design are similar and have been omitted for convenience.

4. Experimental Verification

4.1. Experimental Platform

The configuration of the experimental platform is given in Figure 14, and the practical prototype is shown in Figure 15. The system parameters are shown in Table 2. IRFP4668PBF-type MOSFETs were used as power switches and diodes. The upper arm of the half bridge was kept off, while the lower arm was controlled by a PWM signal. Then, the boost converter was designed in such a manner. For simplicity, all the current loops share the same control parameters.

To accomplish dual-loop control, the feedback signal of inductor current was sent to its own DSP, while the sensing signal of u_{dc} was addressed by DSP#1 (master) to conduct voltage regulation. The resulting reference current was also calculated there and subsequently shared through a controller area network (CAN). Detailed communication variables are presented in Table 4. Considering that the balancing time is quite long, the overall process was recorded using LabVIEW 2018 software. In the RS232 style, the laptop receives the timing data package from DSP#1 and depicts waveforms in LabVIEW.

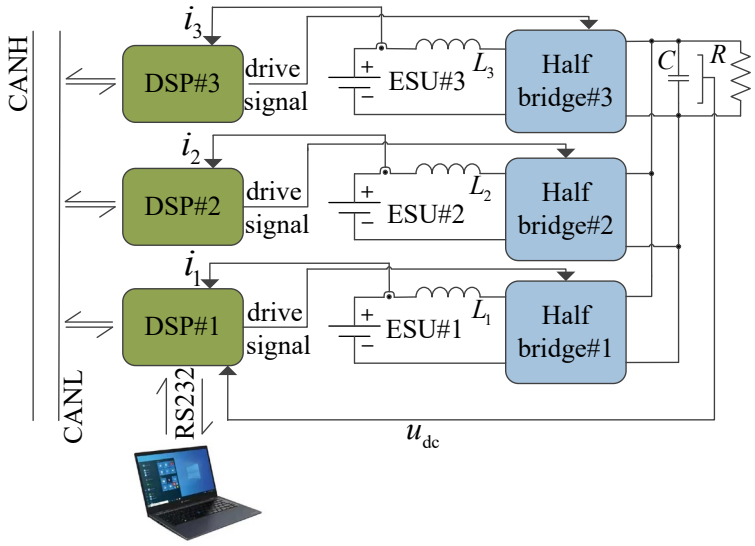


Figure 14. Schematic diagram of experimental platform.

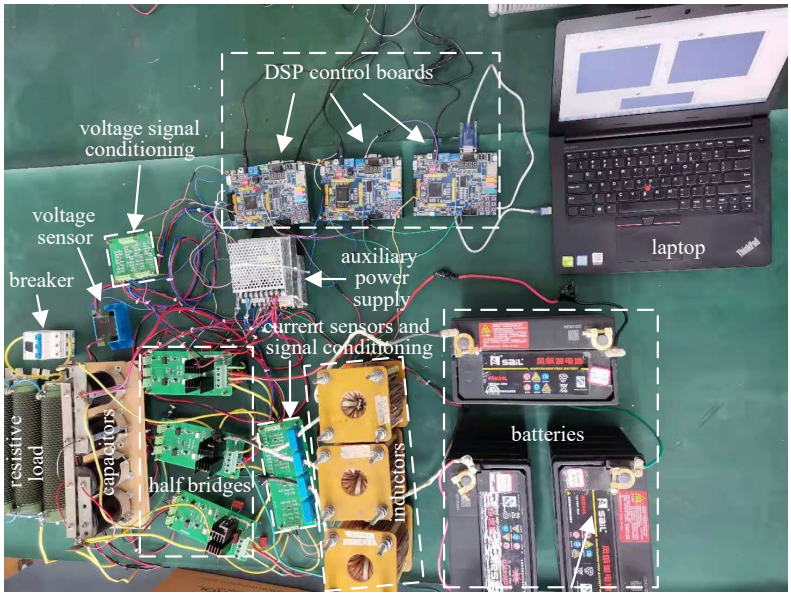


Figure 15. Photo of experimental platform.

Table 4. Communication variables.

Communication	Transmission	Reception	Involved Variables
CAN	DSP#1	DSP#2	i_{sum}, SoC_1^n, SoC_3^n,
	DSP#2	DSP#1	SoC_2^n, SoC_2, i_2
	DSP#1	DSP#3	i_{sum}, SoC_1^n, SoC_2^n
	DSP#3	DSP#1	SoC_3^n, SoC_3, i_3
RS232	Labview	DSP#1	u_{ref}
	DSP#1	Labview	u_{dc}, i_1, i_2, i_3
			SoC_1, SoC_2, SoC_3

4.2. Testing Results and Analysis

First, the items of parallel applications without saturation were analyzed, and the related results are shown in Figure 16a,c. To validate the strategy without saturation in parallel applications, n was set to 8 to guarantee that the peak current was no higher than

i_{satu}. To ensure that u_{dc} was constant, the phase currents were set to gradually increase as a result of a declining SoC and increasing inner resistances. The equilibrium point was reached at 3800 s. Subsequently, i_{satu} was adopted to accelerate the convergence of the balancing process, and n was increased to 50. The required time was about 1450 s according to Figure 17a,c. This corresponds to time savings of around 62% when current saturation is applied. After that, the experiment conducted under variable load (n = 50) was carried out. As Figure 17b displays, the load current was suddenly reduced by half at t = 200 s, while it returned to 20 A after a duration of 800 s. According to the testing data, equal SoC levels and currents were still realized, although the balanced point is delayed somewhat.

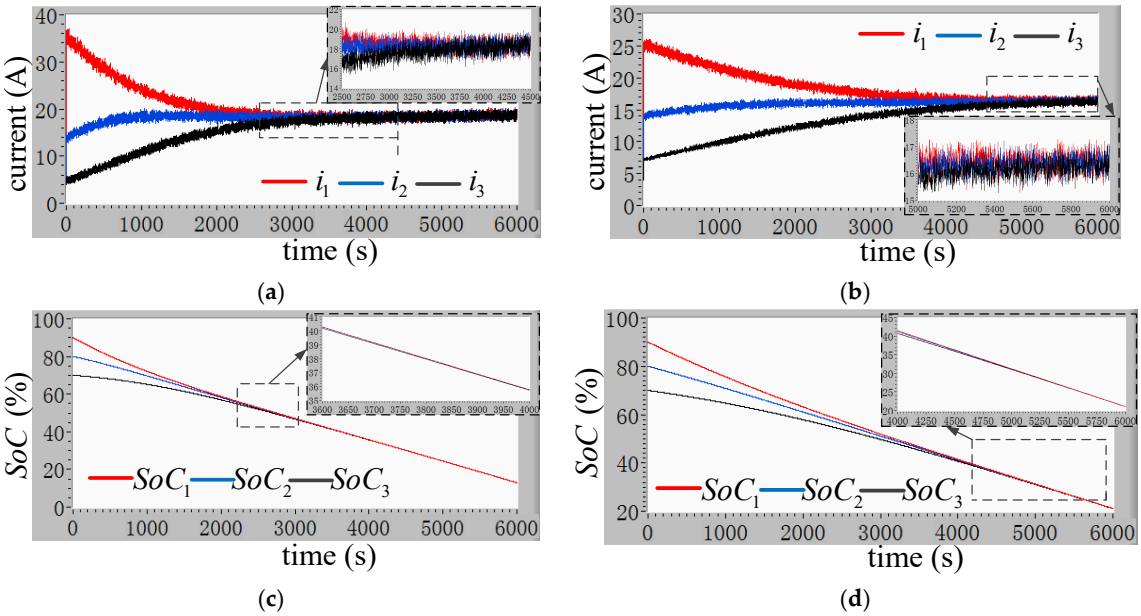


Figure 16. Experimental curves without saturation: (**a**) currents in parallel applications, (**b**) currents in series applications, (**c**) SoC in parallel applications, and (**d**) SoC in series applications.

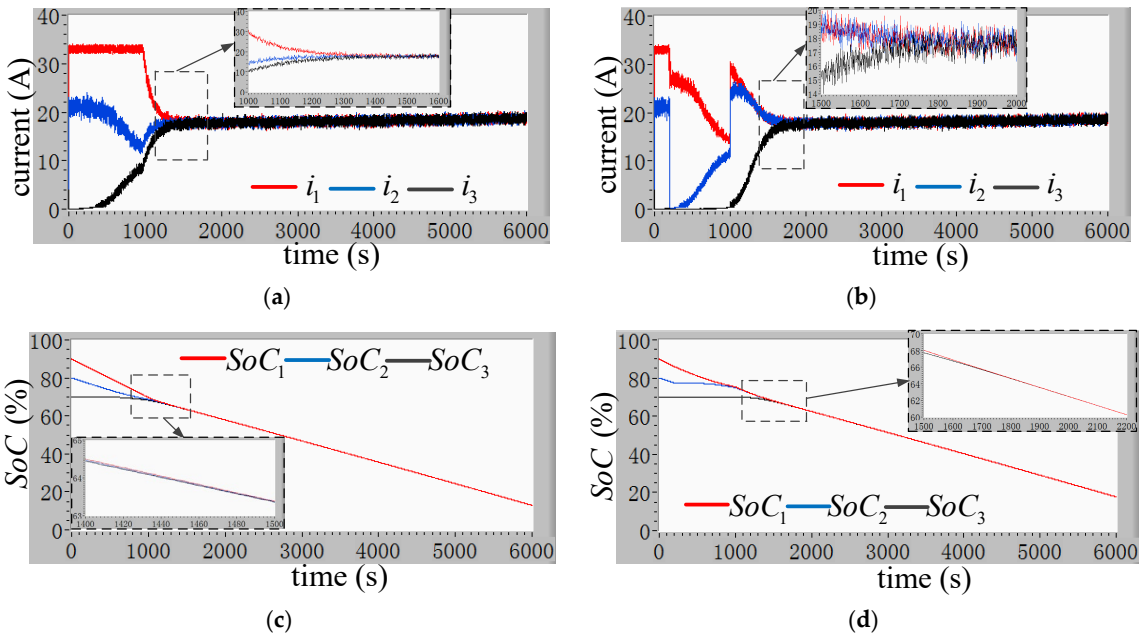


Figure 17. Experimental curves using saturation in parallel applications: (**a**) currents during normal operation, (**b**) currents under load change, (**c**) SoC during normal operation, and (**d**) SoC under load change.

After that, the series application experiments were performed, and the corresponding outcomes are described in Figure 16b,d. To ensure that phase currents are between i_{satu} and i_{satl}, the proper value of n should be 5. Based on Figure 16b,d, it takes as long as 5630 s to accomplish SoC equalization and current balance without saturation because only a small n is utilized. To reduce the balancing time, current saturations were put into use. Figure 18 gives the testing results for when i_{satu} is 24 A and 33 A, respectively. In terms of the requisite seconds, there is no obvious difference. However, voltage fluctuation exists when i_{satu} is 33 A because excessive i_{satu} leads to a step change in the current reference. In contrast, a steady voltage can be maintained when i_{satu} is 24 A. To check the performance regarding variable i_{satu}, tests of load change were executed, and the results are shown in Figure 19. Fixed saturation of the step current reference may be not escapable even if it is elaborately designed. The original condition for preventing step change may no longer be satisfied, as the trajectories of the currents have altered (more or less). If the upper limit varies in proportion to the sum current, the abovementioned condition is always realizable, and Figure 19b gives proof for this.

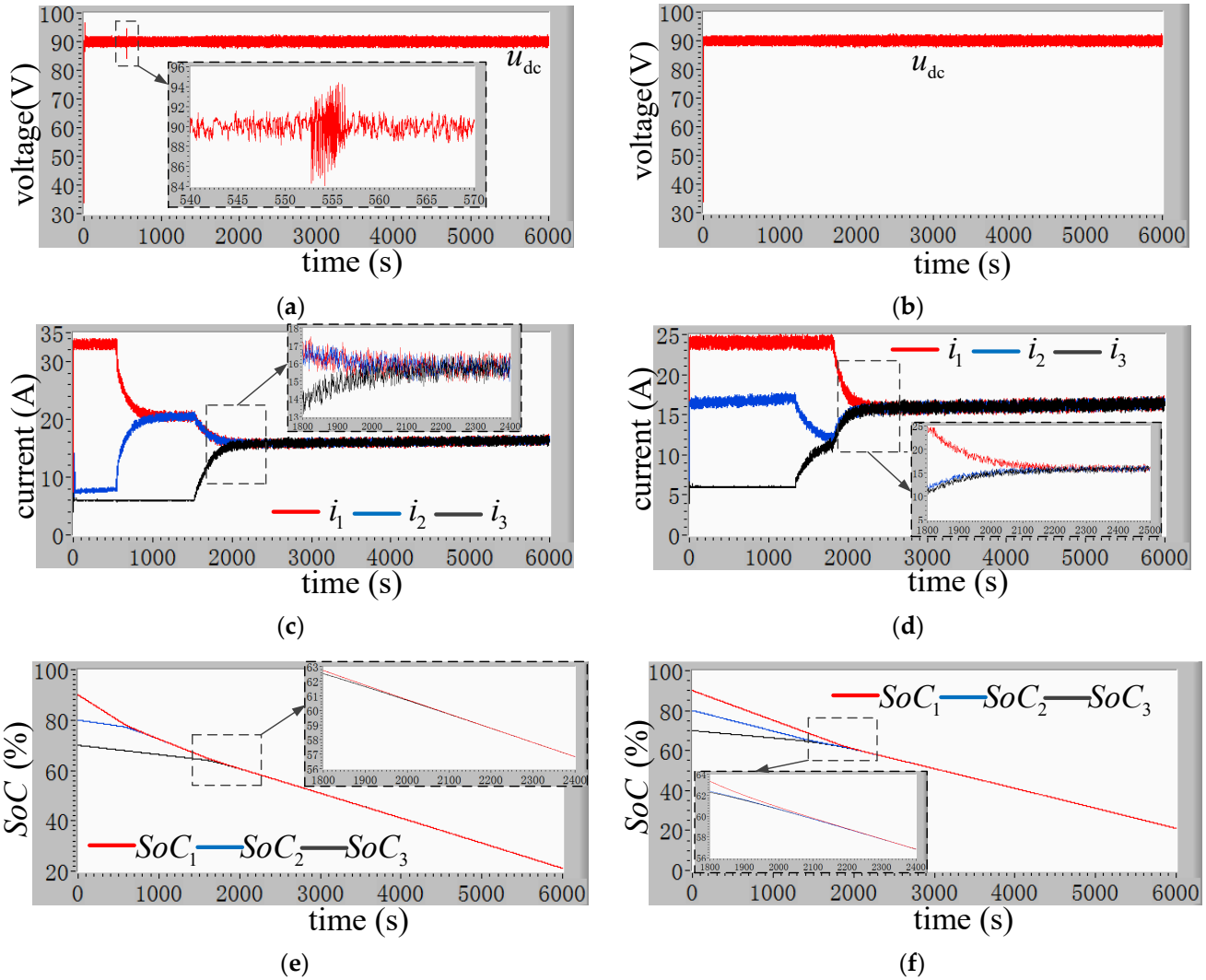


Figure 18. Experimental curves using different i_{satu} in series applications: (**a**) voltage when i_{satu} is 33 A, (**b**) voltage when i_{satu} is 24 A, (**c**) currents when i_{satu} is 33 A, (**d**) currents when i_{satu} is 24 A, (**e**) SoC when i_{satu} is 33 A, and (**f**) SoC when i_{satu} is 24 A.

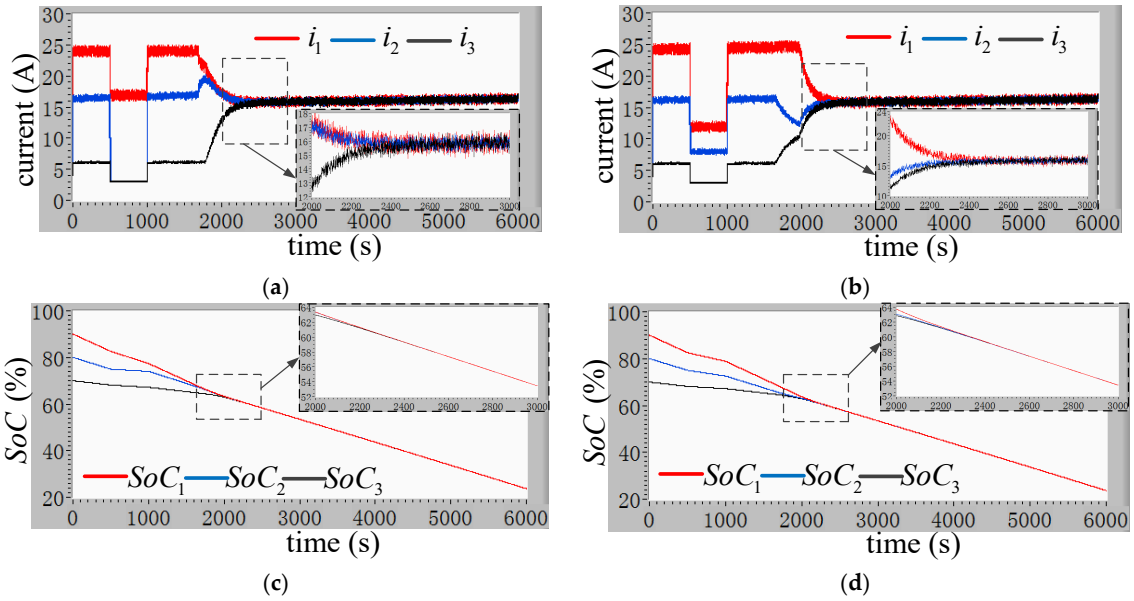


Figure 19. Experimental curves using different saturation styles in series applications: (**a**) currents under load change with fixed saturation, (**b**) currents under load change with variable saturation, (**c**) SoC under load change with fixed saturation, and (**d**) SoC under load change with variable saturation.

Moreover, the slave ESU#2 suddenly stopped working on validating the feasibility of the proposed strategy when the number of slave units was reduced. Figure 20 depicts the entire process when the duty cycle of PCU#2 is disabled in series and parallel applications. Then, SoC_1 and SoC_3 could still be allowed to move towards each other by setting the corresponding variables of SoC_2 in the communication network as zero. Finally, equal SoC levels and balanced currents were still achieved between the remaining ESUs. The SoC_2 linearly decreases in series applications because the load current flows through ESU#2. However, SoC_2 remains unchanged in parallel applications because D_2 is turned off as a result of inverse voltage. After this point, i_2 becomes zero. The experimental results almost agree with the theoretical analysis, which proves the effectiveness of the proposed strategy.

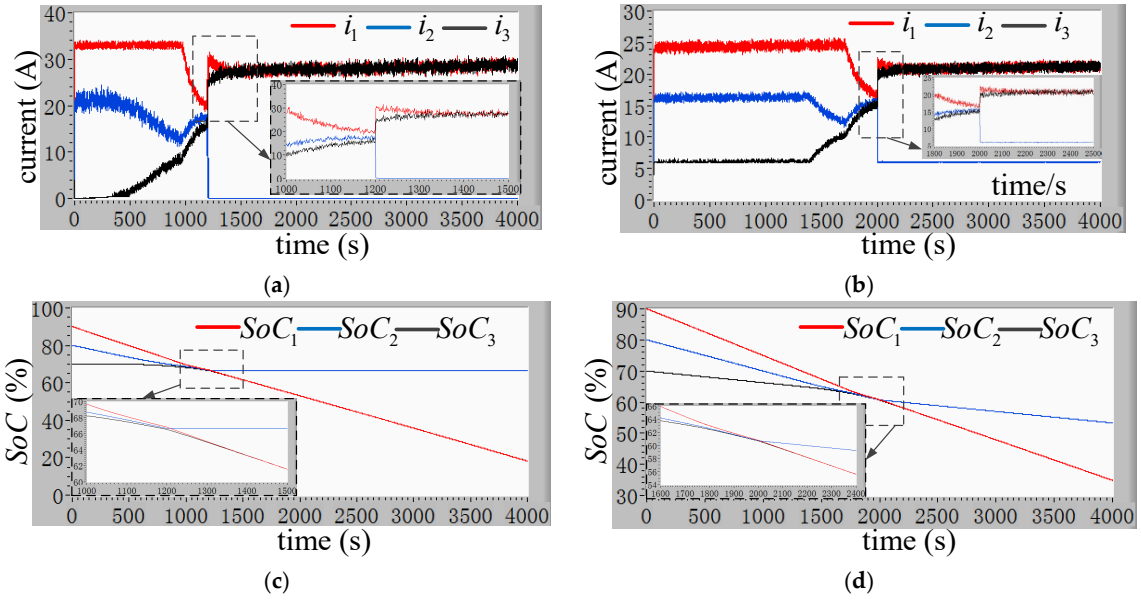


Figure 20. Experimental curves when ESU#2 has ceased functioning: (**a**) currents in parallel applications, (**b**) currents in series applications, (**c**) SoC in parallel applications, and (**d**) SoC in series applications.

Another two old batteries were used to carry out balancing control for the degradation condition. With the help of a battery tester, the actual levels of capacity reduction were obtained by measuring the internal resistance. The experimental waveforms of battery degradation are given in Figure 21. After the SoC levels had balanced, three currents were gradually increased to keep u_{dc} stable because the battery voltages decreased as a result of SoC decline. At the same time, it was satisfied that $i_1/Q_1 \approx i_2/Q_2 \approx i_3/Q_3$ after SoC errors were removed under the two kinds of applications. In other words, the ratio of steady current versus its own capacity was constant. With the proposed strategy, current sharing is realized when the battery capacities are match, so the balancing result with matched battery capacities can be seen as a special case of mismatched results.

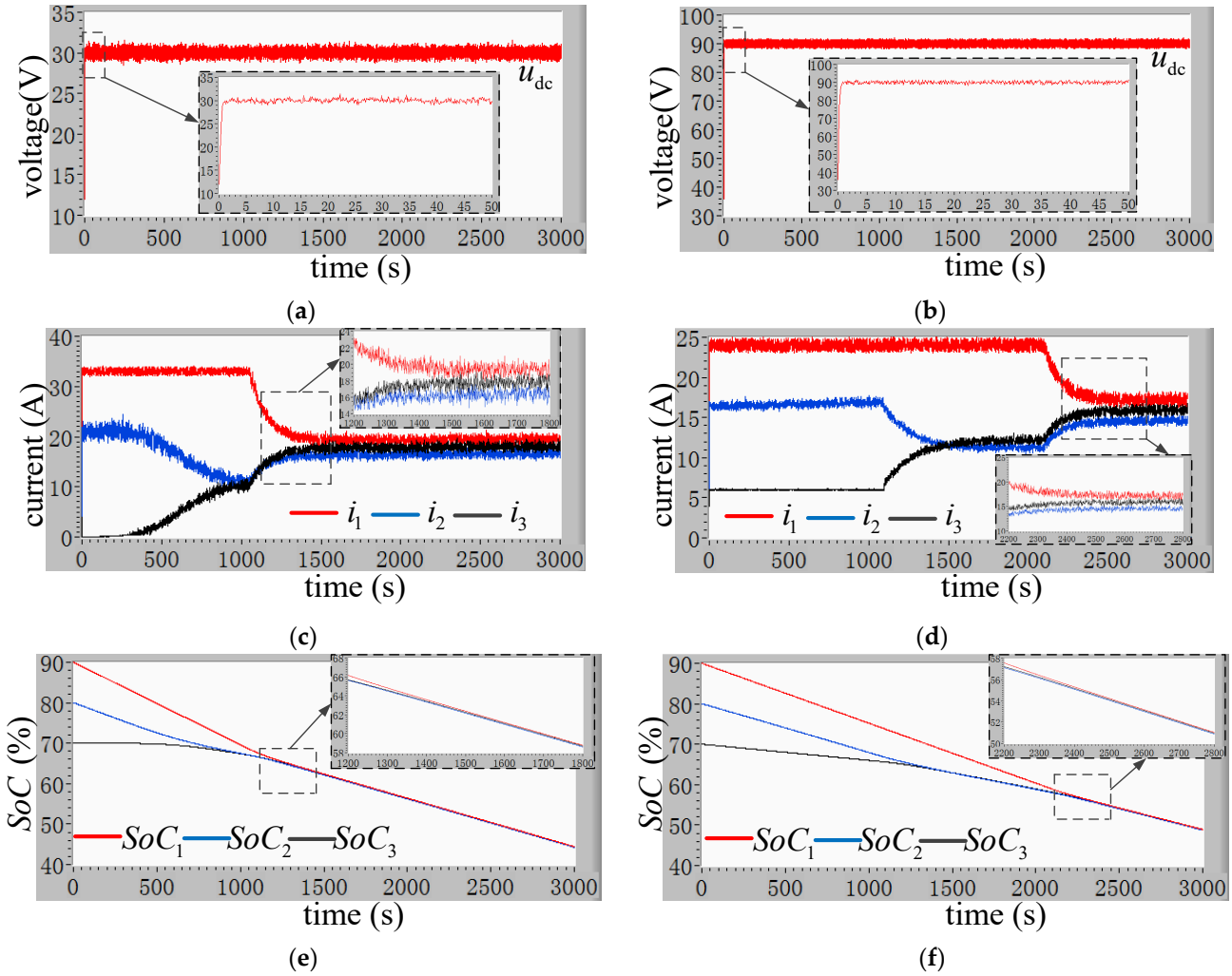


Figure 21. Experimental curves under battery degradation: (**a**) voltage in parallel applications, (**b**) voltage in series applications, (**c**) currents in parallel applications, (**d**) currents in series applications, (**e**) SoC in parallel applications, and (**f**) SoC in series applications.

The theoretical and actual balancing times required to achieve SoC consistency under different cases are collected in Table 5. To obtain the ideal curves, u_{ik} was assumed to be constant at 12 V to power the load in Section 3.4. Compared with the ideal time, the actual time was reduced. In the actual experiment, the battery voltages decreased and internal resistances increased during a long discharge, so d_k increases to keep u_{dc} unchanged and hence i_k gradually increased. With the same CDRs and circuit parameters, the higher the sum current, the shorter the duration required to eliminate SoC differences. In fact, this phenomenon contributes to the reduced balancing time.

Table 5. Theoretical and experimental comparisons of balancing time using the proposed strategy.

Case	Parallel Application			Series Application		
	Theoretical	**Actual**	**Deviation**	**Theoretical**	**Actual**	**Deviation**
Normal operation	1700 s	1450 s	14.7%	2400 s	2200 s	8.3%
Load change	2050 s	1800 s	12.2%	2600 s	2550 s	1.9%
Battery degradation	1560 s	1500 s	3.8%	2620 s	2550 s	2.7%
Sudden termination	1600 s	1400 s	12.5%	2350 s	2250 s	4.3%

To show the performance differences, experiments using the droop methods in reference [2] and [10] were further executed. The method in [2] is a typical voltage-type droop scheme, whose core expression is

$$u_{\text{ref_}k} = u_{\text{ref}} - m_0 SoC_k^n \frac{u_{ok} i_{ok}}{u_{ik}} \tag{38}$$

where $u_{\text{ref_}k}$, u_{ok}, and i_{ok} are the reference voltage, output voltage, and output current of the k-th unit, respectively. In [10], the current-type droop method is denoted as

$$i_{rk} = (u_{\text{ref}} - u_{\text{dc}}) m_1 SoC_k^n \tag{39}$$

where m_0 and m_1 are the initial droop coefficients, which must be properly chosen to prevent obvious voltage deviations. In [2], n was set as 8 in case the power of ESU#1 exceeded its allowable upper limit. A small m_0 helps to reduce the deviation of u_{dc}, and it is 1×10^{-5} here. In [10], i_{satu} was 33 A, and n was 50. A large m_1 leads to a lower voltage drop of u_{dc}, and it was set to 1×10^9. If m_1 is larger than 1×10^9, the system will be unstable. The related waveforms are presented in Figure 22. Affected by the mismatched power losses and line resistances in real circuits, the ESU with the highest SoC does not deliver the highest current in the primary stage. Based on Equations (38) and (39), u_{dc} gradually declines regardless of whether [2] or [10] is adopted because each SoC level persistently decreases when the discharge continues. The comparative indexes are summarized in Table 6. In contrast with [2] and [10], the results of the proposed strategy in Figure 17a,c display faster balancing speed because the voltage deviation is inexistent; hence, the sum current is always higher than that in the droop methods. Furthermore, a higher sum current leads to a faster mitigation of SoC differences with the same CDRs and circuit parameters. As for equalization precision, the proposed method removes the influence of actual power losses and u_{ik} decline, so it is more accurate. In [2] and [10], the SoC in real time is based on approximate estimation. However, the actual SoC during discharge is always lower than its approximate value used in microprocessor programs because ESUs must deliver higher currents to make up for power losses. Furthermore, the mismatched power losses of each unit enlarge the final SoC deviations between the highest and lowest SoC values. The corresponding results are shown in Table 6.

Table 6. Experimental performance comparisons of different methods.

Balancing Scheme	Balancing Duration	Final SoC Deviation
[2]	over 6000 s (Figure 22c)	around 0.9% (Figure 22e)
[10]	over 2300 s (Figure 22d)	around 0.3% (Figure 22f)
proposed	1450 s (Figure 17a)	around 0.1% (Figure 17c)

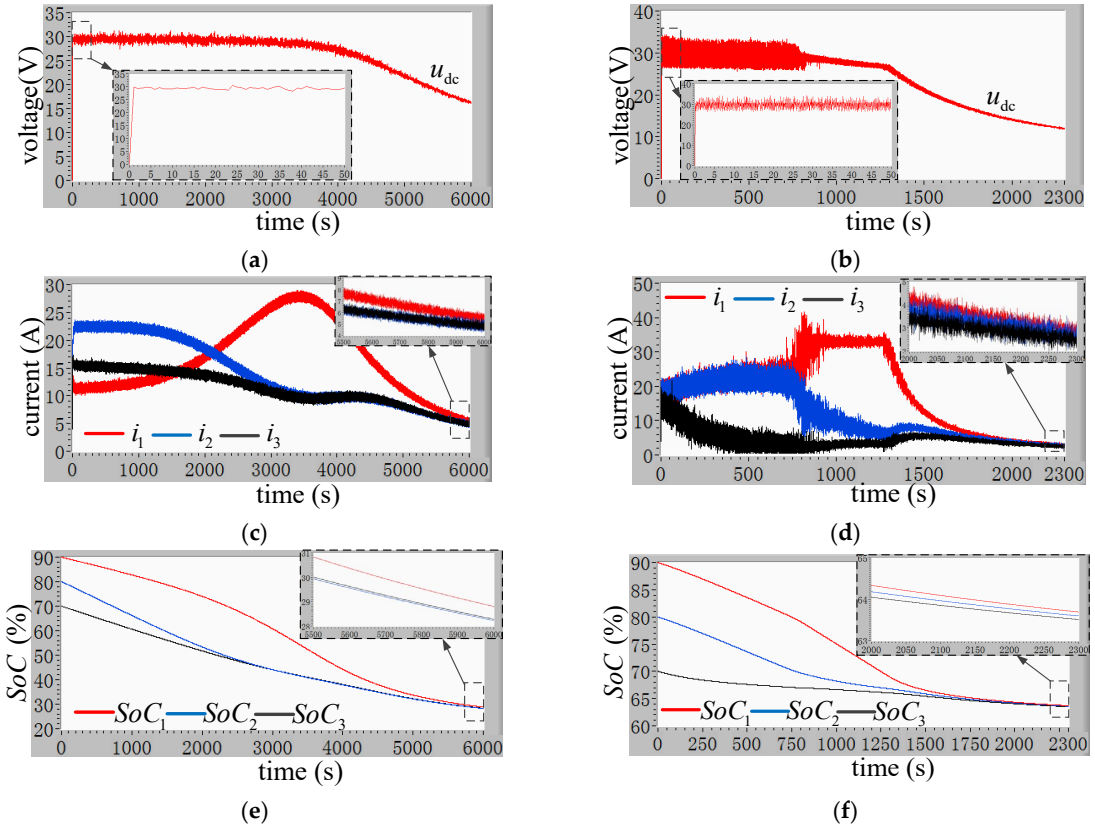


Figure 22. Experimental curves of droop schemes in parallel applications: (**a**) voltage using the method in [2], (**b**) voltage using the method in [10], (**c**) currents using the method in [2], (**d**) currents using the method in [10], (**e**) SoC using the method in [2], and (**f**) SoC using the method in [10].

5. Conclusions

For the ESUs interfacing with boost converters, a fast balancing strategy based on CDRs was designed to eliminate the SoC differences during the discharge process. It is feasible for both parallel and series applications. Instead of energy conservation, accurate SoC estimation and equalization are achieved without the need for extra sensors. Moreover, the balancing duration was remarkably shortened by introducing current saturations into the CDRs. In consideration of the actual execution time, the least significant current, and high current deviation, the accelerating factors in the CDRs were separately chosen for two kinds of applications. Furthermore, the current limits were reasonably selected to reach an equilibrium point and avoid a step reference current. Moreover, the controllers of the dual-loop system were designed to account for enough stability margins. The experimental results obtained under different operating conditions have proven the effectiveness of the proposed strategy. However, this strategy is not feasible at present if the ESUs operate in the charging process or communication fails. Thus, determining how to enhance its reliability and usability will be our concern in the future.

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References

1. Morstyn, T.; Savkin, A.V.; Hredzak, B.; Agelidis, V.G. Multi-agent sliding mode control for state of charge balancing between battery energy storage systems distributed in a DC microgrid. *IEEE Trans. Smart Grid* **2018**, *9*, 4735–4743. [CrossRef]
2. Lu, X.; Sun, K.; Guerrero, J.M.; Vasquez, J.C.; Huang, L. State-of-charge balance using adaptive droop control for distributed energy storage systems in DC microgrid applications. *IEEE Trans. Ind. Electron.* **2014**, *61*, 2804–2815. [CrossRef]
3. Preindl, M. A battery balancing auxiliary power module with predictive control for electrified transportation. *IEEE Trans. Ind. Electron.* **2018**, *65*, 6552–6559. [CrossRef]
4. Ye, Y.; Wang, J.; Wang, X. A multi-winding transformer-based active cell equalizer with self-driven switches for series-connected lithium-ion batteries and super-capacitors. *J. Energy Storage* **2023**, *70*, 107971. [CrossRef]
5. Ye, Y.; Cheng, K.W.E.; Fong, Y.C.F.; Xue, X.; Lin, J. Topology, modeling, and design of switched-capacitor-based cell balancing systems and their balancing exploration. *IEEE Trans. Power Electron.* **2017**, *32*, 4444–4454. [CrossRef]
6. Lee, K.M.; Chung, Y.C.; Sung, C.H.; Kang, B. Active cell balancing of Li-ion batteries using LC series resonant circuit. *IEEE Trans. Ind. Electron.* **2015**, *62*, 5491–5501. [CrossRef]
7. Hsieh, Y.H.; Liang, T.J.; Chen, S.M.O.; Horng, W.Y.; Chung, Y.Y. A novel high-efficiency compact-size low-cost balancing method for series-connected battery applications. *IEEE Trans. Power Electron.* **2013**, *28*, 5927–5939. [CrossRef]
8. Tan, K.T.; Peng, X.Y.; So, P.L.; Chu, Y.C.; Chen, M.Z.Q. Centralized control for parallel operation of distributed generation inverters in microgrids. *IEEE Trans. Smart Grid* **2012**, *3*, 1977–1987. [CrossRef]
9. Díaz, N.L.; Luna, A.C.; Vasquez, J.C.; Guerrero, J.M. Centralized control architecture for coordination of distributed renewable generation and energy storage in islanded AC microgrids. *IEEE Trans. Power Electron.* **2017**, *32*, 5202–5213. [CrossRef]
10. Su, J.; Li, K.; Li, Y.; Xing, C.; Yu, J. A novel state-of-charge-based droop control for battery energy storage systems to support coordinated operation of DC microgrids. *IEEE J. Emerg. Sel. Topics Power Electron.* **2023**, *11*, 312–324. [CrossRef]
11. Zhi, N.; Ding, K.; Du, L.; Zhang, H. An SOC-based virtual DC machine control for distributed storage systems in DC microgrids. *IEEE Trans. Energy Convers.* **2020**, *35*, 1411–1420. [CrossRef]
12. Hoang, K.D.; Lee, H. Accurate power sharing with balanced battery state of charge in distributed DC microgrid. *IEEE Trans. Ind. Electron.* **2019**, *66*, 1883–1893. [CrossRef]
13. Ma, Y.; Wang, S.; Liu, G.; Tian, G.; Zhang, J.; Liu, R. State-of-charge balancing strategy of battery energy storage units with a voltage balance function for a Bipolar DC mircrogrid. *Appl. Energy* **2024**, *356*, 122367. [CrossRef]
14. Mi, Y.; Guo, J.; Fu, Y.; Wang, C.; Wang, P. Accurate power allocation of multienergy storage island DC microgrid based on virtual power rating. *IEEE Trans. Power Electron.* **2023**, *38*, 261–270. [CrossRef]
15. Chowdhury, S.; Shaheed, M.N.B.; Sozer, Y. State-of-charge balancing control for modular battery system with output DC bus regulation. *IEEE Trans. Transp. Electrif.* **2021**, *7*, 2181–2193. [CrossRef]
16. Li, D.; Ho, C.N.M. Decentralized PV–BES coordination control with improved dynamic performance for islanded plug-and-play DC microgrid. *IEEE J. Emerg. Sel. Topics Power Electron.* **2021**, *9*, 4992–5001. [CrossRef]
17. Shi, G.; Han, H.; Sun, Y.; Liu, Z.; Zheng, M.; Hou, X. A decentralized SOC balancing method for cascaded-type energy storage systems. *IEEE Trans. Ind. Electron.* **2021**, *68*, 2321–2333. [CrossRef]
18. Zhang, Q. An improved distributed cooperative control strategy for multiple energy storages parallel in islanded DC microgrid. *IEEE J. Emerg. Sel. Topics Power Electron.* **2022**, *10*, 455–468. [CrossRef]
19. Zeng, Y.; Zhang, Q.; Liu, Y.; Zhuang, X.; Lv, X.; Wang, H. An improved distributed secondary control strategy for battery storage system in DC shipboard microgrid. *IEEE Trans. Ind. Appl.* **2022**, *58*, 4062–4075. [CrossRef]
20. Kang, W.; Chen, M.; Guan, Y.; Tang, L.; Vasquez, J.C.Q.; Guerrero, J.M. Distributed event-triggered optimal control method for heterogeneous energy storage systems in smart grid. *IEEE Trans. Sustain. Energy* **2022**, *13*, 1944–1956. [CrossRef]
21. Bhosale, R.; Gupta, R.; Agarwal, V. A novel control strategy to achieve SOC balancing for batteries in a DC microgrid without droop control. *IEEE Trans. Ind. Appl.* **2021**, *57*, 4196–4206. [CrossRef]
22. Bi, K.; Sun, L.; An, Q.; Duan, J. Active SOC balancing control strategy for modular multilevel super capacitor energy storage system. *IEEE Trans. Power Electron.* **2019**, *34*, 4981–4992. [CrossRef]
23. Wang, P.; Ren, P.; Lu, X.; Wang, W.; Xu, D. A distributed state-of-charge balancing control scheme for three-port output-series converters in DC hybrid energy storage systems. *IEEE Access* **2019**, *7*, 157173–157184. [CrossRef]
24. Xu, W.; Xu, J.; Yan, X. Lithium-ion battery state of charge and parameters joint estimation using cubature Kalman filter and particle filter. *J. Power Electron.* **2020**, *20*, 292–307. [CrossRef]

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