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Compact SOI Dual-Mode (De)multiplexer Based on the Level Set Method

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Abstract: Mode (de)multiplexer is an essential device in integrated multimode photonic systems. Here, we present a dual-mode (de)multiplexer that separates two input modes, TE_0 and TE_1, into two output ports while converting TE_1 to TE_0 mode. Based on the adjoint and level set method, the device features a small footprint of 9.4 μm × 2.9 μm, and a minimum feature size over 200 nm is achieved, affirming stable and reliable fabrication. Through simulations, we observed insertion losses of less than 0.28 dB for TE_0 mode and 0.35 dB for TE_1 mode within the wavelength range of 1500–1600 nm, accompanied by crosstalk levels lower than −30 dB. In our experimental tests, we achieved insertion losses of less than 0.89 dB for TE_0 mode and 0.44 dB for TE_1 modes within the 1530 nm to 1570 nm range, with crosstalk maintained below −25 dB. Furthermore, we conducted an experimental verification of the differences between the standard device and the boundary dilation/erosion device, observing an insertion loss degradation by 0.61 dB within a deviation range of ±40 nm, which demonstrates the device's robustness to the fabrication. The proposed devices exhibit exceptional performance and feature a compact structure, thus holding significant potential for the development of future multimode integrated photonic circuits.

Keywords: silicon photonics; level set method; mode demultiplexer

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1. Introduction

Silicon photonics, with a highly rapid development, is considered as a promising technical field in optical communications and sensing due to its utilization of CMOS compatibility, small footprint, and lower power consumption [1,2]. Recently, an increasing number of optical devices have been reported based on silicon-on-insulator (SOI) platforms, further enhancing the compactness and integration of photoelectric systems [3].

The growing demand for increased communication capacity has become an inevitable challenge, particularly with the advancement of technologies such as cloud computing [4] and big data [5]. Traditionally, parallel data are distinguished by wavelength during data processing and transmission, using a technology known as wavelength division multiplexing (WDM) [6,7]. In response to the need for enhanced signal parallelism, researchers have explored mode division multiplexing (MDM) technology to expand channel capacity. Within the optical waveguide, multiple modes with different orders propagate simultaneously due to the orthogonality between different optical waveguide modes. In MDM systems, different modes are employed for parallel signal transmission, with the mode (de)multiplexer, denoted as mode (de)MUX, serving as a vital device for individual signal detection and processing.

Various methods have been employed to implement mode (de)MUXs, with reported structures including the asymmetric directional coupler (ADC) [8,9], micro ring resonators

(MRR) [10], Y-junctions [11], multimode interference couplers (MMI) [12,13], and subwavelength gratings (SWG) [14]. Among these, the ADC structure, based on phase matching conditions for mode converting, is the most commonly used for (de)MUX devices due to its short coupling length and simple manufacturing process, although its sensitivity to the manufacturing process has been a limitation. The sensitivity can be mitigated by employing tapered structures, as reported by Paredes et al. [9]. An MRR-type device offers the advantage of low crosstalk and compatibility with WDM systems, but they have a relatively narrow operating bandwidth [10]. Y-junction devices, on the other hand, have a broader bandwidth, as demonstrated by Gao et al. in the wavelength range of 1450 nm to 1630 nm [11]. However, Y-junction devices typically have a footprint exceeding 50 µm in length. MMI-based mode (de)MUXs provide low insertion loss and low crosstalk, but they require a larger length, exceeding 400 µm [12,13], which poses challenges for achieving high integration. Moreover, (de)MUX based on SWG structure exhibits relatively low insertion loss (<0.5 dB) and a broad bandwidth (>120 nm) [14]. However, the manufacturing process required for SWG structure production is complex.

The inverse design method has emerged as an innovative approach for designing mode (de)MUX devices, providing an automated and optimized process for searching the optimal solution within a designed region [15,16]. Several algorithms have been proposed for mode (de)MUXs, including particle swarm optimization (PSO) [17], direct binary search (DBS) [18–20], Bayesian DBS [21], density method [22–24], gradient-probability-driven search algorithm (GPDS) [25], and the digitized adjoint method [26]. Based on the PSO algorithm, Chen et al. proposed a four-channel mode (de)MUX that exhibits good scalability [17]. However, due to the issue of premature convergence, PSO may struggle to converge on a suboptimal solution, which can impact the final results. The DBS method, which is powerful and easy to implement, optimizes device performance by dividing the design region into cells and controlling the materials in each cell. However, as a brute force search method, it requires a significant amount of computation, which hampers the optimization speed. To address this challenge, Takeshi Fujisawa et al. proposed an improved DBS method called Bayesian DBS, which reduces the number of iterations needed for optimal structure search. This method has been applied to implement a dual-mode (de)MUX [21]. Both the density method and the GPDS method leverage the gradients of their variables to facilitate rapid convergence of the device structure and achieve high performance. However, both pixel-based and topology-optimization-based approaches can introduce holes and cracks in the device structure. These fine structures can potentially cause additional scattering and dissipation of the optical field, as well as compromise the stability of the manufacturing process. To tackle this issue, Ruan et al. manually removed the island parts from the main body of their designed structure, which was generated based on density method. As a result, an improvement in device performance was demonstrated, with the insertion loss reduced from 0.8 dB to 0.63 dB [27]. However, this approach increases the workload for the designer, particularly when dealing with a large number of intricate structures.

In this paper, we present a compact and high-fabrication-tolerance single-connected mode (de)MUX based on the adjoint and level set method with a footprint of 9.4 µm × 2.9 µm. By utilizing the level set method, only the characteristics of the graphic boundary are evolved. The level set method focuses exclusively on evolving the properties of the graphical boundary, resulting in a final structure that maintains the initial property of being simply connected. This design approach eliminates the presence of hole and crack structures, which could lead to scattering and dissipation. Consequently, it contributes to low loss and high-performance implementation, while enhancing manufacturing stability. In the wavelength range of 1500 nm to 1600 nm, our simulation results demonstrate the insertion losses (ILs) of less than 0.28 dB for TE_0, and 0.35 dB for TE_1, with crosstalk levels (CTs) not exceeding −23 dB for both TE_0 and TE_1. Experimental results validate that the ILs are below 0.89 dB and 0.44 dB for the TE_0 and TE_1 modes, respectively, within the range of 1530 nm to 1570 nm, while CTs remain below −20 dB. For deviations of 40 nm, we achieved

experimental results of 0.93 dB, 1.5 dB (ILs for TE_0 and TE_1), and −13 dB (CTs) in the wavelength range of 1530 nm to 1570 nm. The proposed device exhibits high performance, compactness, and fabrication stability, positioning it as a promising candidate for serving as a fundamental building block in the implementation of on-chip MDM technology.

2. Design Principle

2.1. Design Target

The (de)MUX is designed on the SOI platform with a top silicon layer thickness of 220 nm, and equally thick buried oxide and cladding layers measuring 2 µm each. The device in the design region, as shown in Figure 1, measures 9.4 µm × 3.6 µm. The input waveguide has a width of 0.9 µm to support both TE_0 and TE_1 modes. The output ports solely support the TE_0 mode, with a width of 0.5 µm. The gap between two outputs is 0.8 µm to reduce the mode coupling between them.

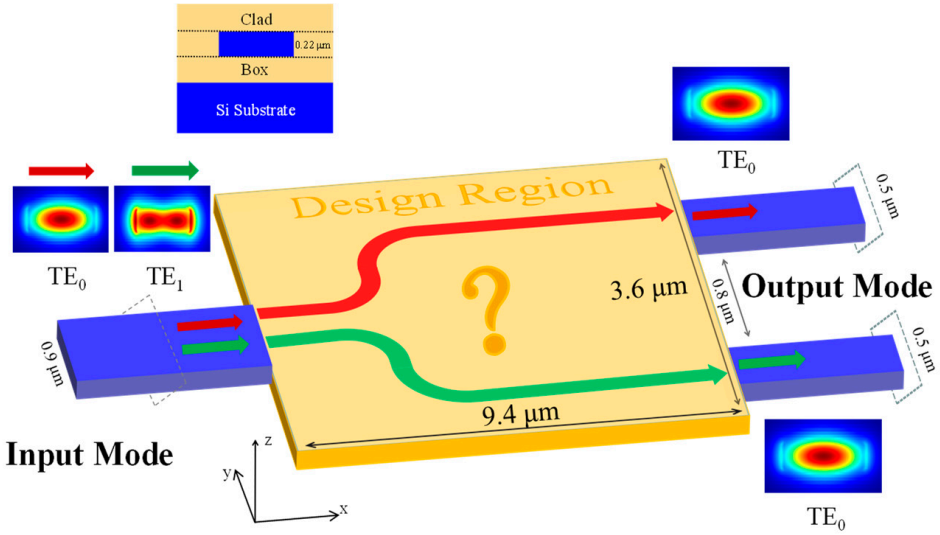

Figure 1. The basic structure of dual-mode demultiplexer. The red line indicates the propagation of the input TE_0 mode, which finally outputs at the first port, while the green line, TE_1, outputs at the second port.

To obtain the desired structure of dual-mode (de)MUX, we first initialized a simple shape in the design region to prepare for the subsequent iterations. To iterate the initial shape towards the optimal structure, we can consider the entire process as a constrained optimization problem. This is because the propagation of mode lights and modal transformation within the waveguide are governed by the constraints imposed by Maxwell's equations,

$$\begin{aligned} \max\ & FOM = f(\boldsymbol{E}, \boldsymbol{H}, \varepsilon_r) \\ s.t.\ & g_i(\boldsymbol{E}, \boldsymbol{H}, \varepsilon_r) = 0,\ i = 1,\ 2\ldots \\ & h_j(\varepsilon_r) \leq 0,\ j = 1,\ 2\ldots \end{aligned} \tag{1}$$

where we define the figure of merit (*FOM*) to assess the performance of a device in terms of the electromagnetic field ($\boldsymbol{E}$, $\boldsymbol{H}$) and the relative permittivity (ε_r). The *FOM* is established by ensuring the fulfillment of Maxwell's equations $g_i(\boldsymbol{E}, \boldsymbol{H}, \varepsilon_r) = 0$, which describe the spatial distribution of $\boldsymbol{E}$ and $\boldsymbol{H}$. The constraint equations $h_j(\varepsilon_r) \leq 0$ impose limitations on the materials and sizes of the designed structure.

In our analysis, we calculate the propagation of the electromagnetic field in the structure for each of the two modes separately. We then multiply their respective *FOM* to obtain the overall *FOM* of the device, rather than simply adding the individual *FOM* together.

Multiplication offers the advantage of maintaining a balanced transmission efficiency between the two modes. The expanded form of the total *FOM* is as follows:

$$\begin{aligned} FOM_{total} &= f_1(\boldsymbol{E}_1, \boldsymbol{H}_1, \boldsymbol{\varepsilon}_1) \cdot f_2(\boldsymbol{E}_2, \boldsymbol{H}_2, \boldsymbol{\varepsilon}_2) \\ &= \prod_{i=1}^{2} \frac{\left| \int_{S_{out}} (\boldsymbol{E_{i,tar}} \times \boldsymbol{H}^*_{\boldsymbol{i,out}} + \boldsymbol{E}^*_{\boldsymbol{i,out}} \times \boldsymbol{H_{i,tar}}) \cdot dS \right|^2}{4 \left[\int_{S_{in}} (\boldsymbol{E_{i,in}} \times \boldsymbol{H}^*_{\boldsymbol{i,in}}) \cdot dS \right] \left[\int_{S_{out}} (\boldsymbol{E_{i,out}} \times \boldsymbol{H}^*_{\boldsymbol{i,out}}) \cdot dS \right]} \end{aligned} \tag{2}$$

where the lower subscript 1 represents the corresponding parameters of TE_0 mode, while the lower subscript 2 indicates TE_1 mode. $\boldsymbol{E_{in}}$ ($\boldsymbol{E_{out}}$) represents the electromagnetic field propagating from the input (output) port as TE_0 ($i = 1$) or TE_1 ($i = 2$), while the target field, denoted as $\boldsymbol{E_{tar}}$, is the distribution of the target electric field on the corresponding port.

To solve the constraint optimization problem, the adjoint method and level set method are employed.

2.2. Adjoint Method

In optimization problems, direct computation of gradients can be computationally expensive, especially when the objective function depends on a large number of variables and their interactions. In contrast, the adjoint method provides a more efficient way to obtain gradient information. The key idea behind the adjoint method is to introduce an auxiliary problem called the adjoint problem, which is derived from the original problem through certain mathematical transformations. For the dual-mode demultiplexer, the gradient $df/d\varepsilon_r$ can be expanded using the chain rule as follows [28]:

$$\frac{df}{d\varepsilon_r} = \frac{df_1}{d\varepsilon_r} \cdot f_2 + \frac{df_2}{d\varepsilon_r} \cdot f_1 \tag{3}$$

Calculating $df_i/d\varepsilon_r$ in Equation (2) directly from the finite difference parameters matrix of the electromagnetic field can be computationally expensive. However, the adjoint variable method provides an alternative approach for computing $df_i/d\varepsilon_r$ by introducing the adjoint electric field and analyzing its electric field propagation in the adjoint problem [29]. The computation of $df_i/d\varepsilon_r$ using the adjoint method is as follows:

$$\frac{df_i}{d\varepsilon_r} = 2k_0^2 \mathrm{Re}(\boldsymbol{E}^T_{\boldsymbol{i,adj}} \cdot \boldsymbol{E_{i,in}}),\ i = 1,\ 2 \tag{4}$$

Here, k_0 represents the wave number in free space, and the adjoint field, denoted as $\boldsymbol{E_{adj}}$, can be regarded as the distribution of the electric field obtained by backwardly inputting the TE_0 mode of the target within the design region.

By solving the adjoint problem alongside the original problem, the adjoint method enables the efficient computation of derivatives or gradients of the objective function with respect to the variables, which allows for the iterative optimization of all the design parameters in an efficient manner, guided by the directionality of the gradients.

2.3. Level Set Method

The level set method is a technique which represents a 2D region as a matrix by utilizing a plane-section of a 3D surface [30]. In the matrix composed of surface data, points with a value of 0 define the boundaries of the evolving structure. Values larger than 0 and less than 0 represent the interior and exterior of the structure, respectively. Consequently, level set method provides a way to evolve the structure by updating the matrices, eliminating the need to find curve equations.

As depicted in Figure 2, the initial device structure can be represented as a 2D matrix using the level set method, which is then mapped onto a 3D surface. Each element in the matrix is denoted as $\Phi(x, y)$, where the silicon material is represented by the set of elements for which $\Phi(x, y) \geq 0$, while the region where $\Phi(x, y) < 0$ corresponds to SiO_2. During the

optimization process, we employ the Hamiltonian–Jacobi equation to iteratively update the matrix $\Phi(x, y)$, as shown below:

$$\frac{\partial \phi(x,y)}{\partial t} + \boldsymbol{V} \cdot \nabla \phi(x,y) = b\kappa \mathrm{Re}|\nabla \phi(x,y)| \quad (5)$$

where t represents the virtual time step; κ denotes the curvature of the set of boundary elements where $\Phi(x, y) = 0$; and b is an adjustable parameter that allows us to control the structure radius, ensuring it meets the requirement for minimum feature sizes of at least 200 nm. The vector $\boldsymbol{V} = df/d\varepsilon_r$ represents the velocity of the curve's points. The structure to be optimized is enclosed by the points where $\Phi(x, y) = 0$. As the optimization progresses, the structure evolves with the points at $\boldsymbol{V} > 0$ expands outward, while the points at $\boldsymbol{V} < 0$ shrinks inward.

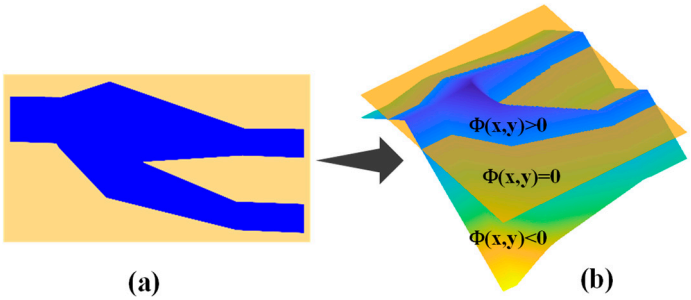

Figure 2. Schematic mapping of the evolutional surfaces from initial structure. (**a**) The initial structure; (**b**) the structure mapping to 3D surface using the level set method.

2.4. Optimization Process

The optimization process flow is illustrated in Figure 3. Firstly, we generate the initial structure and convert it into the $\Phi(x, y)$ function using the level set method. Next, we import the structure into Lumerical solution for 3D-FDTD electron magnetic field (EMF) simulations. For each iteration of TE_0 and TE_1 mode, two simulations are performed. One simulation involves the original TE_0 or TE_1 sources at the input port, while the other simulation involves the adjoint TE_0 source at the corresponding output port. After obtaining the electromagnetic field data from the FDTD monitors, the gradients calculated using the adjoint method are transferred to Matlab. These gradients are used to adjust the velocity values at the boundary points in the level set function, thereby evolving the shape of the design region. The updated structure is then imported back into FDTD for the next iteration. This iterative loop continues until either the FOM value exceeds the required threshold, or the maximum number of iterations is reached. Once the loop terminates, the optimized structure is obtained.

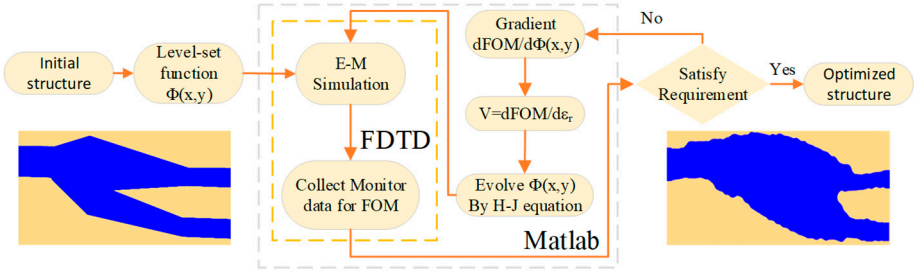

Figure 3. Schematic diagram of the optimization process of the (de)MUX.

We obtain the optimized structure after 200 iterations from the initial structure. Figure 4 illustrates the 3D surfaces mapping of the initial structure (Figure 4a) and the final structure (Figure 4b) using the level set method. Figure 4c displays the total FOM values throughout the optimized process. The entire process takes about 36 h, with the value of FOM increased

from 0.65 to 0.935. We can see that in the first 25 iterations, the FOM function rapidly rises to around 0.9, while the curve of the function exhibits oscillations with an overall upward trend in subsequent iterations. The value exhibits stabilized after 125 iterations, with a final maximum value of 0.935.

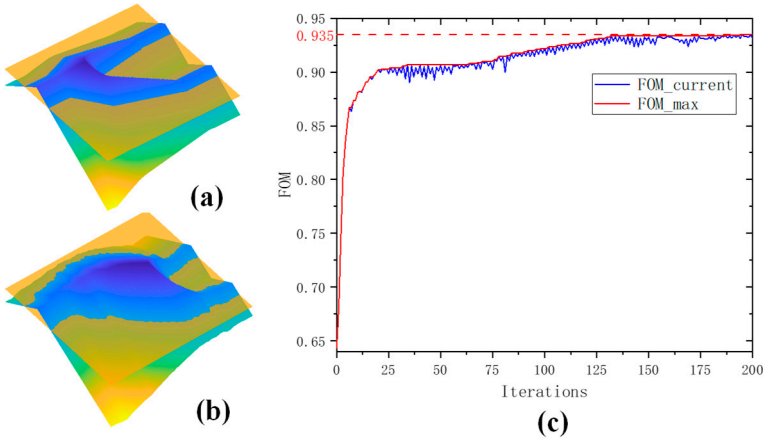

Figure 4. The initial structure (**a**) and the optimized structure (**b**) surface in level set method. (**c**) The value of FOM as the function of iteration numbers.

3. Results

3.1. Simulation

The final optimized structure is shown in Figure 5a, with a footprint of 9.4 µm × 2.9 µm. Figure 5b,c displays the simulations of two modes injected into the device, respectively. The simulations demonstrated that the input TE_0 mode energy was predominantly guided to output 1 port, while the TE_1 mode energy was directed to output 2 port. These results align well with our expectations.

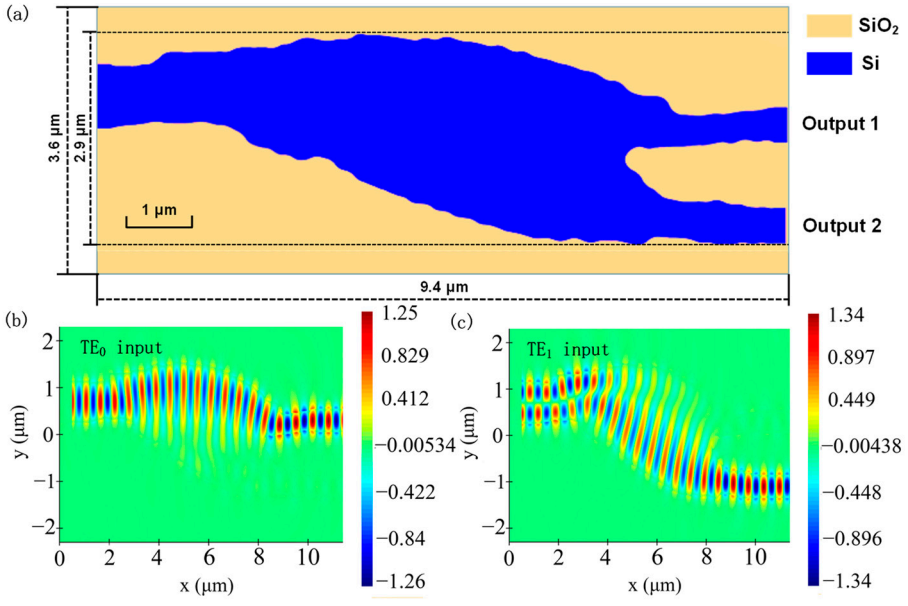

Figure 5. (**a**) Optimized structure of demultiplexer. (**b**) E_y field distribution of the device with a TE_0 input. (**c**) Distribution of E_y field in the device with a TE_1 input.

As depicted in Figure 6, the IL of TE_0 mode was less than 0.28 dB within the wavelength range of 1500–1600 nm, and the IL of TE_1 mode was less than 0.35 dB. At the central wavelength of 1550 nm, the ILs were measured at 0.16 dB for TE_0 mode and 0.14 dB for TE_1 mode. It was observed that the TE_0 mode light exhibited a lower IL at shorter

wavelengths, while TE_1 mode light demonstrated the opposite trend at longer wavelengths. Consequently, these two modes achieved a balance at the central wavelength with the highest FOM values; in other words, the device exhibited minimal insertion loss for TE_0 and TE_1 input overall at 1550 nm. Additionally, the energy coupled to the output 1 port of TE_1 mode and output 2 port of TE_0 mode was characterized by CT, both measuring less than −23 dB.

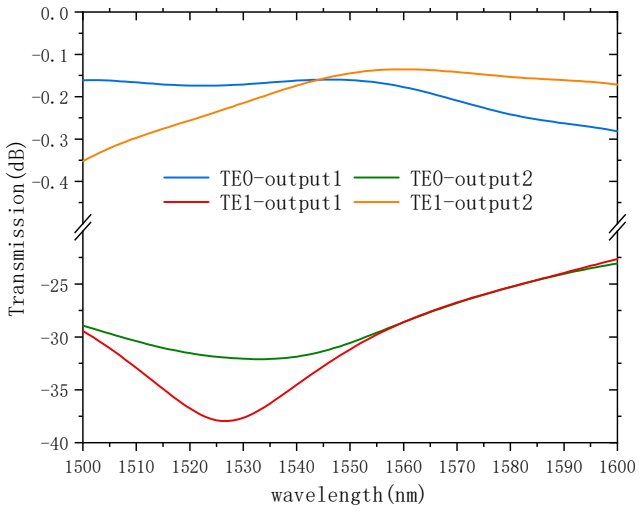

Figure 6. Spectrum of TE_0 and TE_1 dual-mode demultiplexer in the simulation.

Basically, the result of the simulation demonstrated that the device exhibited low IL fluctuation and low CT in the C-band and thus can support wavelength multiplexed signals in the C-band.

3.2. Fabrication Tolerance

During the CMOS fabrication process, particularly in lithography and etching steps, the pattern boundary may undergo dilated expansion or eroded contraction. Shown as Equation (6), we use Δw to represent the deviation:

$$\Delta w = W_{dilated} - W_{origin} = W_{origin} - W_{eroded} \quad (6)$$

Figure 7 shows a schematic of the device with the fabrication deviation. In order to investigate the fabrication tolerance, we swept the deviation of the waveguides and the demultiplexer in the simulation to obtain the losses at the central wavelength 1550 nm.

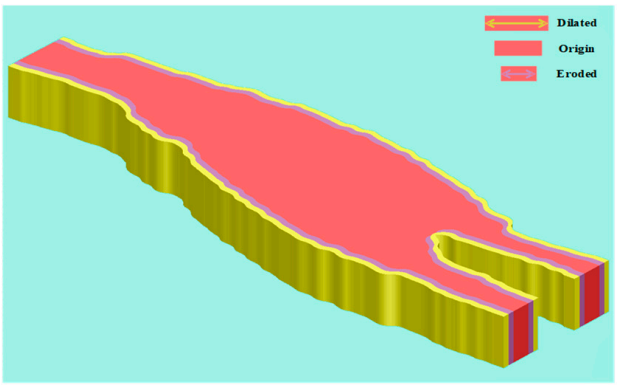

Figure 7. Schematic diagram of the deformation of the device's pattern caused by the lithography and etching step in fabrication.

The results presented in Figure 8a demonstrate that the ILs of two modes were below 1.8 dB in the Δw range of −100 nm to 100 nm. Particularly, when Δw varied from −40 nm to 40 nm, the ILs were consistently less than 0.49 dB. Additionally, the CTs within the range of [−40 nm, 40 nm] were maintained at less than −20 dB. Notably, the modern manufacturing processes in commercial SOI foundries allow for the effective control of geometrical variations within a 40 nm range. Consequently, our device remained stable even in the presence of manufacturing deviations.

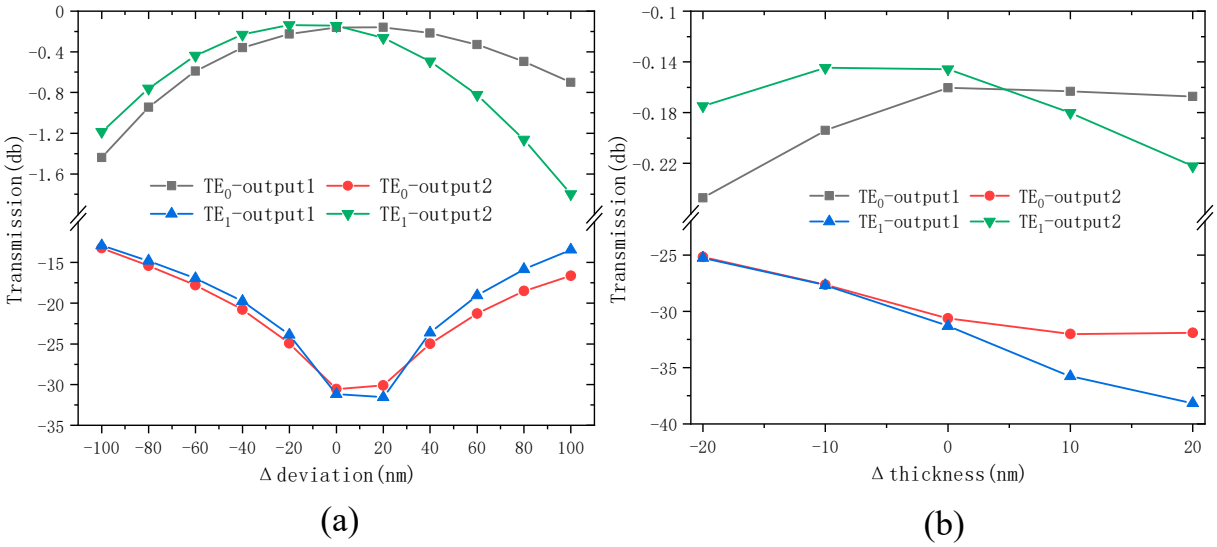

Figure 8. (**a**) The ILs and CTs vs. deviation; whether the device was zoomed in or zoomed out depended on the value of Δdeviation greater or less than 0. (**b**) The ILs and CTs vs. thickness.

Similarly, we also estimated the deviation in the thickness of the top Si layer of SOI wafer. The actual thickness of the device typically fluctuated within a range of 20 nm above and below the original 220 nm. As shown in Figure 8b, with the variation in thickness, the IL was below 0.24 dB for TE_0 mode and 0.22 dB for TE_1 mode, while both two modes had CTs less than −25 dB. Compared with the original-structure values of 0.16 dB, 0.14 dB, and −30 dB for TE_0 mode, TE_1 mode, and the CTs, respectively, we observed no significant deterioration in the results.

3.3. Experiment

The device was fabricated on SOI wafer with electron beam lithography and etching at Applied Nanotool. Figure 9a shows the setup of the experimental apparatus. We used the broadband continuous light from the amplified spontaneous emission (ASE) as the input source and polarized it into linearly polarized light by a polarizer. Then, we coupled the light into and out of the chip by grating couplers and measured the output spectrum of the device by an optical spectrum analyzer (OSA). As shown in Figure 9b, the micrograph of the fabricated structures, we measured the IL and CT by forming (de)MUX into pairs. In addition to measuring the original structures, we additionally measured the performance of the device with the fabrication deviation of ±40 nm. Figure 9c illustrates the microstructure under electron microscopy, revealing a single connected structure for the designed architecture. The absence of holes and gaps within the device contributed to the simplicity and stability in the manufacturing process, while it also played a role in improving device performance, which is discussed further.

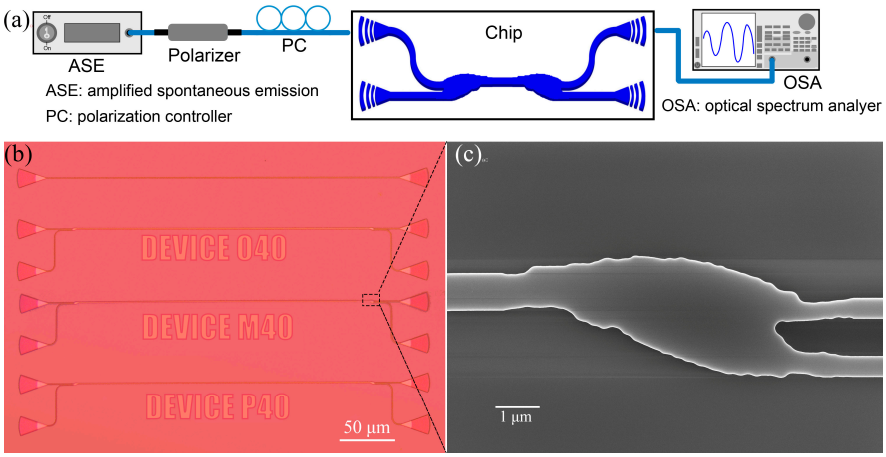

Figure 9. Micrograph of devices that contain dual-mode demultiplexers in the testing experiment. (**a**) The configuration of the experimental apparatus. (**b**) The structures from top to bottom are the waveguide where grating couplers are at the both ends, the waveguides with both sides using dual-mode (de)MUX with the original width, 40 nm inward contraction, and 40 nm external expansion, denoted as Device O40, Device M40, and Device P40, respectively. (**c**) The structure of our device under the scanning of the electron microscopy.

Figure 10 shows the transmission spectra for the structures shown in Figure 9, where Device P40 represents a dilated structure with a positive deviation of 40 nm compared with the original ones (Device O40), while Device M40 represents an eroded structure with a negative deviation of −40 nm.

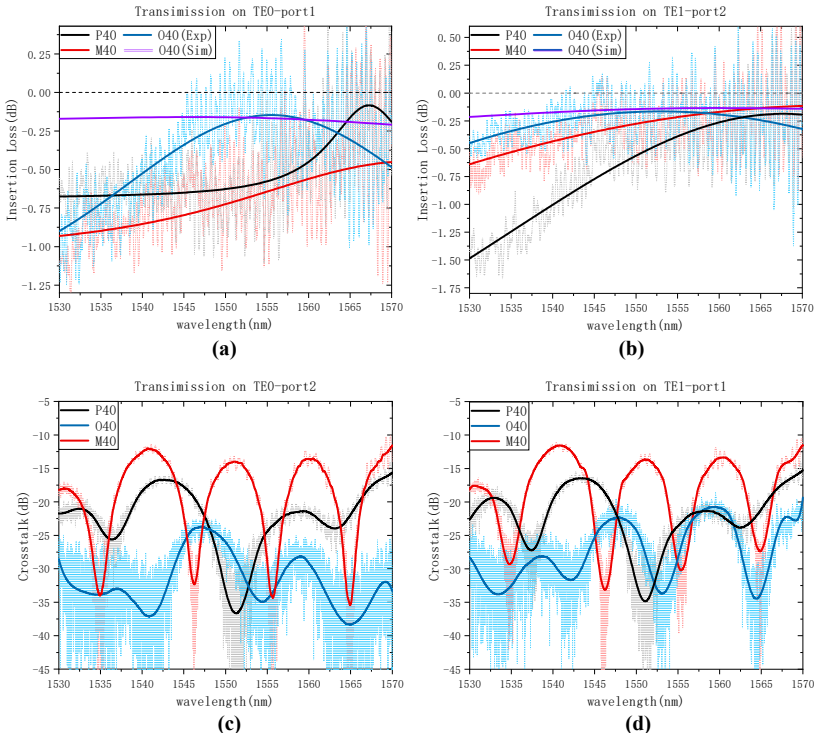

Figure 10. Experiment results of the effect of fabrication deviation on ILs of TE_0 (**a**) and TE_1 (**b**) as well as the CTs of TE_0 (**c**) and TE_1 (**d**). The value of the deviation is [40 nm, 0 nm, −40 nm], represented in the figure as Device P40, O40, and M40, respectively. The ripple curve is attributed to the resonance formed by the reflection between two grating couplers, while the solid traces represent the smooth fit to the corresponding ripple curve.

Figure 10a,b display the insertion losses for TE_0 and TE_1 modes, respectively, and Figure 10c,d shows the CTs of the two modes. For the O40 structure, the average ILs of TE_0 and TE_1 in the wavelength range of 1530 nm to 1570 nm were 0.39 dB and 0.24 dB, respectively, with maximum IL values of 0.89 dB for TE_0 and 0.44 dB for TE_1. For the deviation of ±40 nm, compared with the simulation results, with the IL degradation by 0.36 (0.11) dB for TE_0 (TE_1), the values of ILs were 0.72 dB for TE0 mode and 0.60 dB for TE_1 mode. In the range of 1530 nm to 1570 nm, the losses for TE_0 and TE_1 mode were less than 0.93 dB and 1.5 dB, respectively. The transmission from the TE_0 mode to output 2 port and the transmission from the TE_1 mode were less than −13 dB, −24 dB, and −17 dB, corresponding to P40, O40, and M40, respectively. The measured IL in the experimental data was higher than the simulated data due to the introduced random errors in the electron beam lithography (EBL) and etching steps in the fabrication process, while the misalignment of the grating coupler during the experimental measurement process can lead to slight inconsistency between the experimental and simulated results. However, through comparison with other reported works, which will be discussed below, the experiment results from our experiment are deemed relatively stable. Overall, the results shown in Figure 10 exhibited low insertion loss and high crosstalk suppression for both TE_0 and TE_1 modes in the wavelength of 1530 nm to 1570 nm, indicating the robustness of our device to deviations in an SOI platform.

4. Discussion

Table 1 shows the simulation and experiment results of various reported mode (de)MUX designed by inverse design methods. Our designed device exhibited a remarkable performance with a low IL and CT. Compared to the simulation results of other works, our work demonstrated the lowest insertion loss below 0.35 dB, which validated the advancement of our work. The outstanding performance of our reported device can be explained below. In cases where devices contain more holes and cracks, light tends to scatter and dissipate as it passes through the interfaces, and this could introduce higher scatters and dissipations, resulting in a higher IL. Compared with the optimized structures generated by other DBSs and the density method, our device is simply connected, containing no holes and cracks inside. Therefore, a single-connected structure offers the advantage of minimizing IL.

Table 1. Comparison of the performances of (de)MUX, where the results were obtained from the simulation and the experiment.

Method	Modes	Simulation IL (dB)	Experiment IL (dB)	Experiment CT (dB)	Ref.
Direct binary search	TE_0; TE_1	<0.47 (1530–1590 nm)	<1.0 (1530–1590 nm)	<−24	[18]
	TE_0; TE_1	<1.53 (150 nm in C-band)	<3.0 (138 nm in C-band)	<−18.6	[19]
	TE_0; TE_1	<0.83 (1500–1630 nm)	<1.7 (1525–1565 nm)	<−10.91	[20]
Density topology optimization	TE_0; TE_1	-	<1.5 (1530–1600 nm)	<−25	[22]
	TE_0; TE_1; TE_2	<1.2 (1520–1620 nm)	<3.0 (1520–1620 nm)	<−12	[23]
	TE_0; TE_1	<2.6 (1520–1580 nm)	-	-	[24]
	TE_0; TE_1	<0.63 (the whole O-band)	-	-	[27]
Bayesian DBS	TE_0; TE_1	<0.9 (1270–1330 nm) <1.1 (1530–1570 nm)	<4.2 (1270–1330 nm) <3.4 (1530–1570 nm)	<−22 <−13	[21]
Gradient-probability-driven search algorithm	TE_0; TE_1	<1.0 (1525–1610 nm)	-	-	[25]
Digitized adjoint method	TE_0; TE_1	Avg. 0.68 (1530–1570 nm)	<1.36 (1530–1570 nm)	<−20	[26]
Adjoint and level set method	TE_0; TE_1	<0.35 (1500–1600 nm)	<0.89 (1530–1570 nm)	<−24	This work

Moreover, some of the topologically optimized structures that performed well in the simulation are difficult to manufacture by nanofabrication standards with a restriction of minimum feature size [31]. In contrast, the fabrication of single-connected structures only

requires attention to the contour edges, making the experimental results more consistent with the simulation.

5. Conclusions

In conclusion, we designed and demonstrated a dual-mode (de)multiplexer device on an SOI platform. The device has a compact footprint of 9.4 μm × 2.9 μm and features a simply connected structure with a minimum feature size exceeding 200 nm, ensuring stable fabrication. The experimental results indicate that the device exhibited low IL (<0.89 dB) and low CT (<−24 dB) for both TE_0 and TE_1 modes within the wavelength range of 1530–1570 nm. With a fabrication deviation of 40 nm, the results of IL increased to 1.5 dB and CT to −13 dB, demonstrating sufficient robustness in fabrication. The device's exceptional performance, ultra-compactness, and stable fabrication characteristics make it a promising candidate for large-scale and highly integrated on-chip mode-division-multiplexing systems.

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